PERFORMANCE EVALUATION OF SiC MOSFET AND Si IGBT BASED MULTISTAGE SUPERLIFT DC TO DC CONVERTER.

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Abstract *Multistage super lift Luo converter is a new topology in a step up DC / DC converter with high voltage transfer gain, reduced ripple and low parasitic effects. This paper focuses on characterizing the Silicon carbide (SiC) MOSFET (CMF20120D, 1200V / 33 A) to realize the positive output multistage Superlift converter. The steady state and transient characteristics of SiC MOSFET are studied using LTspice. The proposed converter employing SiC MOSFET is simulated and its performance is compared with the conventional Si IGBT (IRG7PH30K10PBF) of same rating. The performance parameters related to the proposed DC / DC converter under non ideal condition is derived. A prototype of the SiC MOSFET and Si IGBT based super lift Luo converter is developed to validate the results.*

Keywords: *Positive Output Super Lift Luo converter (POSLLC), SiC MOSFET and parasitic effects.*

1. Introduction

Super Lift Converter is a new topology in which the output voltage increases in geometric progression from elementary to n series [1]. The advantages of this converter are reduced ripple voltage and current, high voltage transfer gain. Output voltage in super lift converter is increased by pumping the energy stored in the inductors and stage capacitors to the output load. Based on the number of inductors in the topology [2-4], it is classified into Positive Output Super Lift Luo Converter (POSLLC) and Negative Output Super Lift Luo Converter and this paper focuses on POSLLC. Positive output super lift relift type Luo converter consists of two inductors and one switch. Cree CMF20120D spice model [5] is used to realize the SiC switch in converter topology using LTspice simulation software package. Performance of the converter is evaluated in terms of variation ratio of the inductor current, variation ratio of the capacitor voltage and switching losses and it is compared with Si IGBT. Hardware of the proposed SiC MOSFET and Si IGBT based Luo converter is implemented to prove the enhanced performance of the converter with wide gap semiconductor device.

2. Principle of operation of positive output relift type luo converter.

POSLLC consist of two inductors L_1 and L_2, Switch S, four capacitors C_1, C_2, C_3, C4 and load resistance R shown in Figure 1. Two modes of operation of the converter during switch ON and OFF are shown in Figure 2 and Figure 3. In mode-1 operation, when the switch is closed the current through the inductor L_1 increases and the capacitor C_1 is charged to the supply voltage V_{in}. Diode D_2 is reverse biased by the positive voltage V_1 at the capacitor C_2. Current through the inductor L_2 raises linearly with the voltage V_1 and the Capacitor C_3 is charged to the voltage V_1. Diode D_5 is reverse biased by the output voltage V_0 across the capacitor C_4 , the output voltage across the capacitor C_4 is discharged to the load resistor R [6]. During mode -2 operations, when the switch is in the OFF condition as shown in Figure 3, voltage polarity across the inductor changes and the current through the inductor L_2 decreases linearly. Diode D_1 is reverse biased by the voltage across the capacitor C_1.

Capacitor C_2 is charged to the voltage V_1 at this mode. Voltage polarity across the inductor is changed and the current through the inductor L_2 decreases linearly. Voltage across the capacitor C_3 reverse biases the diode D_3 and the capacitor C_4 is charged to the output voltage V_0.

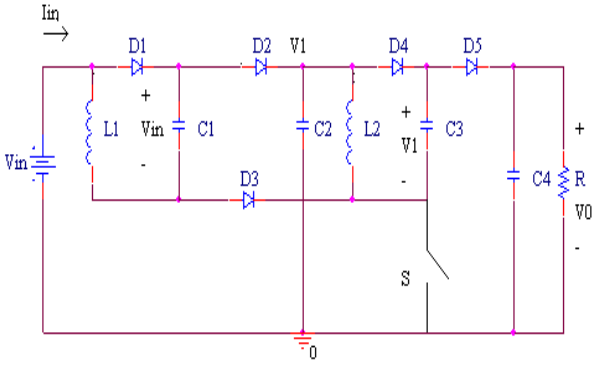


Fig. 1. Positive output relift type Superlift luo converter

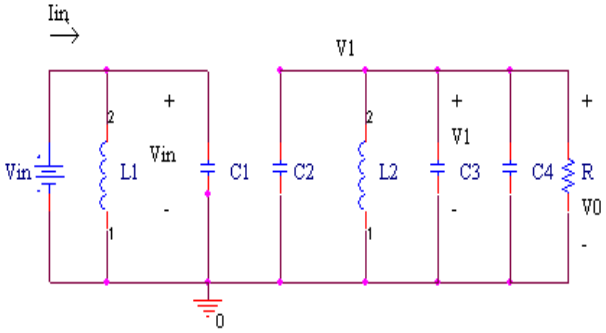


Fig. 2. Mode 1 operation

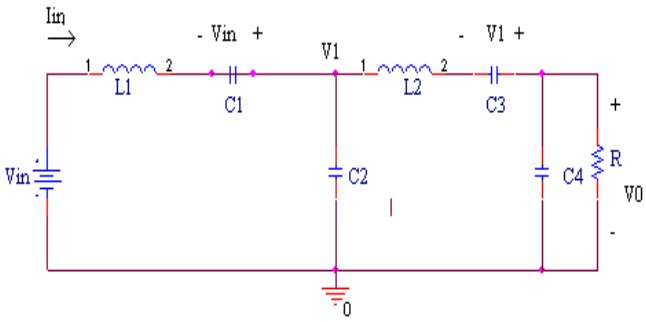


Fig. 3. Mode 2 operation

During ON mode capacitor C_1 is charged to the supply voltage V_{in} and capacitor C_2 is charged to the voltage V_1. Current through the inductor i_{L2} increase with the voltage V_1 and decreases with the voltage V_0-$2V_1$.

By equating the ripple in the inductor current L_2.

$$V_{iL2} = \frac{V_1}{L_2} KT = \frac{(V_0 - 2V_1)}{L_2}(1-K)T$$

$$V_1 = \left(\frac{2-K}{1-K}\right) \quad (1)$$

$$V_o = \left(\frac{2-K}{1-K}\right) V_1 = \left(\frac{2-K}{1-K}\right)^2$$

Voltage transfer gain is $G = \frac{V_0}{V_{in}} = \left(\frac{2-K}{1-K}\right)^2$ (2)

Average Inductor Current $I_{L1} = \frac{I_{in}}{2-K}$ (3)

Average Inductor Current $I_{L2} = \left(\frac{2-K}{1-K} - 1\right) I_0$ (4)

Variation ratio of inductor current i_{L1} is

$$\partial_1 = \frac{V_{iL1}/2}{I_{L1}} = \frac{K(1-K)^4}{2(2-K)^3} \frac{R}{fL_1} \quad (5)$$

Variation ratio of inductor current i_{L2} is

$$\partial_2 = \frac{V_{iL2}/2}{I_{L2}} = \frac{K(1-K)^2}{2(2-K)} \frac{R}{fL_2} \quad (6)$$

Variation ratio of output voltage V_o is

$$\partial = \frac{V_{Vo}/2}{V_o} = \frac{(1-K)}{2RfC_4} \quad (7)$$

By using equations (1) – (7), the proposed converter can be designed.

3. Silicon Carbide (SiC) MOSFET

Wide band gap materials such as SiC, GaAS and GaN are available, out of which SiC is most well developed one in realization of power devices. SiC based devices have wide band gap of 3.2 eV, due to which there is a reduction in carrier concentration and increase in dielectric strength. Thermal conductivity of the SiC device is much better when compared to the Si device of same rating [7-11]. In order to evaluate the potential utilization of the SiC MOSFET in the proposed converter system a commercially available Cree's CMF20120D (1.2 kV, 33 A) device is used.

4. SiC MOSFET Characterization

The device characterization are carried out under varying temperatures from 25° C to 125° C to show the superiority of the device under high junction

temperature. Dynamic and static characteristics of the device were studied using LTspice simulation software. The static characterization of the MOSFET includes transfer characteristics, output characteristics, leakage current characteristics, on-state resistance characteristics and body diode characteristics. These characteristics are useful in evaluating the performance of the SiC MOSFET. I_{DSS} characteristics evaluates the device blocking capability by measuring the drain- source leakage current at rated blocking voltage with gate source terminals shorted. From the Figure 4, it is clear that at 25° C the leakage current is 1 µA and at 125°C the leakage current is 16 µA. Characteristics shows a positive temperature coefficient for I_{DSS} with very low leakage current indicating a good blocking capability of the device at the rated voltage.

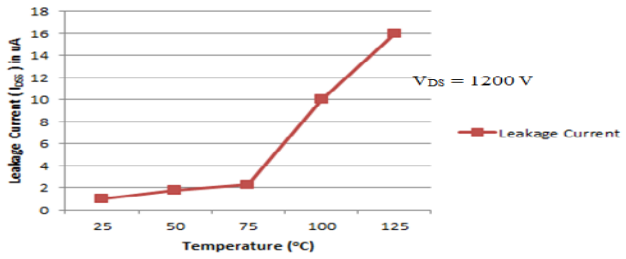


Fig.4. Leakage current (I_{DSS}) vs. Temperature Characteristics

Transfer characteristics as shown in Figure 5, were drawn by measuring the variation of drain current (I_D) with respect to the gate source voltage (V_{GS}) .at drain source voltage (V_{DS}) equal to 50 V and 100V. The gate source threshold voltage ($V_{GS\text{-}th}$) is equal to 2.6 V and transconductance (g_{fs}) which is a measure of relative sensitivity of the drain current (I_d) with respect to the gate voltage (V_{GS}).Calculated g_{fs} for V_{DS} equal to 100 V is 0.375 S.It is observed that at high temperature the threshold voltage of the device and transconductance increases [12].

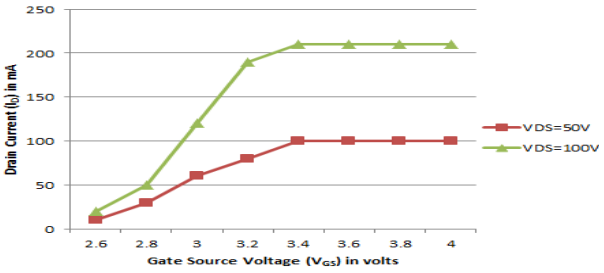


Fig. 5. Transfer Characteristics

Output characteristics of the power MOSFET is the variation of drain current (I_D) with respect to the drain source voltage (V_{DS}) with constant gate source voltage (V_{GS}). From the Figure 6 it isfound that SiC MOSFET goes into saturation at prolonged period thereby pinch off point is increased [13].

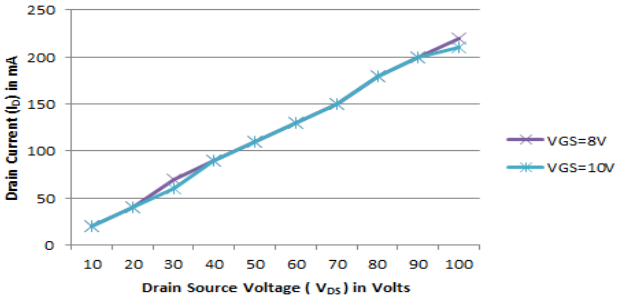


Fig. 6. Output Characteristics

The on-state resistance determines the conduction losses; it is directly measured from the output characteristics [14]. Resistance is measured at V_{DS} = 2 V and 20 V with variation in temperature. It is obvious from Figure 7. That the variation of on state resistance is in milli ohms for the entire range of temperature.

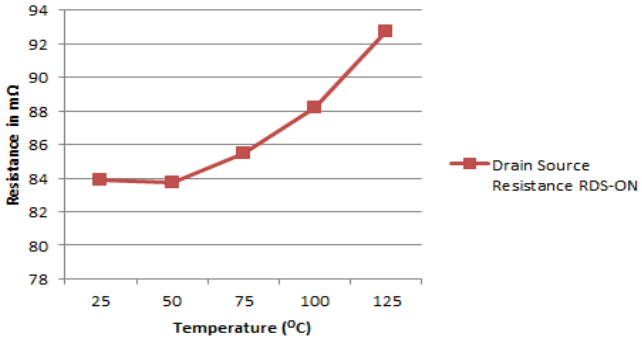


Fig. 7. ON Resistance vs Temperature Characteristics

The dynamic behaviour is described by the switching characteristics of the power MOSFET. The intrinsic capacitances, resistance, gate charge and reverse recovery characteristics of the body diode plays a significant role in the dynamic performance of the device. Dynamic characteristics of the power MOSFET were simulated using clamped inductive and resistive load switching test [15]. Table 1 compares the turn on and turn off times of the devices under resistance switching test. From the result, it is clear that turn off time of the SiC MOSFET is one third of the Si IGBT. Clamped inductive switching test results are shown in table 2.Since the switching time of the SiC device is very less it is suitable for high efficiency converters, employed in renewable energy conversion applications.

Table. 1 Resistance Switching Comparison

Device	Turn ON time (t_{ON}) in µs	Turn OFF time (t_{OFF}) in µs	Condition
CMF20120D SiC MOSFET	0.08916	0.2573	V_{DS} = 100 V,F_S = 100 kHz and load R=100Ω/50W
IRG7PH30K10pbf Si IGBT	0.08367	0.839	V_{DS} = 100 V,F_S = 100 kHz and load R=100Ω/50W

Table. 2 Clamped Inductive Switching Comparison

Device	Turn ON time (t_{ON}) in µs	Turn OFF time (t_{OFF}) in µs	Condition
CMF20120D SiC MOSFET	0.05179	0.36174	V_{DS} = 100 V,F_S = 100 kHz and Inductive load
IRG7PH30K10pbf Si IGBT	0.0828	0.48768	V_{DS} = 100 V,F_S = 100 kHz and Inductive load

5. Comparison of SiC MOSFET with Si IGBT

Important parameters of SiC MOSFET and Si IGBT are listed in Table 3.On-state resistance of the SiC MOSFET is one third of the Si IGBT, which leads to reduced conduction loss of the switch. The output capacitance of the SiC MOSFET is twice that of the Si IGBT as a result the energy stored in output capacitance of SiC MOSFET during off-state is significant. Thermal resistance of the SiC MOSFET is slightly lesser than Si IGBT thereby the cooling requirements and power density of the converter can be reduced.

Table. 3 Comparison of SiC MOSFET and Si IGBT under study

Part Number	**CMF20120D**	**IRG7PH30k10PBF**
Material	SiC	Si
Device	MOSFET	IGBT
Voltage Rating (V_{DS})	1200 V	1200 V
Current Rating (I_{DS}) continuous at 25^0 C	33 A	33 A
ON-State Resistance ($R_{DS\text{-}on}$)	80 mΩ	261 mΩ
Total Gate Charge	90.8 nC	45 nC
Gate to Drain Charge Q_{GD} / Gate to Collector Charge Q_{GC}	43.1 nC	20 nC
Gate to Source Charge Q_{GS} / Gate to Emitter Charge Q_{GE}	23.8 nC	8.7 nC
Body diode reverse recovery	Yes	No
Gate Threshold voltage $V_{GE(th)}$	2.5 V	5.0 V
Output Capacitance C_{oss}	120 pF	63 pF
Thermal Resistance , junction to case $R_{\theta jc}$	0.58^0 C/W	0.7^0 C/W

6. Simulation of Two Stage Superlift Converter

Based on the design equations, SiC MOSFET based super lift Luo converter is simulated in LTspice and the design parameters are shown in Table 4. CREE SiC MOSFET model and International Rectifier IGBT model is used in the simulation. Energy storage element inductor L_1 is designed by assuming the inductor ripple current equal to 10% of the input current and inductor L_2 is designed by assuming the inductor ripple current equal to 10% of the output current. Output capacitor C_4 is designed by considering 1% of ripple in the output voltage. Capacitors C_1 to C_3 are assumed to be equal to the value of the output capacitor.

Table.4 Parameters for Two stage Superlift converter

Parameters	**Value**
Input Voltage (V_{in})	5-30 V
Output Voltage (V_0)	45-270 V

Inductor (L_1)	106 µH
Inductor (L_2)	8.5 mH
Capacitor (C_1 to C_4)	220 µF
Switching Frequency (f)	100 kHz
Load Resistance (R)	470 Ω
Desired duty cycle (k)	0.5

LTspice simulation software is used to simulate the Superlift converter with Cree SiC MOSFET model and International Rectifier IGBT model. In the Superlift Luo converter the switches are configured in the low side mode and the gate pulse width is fixed to 50 % duty cycle. Performance evaluation of the converter is studied to evaluate the efficiency of the converter under varying input voltage, inductor ripple current and capacitor output voltage ripple for a varying switching frequency.

Table.5 Efficiency Computation of SiC MOSFET based Superlift converter

Input voltage (V)	Output voltage (V)	Output Power (W)	Input Power (W)	Power Loss (W)	Efficiency (%)
5	43.29	3.987	4.57	0.583	87.24
10	90.054	17.255	18.867	1.612	91.45
15	136.82	39.83	42.85	3.02	92.95
20	183.58	71.708	76.54	4.832	93.68
25	230.3	112.85	119.89	7.04	94.127
30	276.96	163.21	172.87	9.66	94.41

Table 5 represents the efficiency computation of the SiC MOSFET based power converter with variation in the input voltage from 5 V to 30 V. It is observed from the table that efficiency varies from 87 % to 95 %.

Table.6 Efficiency Computation of Si IGBT based Superlift converter

Input Voltage (V)	Output Voltage (V)	Output Power (W)	Input Power (W)	Power Loss (W)	Efficiency (%)
5	42.858	3.908	5.57	1.662	70.1
10	88.883	16.809	20.78	3.98	80.85
15	136.49	36.639	46.26	9.624	79.197
20	181.54	70.12	78.14	8.026	89.72
25	224.06	106.82	115.6	8.83	92.36
30	271.67	157.03	170.3	13.3	92.19

Table 6 represents the efficiency computation of the Si IGBT based power converter with variation in the input voltage from 5 V to 30 V. It is observed from the table that efficiency varies from 70 % to 93 %.

Table .7Ripple effect on SiC MOSFET based Superlift converter

Frequency (kHz)	Inductor Ripple Current (ΔI_{L1}) mA	Inductor Ripple Current (ΔI_{L2}) mA	Output Voltage Ripple (ΔV_0) mV
100	136.29	7.96	2.062
200	70.37	4.16	1.096
300	47.24	2.82	0.77
400	35.91	2.17	0.62
500	29.15	1.77	0.52

Ripple effect on SiC MOSFET based power converter is represented in the table 7. Inductor ripple current and output voltage ripple is influenced by the switching frequency of the converter. At 500 kHz switching frequency, the inductor ripple current and output voltage ripple is less than 25% of the value at 100 kHz frequency. Since the ripple effect is less the size of inductor and capacitor will be reduced.

Table.8 Switching frequency impact on SiC MOSFET based Superlift converter

Frequency (kHz)	**Turn-On time (t_{On}) (ns)**	**Turn-Off time (t_{Off}) (ns)**	**Switching Loss (P_{SW}) mW**
100	374.08	205.85	283.75
200	343.25	210.77	603.61
300	344.30	201.193	974.43
400	343.48	203.736	1403
500	219.12	191.75	1246

Impact of switching frequency on SiC MOSFET based power converter is represented in the table 8. From the table, it is observed that turn-on and turn-off time is reduced and switching loss of the converter is increased at high frequency.

Ripple variation with respect to switching frequency in Si IGBT based power converter is represented in table 9. From the table, it is observed that inductor ripple current and output voltage ripple is reduced. The variation in ripple is comparable with respect to SiC based power converter.

Table .9 Ripple effect on Si IGBT based Superlift converter

Frequency (kHz)	**Inductor Ripple Current (ΔI_{L1}) mA**	**Inductor Ripple Current (ΔI_{L2}) mA**	**Output Voltage Ripple (ΔV_0) mV**
100	112.78	6.79	1.85
200	55.912	3.62	1.067
300	39.34	2.58	0.81467
400	30.05	2.07	0.696
500	24.66	1.76	0.591

Table.10 Switching frequency impact on Si IGBT based Superlift converter

Frequency (kHz)	**Turn-On time (t_{On}) (ns)**	**Turn-Off time (t_{Off}) (ns)**	**Switching Loss (P_{SW}) mW**
100	534.83	690.33	4209
200	459.39	576.22	1080
300	435.79	626	2090
400	668.69	589.4	4760
500	597.21	537.85	6160

Switching loss of the Si IGBT based power converter with variation in frequency is shown in table 10. At frequency 500 kHz, the increase in switching loss is almost 5 times that of SiC based converter, this impact is due to increase of tail current in the device.

7. Converter Performances Comparison

Converter efficiency with fixed switching frequency and varying input voltage is shown in Figure8. From the graph, it is clear that the efficiency of the SiC MOSFET is above 80% far a variation in input voltage from 5 V to 30 V.

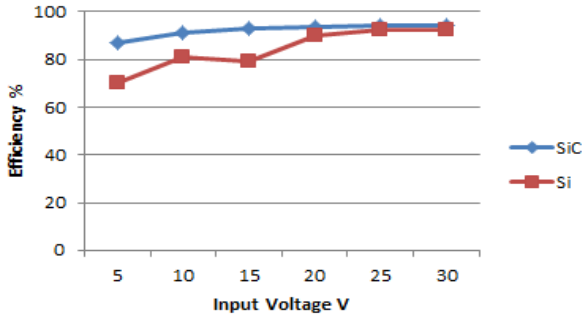


Fig. 8. Converter efficiency for variation in input voltage with constant switching frequency.

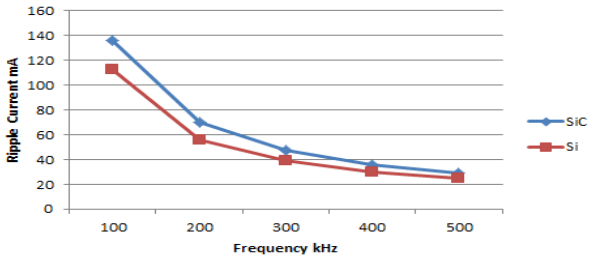


Fig.9.Inductor L_1 ripple current with varying switching frequency

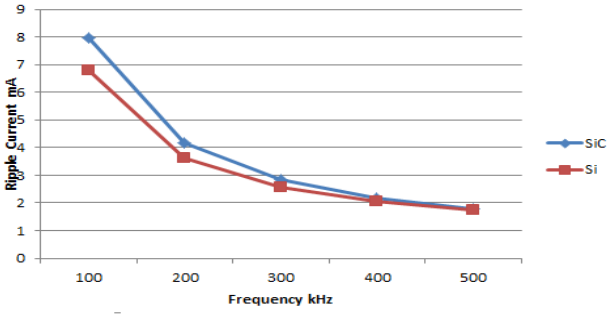


Fig.10.Inductor L_2 ripple current with varying switching frequency

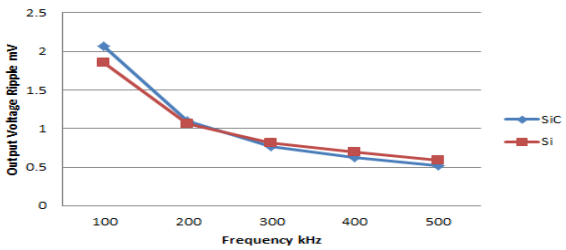


Fig.11.Output voltage ripple with varying switching frequency

At low frequency, SiC MOSFET based converter Inductor L1 ripple current is comparable to Si IGBT based converter. It is clear that the ripple current of the SiC based converter is less than Si IGBT based converter at high frequency as shown in Figure 9. Inductor L_2 ripple current for SiC based converter is comparable with respect to Si IGBT based converter for varying switching frequency as shown in Figure 10. Variation in the output voltage with respect to frequency is shown in Figure 11. From the graph it is clear that the ripple voltage is comparable with respect to variation in switching frequency for both the converters.

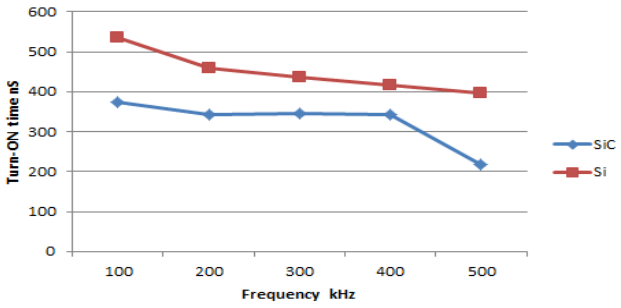


Fig.12.Turn-ON time (vs.) switching frequency

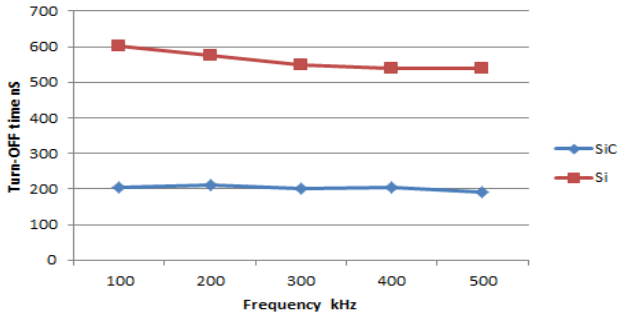


Fig.13.Turn-OFF time (vs.) switching frequency

Variation in turn on time and turn off time with respect to switching frequency for SiC MOSFET based converter and Si IGBT based converter are shown in Figure 12 &Figure 13. From the graph it is clear that the turn on time and turn off time for SiC based converter is less when compared to Si IGBT. Turn off loss of the SiC MOSFET based converter is fairly constant with variation in switching frequency

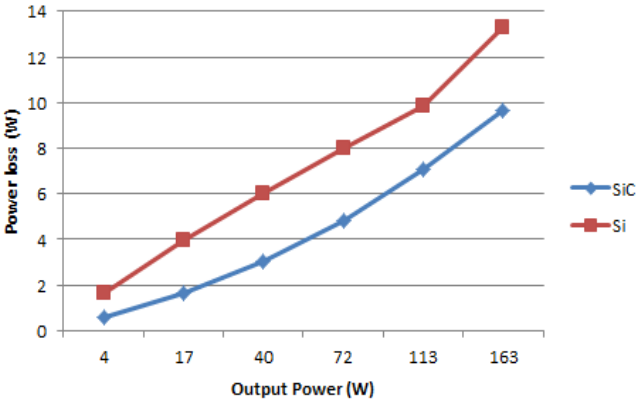


Fig.14. Power loss (vs.) Output Power

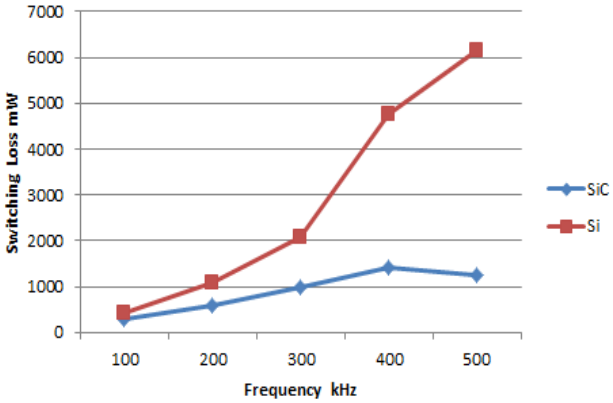


Fig.15.Switching loss (vs.) Frequency

Power loss and switching loss of the converter are shown in Figure14&15. Effect of switching frequency on switching losses reveals that losses for SiC based converter is less when compared to Si based converter. At very low output power the power loss is considerable when compared to high power output, the power loss for SiC based converter is less compared to Si IGBT based converter.

8. Non-ideal Relift converter

In non-ideal relift converter the parasitic effects [16] of active and passive components are considered. Equivalent circuit with parasitic is shown in Figure 16. Turn-on and turn-off equivalent are shown in Figure 17 and Figure 18.

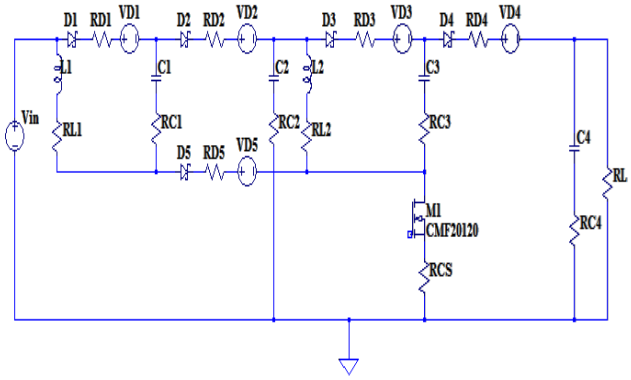


Fig.16.Equivalent circuit with parasitic

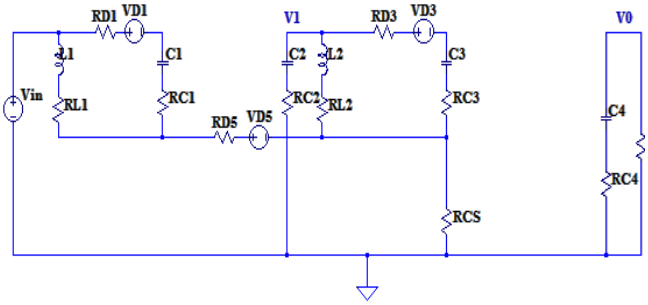


Fig.17. Turn-on equivalent with parasitic

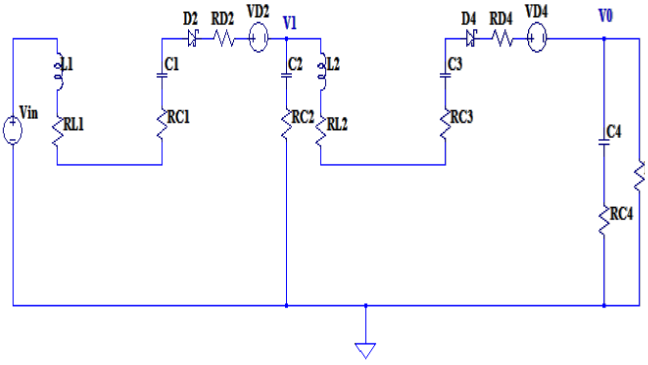


Fig.18. Turn-off equivalent with parasitic

Non ideal converter voltage gain

$$V_0 = [S] + V_{C3} - V_{D4} - K_4 I_{in2} \quad (8)$$

$$S = (V_{in} + V_{C1} - V_{D2} - D\,V_{C1} + D\,V_{D2} - D\,V_{D5} + K_1 I_{in1}(D-1) - I_{L1} R_{L1} D - K_2 I_{in1} D - K_3 I_{in2} D) / (1 - D)^2$$

$K_1 = R_{L1} + R_{C1} + R_{D2}$
$K_2 = R_{D5} + R_{CS}$
$K_3 = R_{CS}$
$K_4 = R_{L2} + R_{C3} + R_{D4}$
I_{in1} = First stage input current
I_{in2} = Second stage input current
R_{L1} = Equivalent series resistance of an Inductor L_1
R_{L2} = Equivalent series resistance of an Inductor L_2
R_{C1} = Equivalent series resistance of a capacitor C_1
R_{C3} = Equivalent series resistance of a capacitor C_3
R_{CS} = ON state resistance of a switch
R_{D2} = ON resistance of a diode D_2
R_{D5} = ON resistance of a diode D_5
R_{D4} = ON resistance of a diode D_4
V_{D2} = Forward voltage drop of a diode D_2
V_{D4} = Forward voltage drop of a diode D_4
V_{D5} = Forward voltage drop of a diode D_5

Table.11.Comparision of ideal and non- ideal converter output voltage

Input voltage (V_{in})	Ideal converter Output Voltage(V_o)	Non ideal converter Output Voltage (V_o)
5	43.29	32
10	90.054	75
15	136.82	118
20	183.58	161
25	230.3	204
30	276.96	245

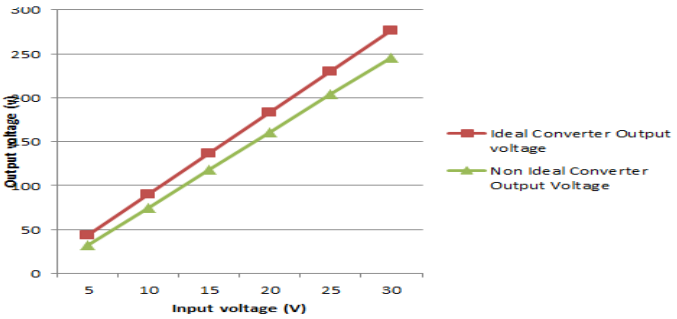


Fig.19.Output voltage of ideal and non- ideal Converter

Effect of non- idealities in the two stage Superlift converter is shown in fig.19. It is evident that the effect of parasitic due to active and passive components is predominant. This effect can be mitigated by proper selection of components with minimal parasitic

9. Hardware implementation of two stage Superlift converter

A prototype of two stage super lift converter is implemented, to validate the simulation results. Table .12. shows the converter components, driver circuit components and specifications used in the implementation. From the super lift converter configuration, it is evident that the switch is connected in low side switch mode. Cree CRD-001 [17]. SiC MOSFET dedicated driver circuit board is used, to trigger the MOSFET in the two stage Superlift converter. Variable frequency and variable duty cycle firing pulses is generated using dspic30f4011 microcontroller. For Si IGBT based power converter low side driver IC MICREL 4422YN [18] is used and the opto isolator HCPL 3020 [19] is used for isolating the power circuit from the firing circuit.

Table.12. Hardware circuit components and specifications

Hardware Component and Specification	**SiC based Converter**	**Si based converter**
Input Voltage (V_{in})	5-12 V	5-12 V
Inductor (L_1)	106 µH	106 µH
Inductor (L_2)	8.5 mH	8.5 mH
Capacitor (C_1 to C_4)	220 µf / 165 V	220 µf / 165 V
Switch	CMF20120D	IRG7PH30K10PbF
Diode	SR360	SR360
Driver IC	IXDN 609SI non inverting	MC 4422 YN non inverting
Opto isolator	ACPL-4800-300E	HCPL -3020
Gate voltage (V_{GS})	20 V	20V
Load	470 Ω / 50 W	470 Ω / 50 W

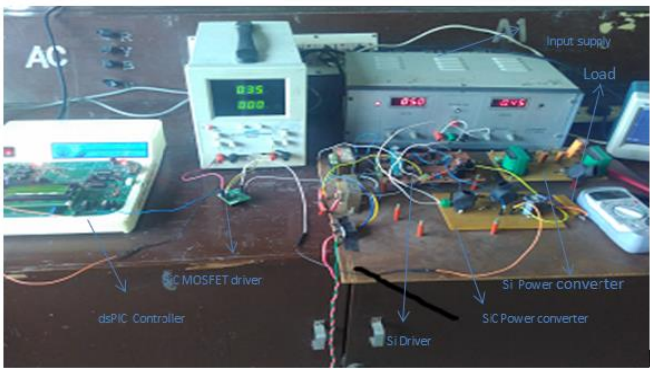


Fig.20. Experimental Setup of two stage Superlift converter

To validate the simulation results, power converter input voltage is set to three different values such as 5 V, 10 V and 12 V. For an input voltage of 5 V, first stage and second stage output voltage are shown in Figure 21.To measure the inductor ripple current, sensing resistors are used.

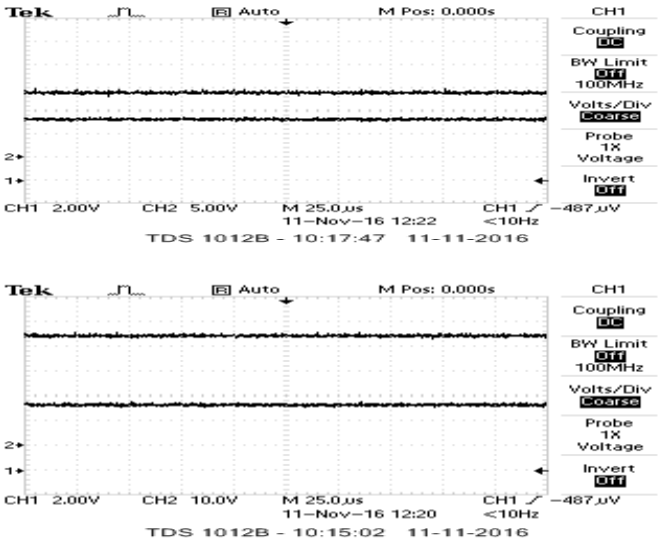


Fig.21. First stage and second stage output voltage of Superlift converter.

From the graph it is observed that the first stage voltage lift V_1 is approximately equal to 15 V and the second stage voltage lift V_0 is equal to 42 V. Ripple in the Inductor current L_1 and L_2 are shown in Figure 22.

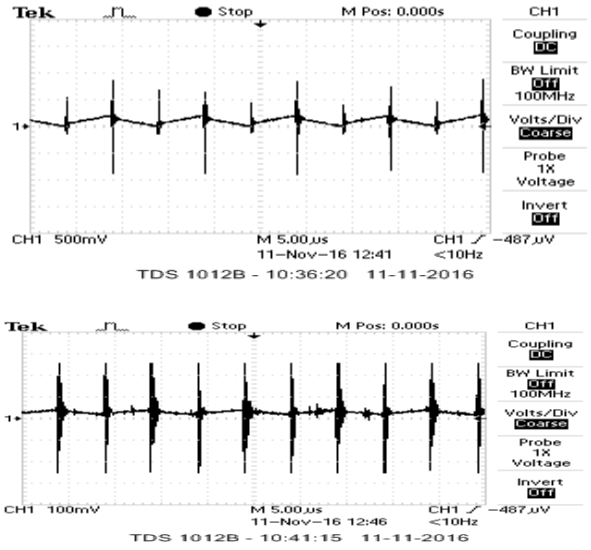


Fig.22. Inductor L1 and L2 ripple current

From the graph, it clear that high frequency ringing is present in the inductor ripple current at switching instant. These ringing can be mitigated by adding a decoupling capacitor during measurement. Switching instant parameter related to turn on and turn off instant is shown are in Figure 23. Channel 1 represents the V_{DS} drain source voltage and its approximately equal to 30 V and drain current i_{ds} equal to 200 mA. Gating pulse waveform is shown in Figure 20 with frequency equal to 100 kHz and duty cycle is 50 %.

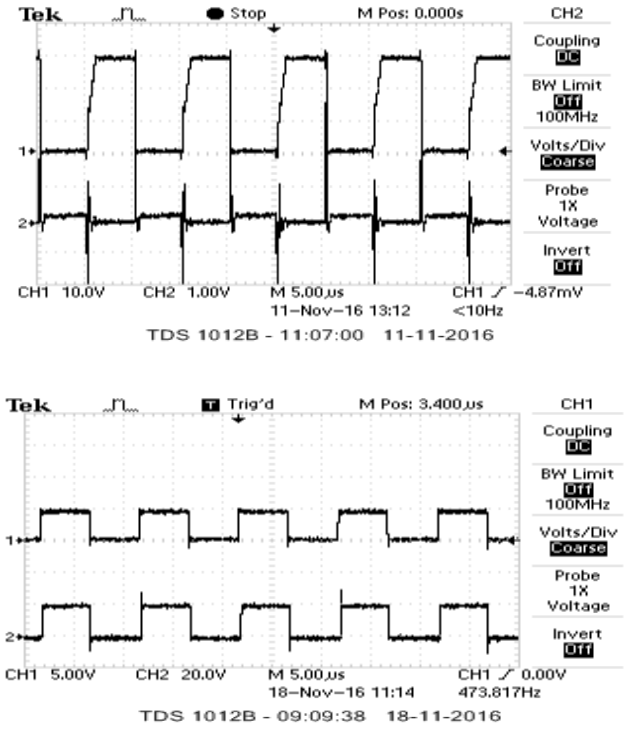
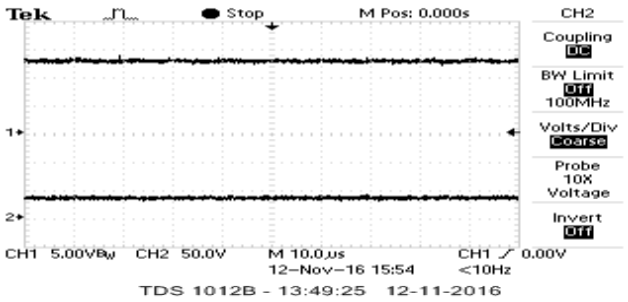


Fig.23. Drain voltage V_{DS}, drain current i_{DS} and gate source voltage V_{GS} waveform

For a 12 V input voltage the output voltage, inductor ripple current, output voltage ripple and switching waveform are shown below.



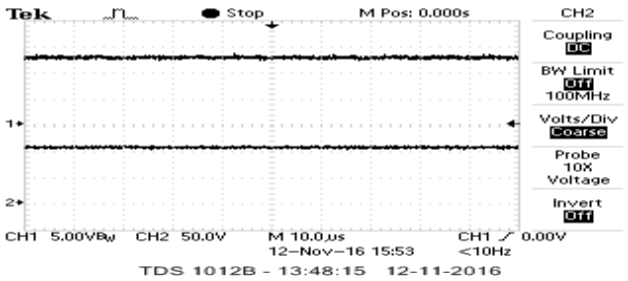


Fig 24. First stage and second stage output voltage of Superlift converter

In the captured waveform channel 1 represents the input voltage and channel 2 represents the first stage and second stage output. Stage 1 output is approximately equal to 35 V and stage 2 output is equal to 106 V. Inductor ripple current is captured and shown in Figure 25.

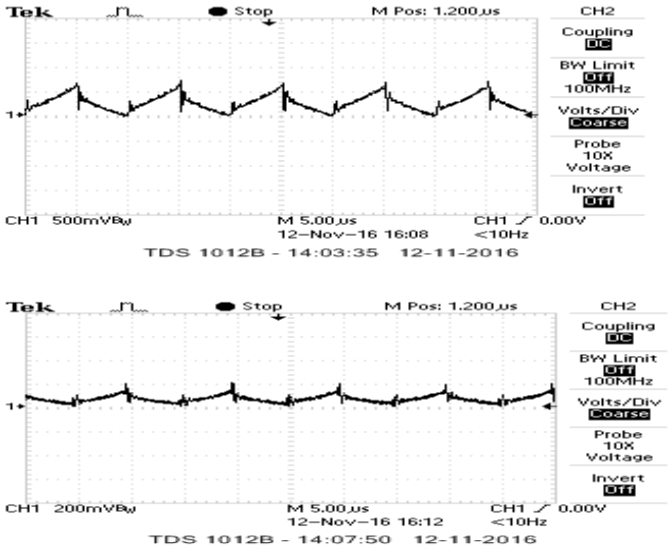
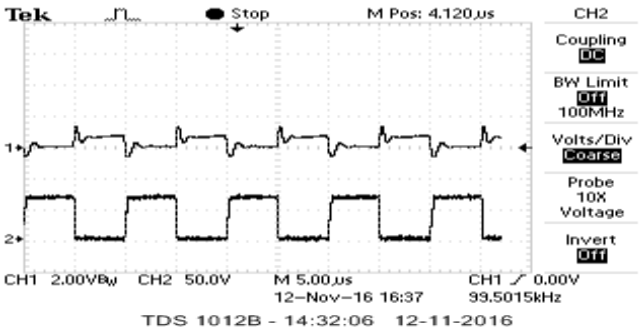


Fig. 25. Inductor L1 and L2 ripple current.

Peak to peak inductor ripple current Δ_{iL1} is equal to 0.70 A and ripple current Δ_{iL2} is equal to 0.18 A. Switching instant and gate voltage waveform are shown in Figure 26.



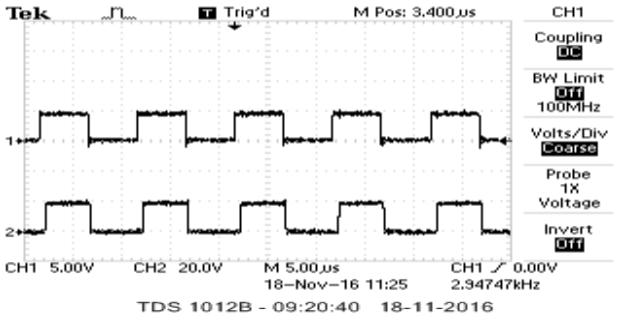


Fig.26. Drain voltage V_{DS}, drain current i_{DS} and gate source voltage V_{GS} waveform.

From the observed waveform channel 1 represents the drain current equal to 0.8 A and channel 2 represents the drain source voltage equal to 75 V. Pulse waveform from the driver circuit is captured and shown in Figure 26. With turn on time of 5 µs, total time period of 10 µs and positive amplitude equal to 20 V. Channel 1 represents gate pulse generated from dsPIC microcontroller and channel 2 represents the driver output. For a variation of 5 V in input, first stage and second stage output voltage for Si IGBT based two stages super lift is shown in Figure 27.

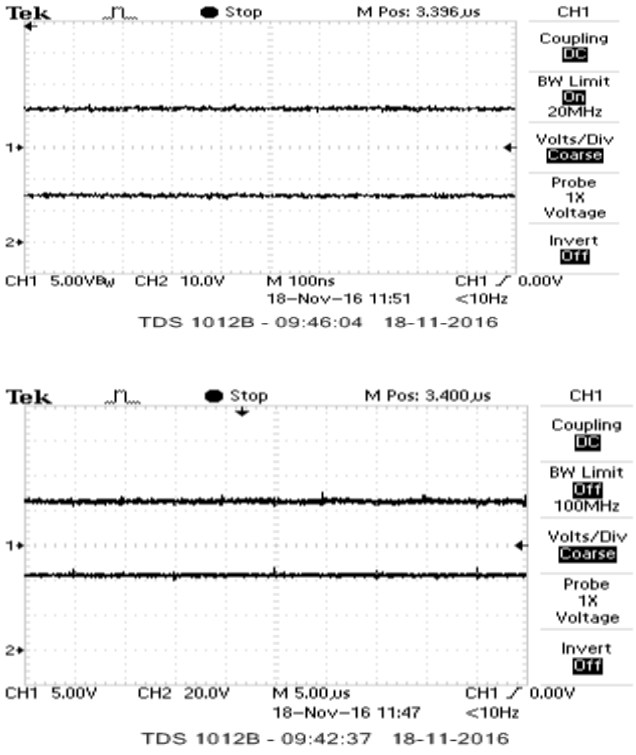


Fig. 27.First stage and second stage output voltage of Si IGBT based superlift converter

From Figure .27, it is observed that the output voltage for stage 1 is approximately equal to 14.5 V and stage 2 is equal to 42 V. Inductor current is captured and shown in Figure 28.

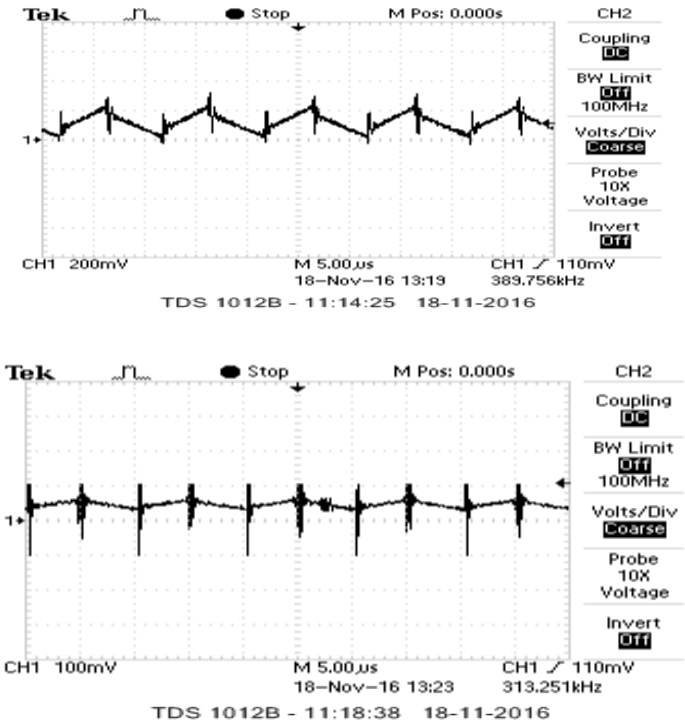
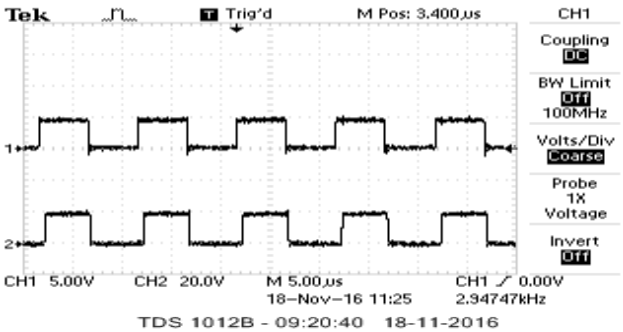


Fig.28. Inductor L1 and L2 ripple current.

From the captured waveform it is observed that during switching transition there is some high frequency noise signals gets superimposed to the current waveform, excluding the noises the inductor L_1 peak to peak ripple current is equal to 220 mA and inductor L_2 peak to peak ripple current is equal to 60 mA. Switching transition waveforms such as collector emitter voltage, collector current and gate emitter voltage is shown in Figure 29.



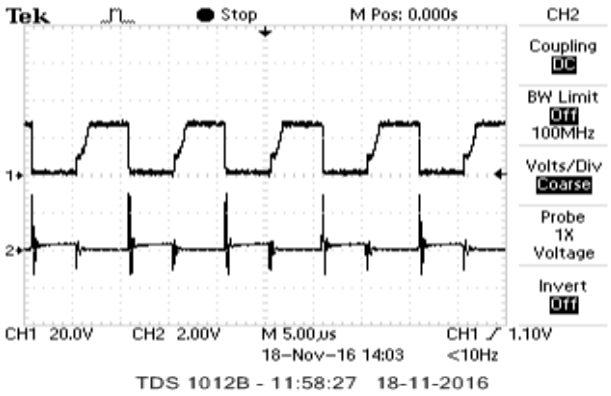


Fig. 29. Switching Transition waveform

Channel 1 in Figure 29 represents the collector emitter voltage V_{CE} and it is equal to 28 V and channel 2 is collector current equal to 400 mA with gate emitter voltage of 20 V magnitude and 100 kHz switching frequency. Experimental test result for SiC MOSFET based two stage Superlift converter is shown in table 13.

Table 13. Experimental test results for SiC Converter

Case No	Input voltage (V)	Output voltage (V)	Output Power (W)	Loss (W)	Efficiency %
1	5	42	3.753	0.738	83.56
2	10	88.82	16.78	1.813	90.24
3	12	106	23.79	2.251	91.35

Experimental test result for Si IGBT based two stage Superlift converter is shown in table 14, for three test cases with variation in input voltage, constant switching frequency and load.

Table 14. Experimental test results for Si Converter

Case No	Input voltage (V)	Output voltage (V)	Output Power (W)	Loss (W)	Efficiency %
1	5	42	3.753	1.714	68.64
2	10	87.85	16.42	4.25	79.43
3	12	104	23.01	3.57	86.56

10. Conclusion

A POSLLC based on SiC MOSFET was designed, simulated and implemented. Basic characterization of the SiC MOSFET was done to study the superiority of the device. Resistance and inductance switching is performed to study the dynamics of the device under pulsed condition, study reveals that turn off time of the device is less, when compared to the Si device of same rating. Ripple analysis is performed with variation in switching frequency. At 500 kHz, ripple present in the output voltage is less than 1%. POSLLC converter voltage gain is derived with inclusion of parasitic in active and passive components. Experimental test case is formed to validate the simulation results. Efficiency of the proposed SiC based converter is high compared to the Si based converter of same rating. Therefore employing a SiC based device in the high voltage gain converter topology will be a promising one in applications like renewable energy studies, PEV'S and power generation systems.

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