APPLICATION OF SUPERCAPACITOR IN ENHANCING POWER QUALITY OF UPQC FOR A THREE PHASE BALANCED/UNBALANCED LOADS

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Abstract - This paper introduces the integration of unified power quality conditioner with the supercapacitor for improving the power quality at the supply mains. This work described the unified power quality conditioner principles and power restoration for balanced or unbalanced voltage sags or swells in a distribution system. This method proposes a typical configuration of unified power quality conditioner for compensating sag or swells conditions for three phase system that consists of a DC/DC converter supplied by a supercapacitor at the DC link. A suitable series-shunt controller is employed for controlling the unified power quality conditioner under balanced or unbalanced load currents is also presented. The operation of the proposed system is modeled and simulated in MATLAB environment using Simulink and Simpower System toolboxes.

Key words — Power quality, unified power quality conditioner (UPQC), supercapacitor, DC/DC converter, third harmonic distortion (THD), phase locked loop (PLL), synchronous reference frame (SRF)

1. Introduction

The modern equipment's that are used in home are very sensitive and prone to harmonics as well as voltage disturbances with poor power factor. The power quality problem is also due to the different faults conditions occurring on the power system network. These conditions cause voltage sag or swell in the system and malfunctioning of devices which damages the sensitive loads. The mitigation of these on the source and load sides is most important for improving the reliability as well as performance on the system. Unified Power Quality Conditioner (UPQC) is expected to be one of the most powerful solutions to large capacity loads that are sensitive to the changes in supply voltage, flicker or imbalance. The UPQC has a single topology that combines series active power filter and shunt active power filter with a common DC link. These two are connected in a back to back configuration. Shunt active power filter compensates all current related distortions and series active power filter compensates all voltage related distortions. The compensation can be done effectively, if there is an effective DC link. The operation of both series

active power filter and shunt active power filter are based on voltage source converter technique. The shunt compensator takes care of reactive power compensation, current harmonic compensation, load unbalance compensation and power factor improvement. The series compensator acts for voltage harmonics, voltage sag or swells, flickering etc., with the harmonic isolation between load and supply. The supercapacitor is used as a battery storage device across the DC link for short time duration.

The energy can be stored in the form of batteries, flywheels, compressed air, hydraulic systems and super conducting energy storage systems [1]. A configuration with STATCOM-supercapacitor energy storage system is used to enhance power system stability and quality [2]. Supercapacitors are also find applications in metro vehicles and hybrid electric vehicles [3], also in traction [4]. The battery has a high storage capacity but unreliable and flywheels requires a lot of maintenance. The discharge rate is slower in batteries because of slower chemical process. But now the future is turned to higher rate of charging and discharging the energy which is possible with the supercapacitors. The supercapacitors stores less energy however the power transfer capability is high compared to the conventional batteries. The rate of discharge while compensation is fast and it takes only a small current for charging [1]. Use of supercapacitor is proposed in UPQC scheme as it is characterized by less weight, faster charge/discharge cycle time, higher power density, higher efficiency and almost maintenance free.

The paper [5] explains the power circuit modeled as a 3-phase 3-wire system with a non-linear load that is composed of 3- phase diode-bridge rectifier with RC load in the DC side. The Third Harmonic Distortion (THD) of more than 40% is observed. In paper [6] described the application of Bi-directional full bridge DC-DC converters in UPQC. In the papers [7]-[9] concentrated only on voltage sag or swell utilizing the series inverter. The most important parameters of a supercapacitor include the capacitance(C), equivalent series resistance and equivalent parallel resistance which is also called leakage resistance [10]-[15]. UPQC is a custom power device and consists of combined series active power filter compensates voltage harmonics, voltage sag, voltage swell, flicker etc. and shunt active power filter compensates current related problems such as reactive power compensation, reactive power compensation and power factor improvement etc. [16]-[17]. In all the operating conditions the THD of source current has been observed within an IEEE 519-1992 standard limit of 5% [18]. Using UPQC how to minimize the power losses and improve voltage profile to determine the best location and the size of UPQC while the load constraints, network constraints and operational constraints are satisfied and compensation of harmonics [19]-[20].

This Integrated unit is developed to enhance the capability of the UPQC and to maintain a high quality voltage, current and power factor at the point of common coupling. This paper concentrates on both series and shunt inverters functioning on voltage related issues like sag, swell and flickering etc. and reduction of harmonics and reactive power control.

This paper suggests a new form of UPQC, DC/DC converter and energy storage system. The operation of the intended system was observed through MATLAB environment using Simulink and Simpower System toolboxes. This paper is organized as: Section 2; describes the supercapacitor based UPQC. Section 3; deals with the control scheme of series and shunt converter. Section 4; presents the supercapacitor energy storage system design. Section 5; presents the operation of DC-DC converter. Sections 6; presents the results and discussions. Sections 7; presents the conclusion. Sections 8; presents the appendix.

2. Supercapacitor based UPQC

The block diagram representation for the proposed system is shown in Fig 1. The dc link of both of these active filters is connected to a supercapacitor through a common dc link capacitor. The three-leg voltage source inverter based shunt active filter is capable of suppressing the harmonics in the source currents, load balancing and power factor correction. The series filter is connected between the supply and load terminals using a three phase transformer. The main aim of the series active power filter is to obtain harmonic isolation between the load and supply. In addition to injecting the voltage, these transformers are also used to filter the switching ripple content in the series active filter. A small capacity rated R-C filter is connected in parallel with the secondary of each series transformer to eliminate the high switching ripple content in the series active filter injected voltage. The voltage source inverters for both the series and shunt active power filters are implemented with insulated

gate bipolar transistors. The load under consideration is a combination of linear and non-linear type.

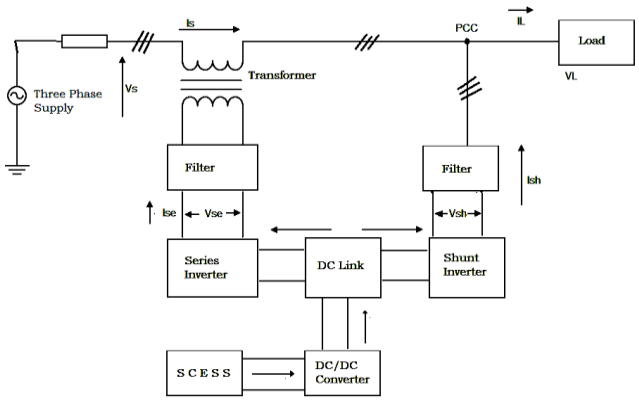


Fig 1. Proposed Block Diagram of UPQC with Supercapacitor

The supercapacitor bank consists of number of series and parallel capacitors to increase the current and voltage at the DC link and the DC/DC converter is used to maintain constant voltage at the DC link irrespective of the voltage at the supercapacitor bank. It boosts the voltage level when sag appears in the line, and consumes energy when there is a swell in the line. UPQC can be utilized to solve power quality problems simultaneously [9]. Proposed method is

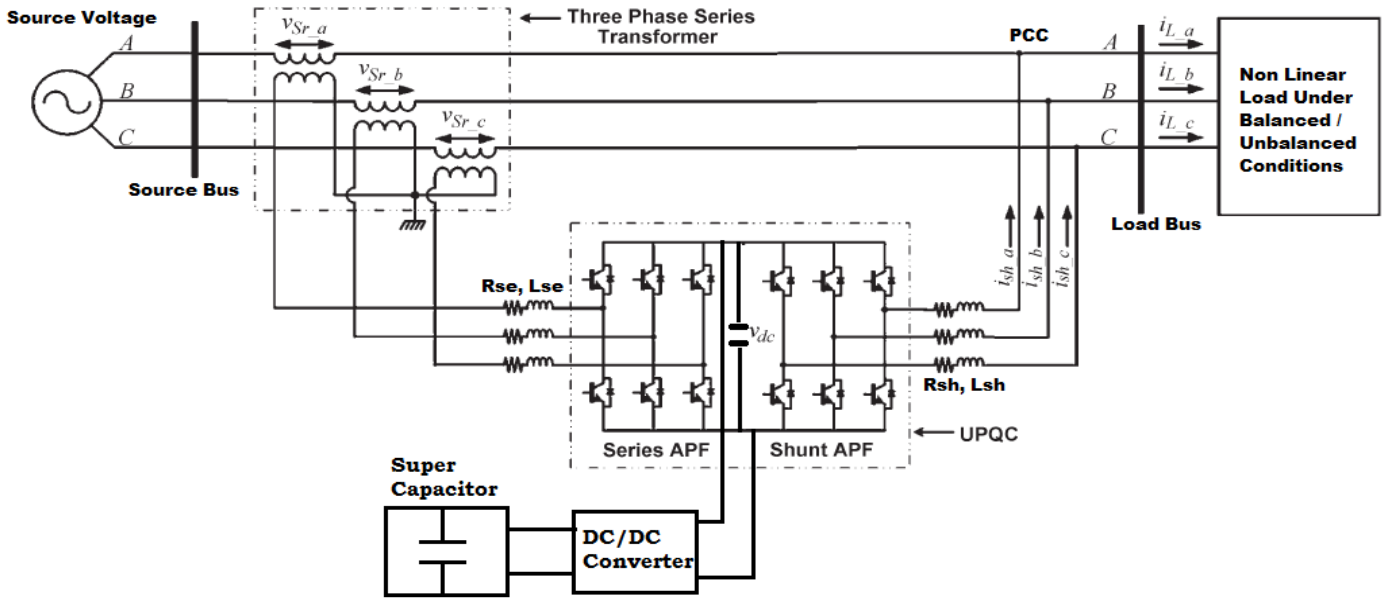


Fig 2. Circuit Diagram of Enhanced UPQC.

about the usage of supercapacitor instead of a conventional energy storage for a UPQC. The UPQC for harmonic elimination and simultaneous compensation of voltage and current, which improve the power quality, offered for other harmonic sensitive loads at the point of common coupling. UPQC has the capability of voltage imbalance compensation as well as voltage regulation and harmonic compensation at the consumer end. The shunt active power filter is used to absorb current harmonics and to regulate the dc-link voltage between both active power filters. The UPQC, therefore, is expected to be one of the most powerful solutions to large-capacity loads sensitive to supply-voltage-imbalance distortions. In this paper, the proposed synchronous-reference frame based control method for the UPQC system with a DC/DC converter to control voltage at the supercapacitor end is used and the system performance is improved. In the proposed control method, load voltage, source voltage, and source current are measured, evaluated,

and tested under unbalanced and distorted load conditions using MATLAB/Simulink software. The values of the circuit parameters and the loads under consideration are given in the Appendix.

3. Control Scheme of Series and Shunt Converter

i. Control Scheme for Series Converter

The role of the proposed series converter is to eliminate harmonics and to provide reactive power requirement of the load so that ac source feeds only active component of unity power factor current. Since this series converter is connected in series with load, it improves the system efficiency. The proposed control strategy works by sensing the load voltage and compared with the reference voltage. Then the error is supplied to the controller for switching the inverter and to supply the required voltage by the series active power filter, thus making the voltage at point of common coupling a pure sinusoidal with a desired amplitude as shown in Fig 2.

Therefore, the sum of the supply voltage and the injected series voltage makes the desired load voltage. Fig. 3 shows the block diagram of control scheme for the series active power filter system for phase A. DC bus voltage, supply voltage and current are sensed to generate pulses for the series converter. AC source supplies fundamental active power of load current and a fundamental current to maintain the dc bus voltage to a constant value. The sensed dc bus voltage of the active power filter along with its reference value is processed in the proportional-integral voltage controller.

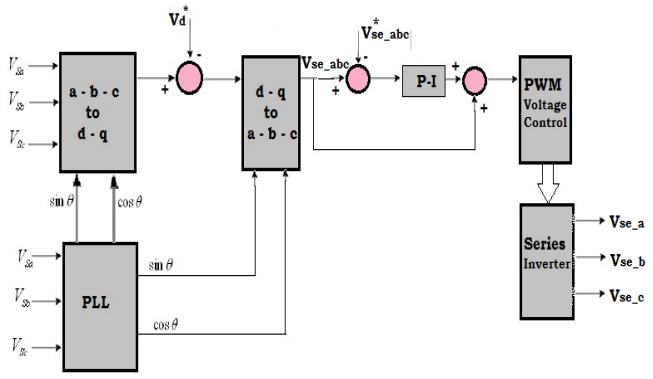


Fig 3. Control Scheme for Series Active Power Filter

A proportional-integral controller is used to regulate the dc bus capacitor voltage of the series active power filter.

$$V_e(n) = V_r(n) - V(n) \quad (1)$$

The output of proportional-integral Controller is

$$V_o(n)=V_o(n-1)+K_p\{V_{e(n)}-V_{e(n-1)}\}+K_iV_{e(n)} \quad (2)$$

Where K_p and K_i are proportional and integral constants.

The output of the proportional-integral controller is taken as peak of source current. A unit vector in phase with the source voltage-e is derived using its sensed value. The peak source current is multiplied with the unit vector to generate a reference sinusoidal unity power factor source current. The reference source current and sensed source current are processed in hysteresis current controller to derive gating signals for the switches of the series active power filter.

In response to these gating pulses, the active power filter impresses a pulse width modulation voltage to flow a current through filter inductor to meet the harmonic and reactive components of the load current.

ii. Control Scheme for Shunt Converter

The synchronous reference frame based control method presents excellent characteristics but it requires decisive PLL techniques. The shunt active filter shown in Fig.1 is a current controlled voltage source inverter, which is connected in parallel with the load. It is controlled in such a way to generate the required reactive and harmonic currents of the load. Hence, the utility needs to supply only the active part of the fundamental component of the load current. Control algorithm computes the reference for the compensation current to be injected by the shunt active filter. The choice of the control algorithm therefore decides the accuracy and response time of the filter. The calculation steps involved in the control technique have to be minimal to make the control circuit compact. The control strategy has an objective to guarantee balanced and sinusoidal source current at unity power factor. This objective can be easily realized if the active part of the fundamental component of the load current is accurately and instantaneously determined.

The hysteresis current control scheme decides the switching pattern of active filter in such a way to maintain the actual injected current of the filter to remain within a desired hysteresis band.

The switching logic is formulated as follows:

If i_{inj} < (iref − HB) S1, S2 ON & S3, S4 OFF

If i_{inj} > (iref + HB) S1, S2 OFF & S3, S4 ON

The switching frequency of the hysteresis current control method described above depends on how fast the current changes from upper limit to lower limit of the hysteresis band, or vice versa. Therefore the switching frequency does not remain constant throughout the switching operation, but

varies along with the current waveform. Furthermore, the filter inductance value of the active filter is the main parameter determining the rate of change of active filter current.

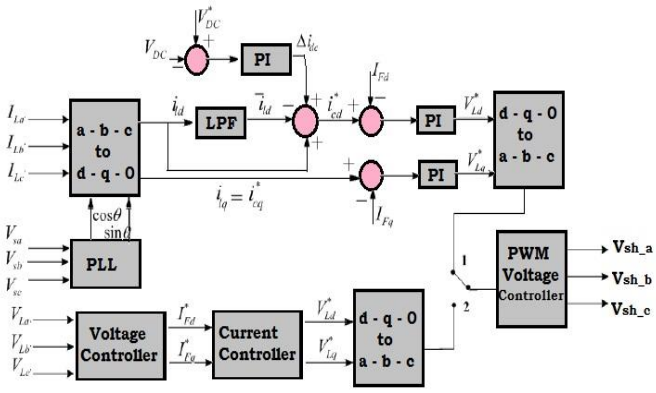


Fig 4. Proposed block diagram of SRF control

Synchronous reference frame (SRF) control is the method used conventionally with excellent characteristics and it uses a-b-c to d-q-0 transformation technique with a PLL. The load currents I_{La}, I_{Lb}, I_{Lc} are transformed to d-q-0 components using park's transformations [21]-[24] as per the equation shown below:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos(\theta-\frac{2\Pi}{3}) & -\sin(\theta-\frac{2\Pi}{3}) & \frac{1}{2} \\ \cos(\theta+\frac{2\Pi}{3}) & \sin(\theta+\frac{2\Pi}{3}) & \frac{1}{2} \end{bmatrix} \quad (3)$$

After calculating the d-q-0 component of the load currents , the d-component is passed through a low pass filter to extract dc component. A non-dc component is seperated from the reference signal. In the proposed control algorithm the sensed currents are compared with the reference currents in a hysteresis current controller to generate switching pulses for the shunt active power filter.

4. Supercapacitor Energy Storage System Design

Supercapacitors are the latest inventions in the field of energy storage systems. Usually supercapacitors are divided into two types: double-layer capacitors and electrochemical capacitors. The former depends on the mechanism of double layers, which is result of the separation of charges at interface between the electrode surface of active carbon or carbon fiber and electrolytic solution. Its capacitance is proportional to the specific surface areas of electrode material. The latter depends on fast faraday redox reaction. The capacitors can work at high voltage without connecting many cells in series.

The size of supercapacitors is determined from the size of load connected and the duration of voltage interruption. Therefore, total energy to be released during the voltage interruption is 30kJ. The maximum current flows through the supercapacitor bank, when it discharges the maximum power. The minimum voltage across the supercapacitor bank can be determined with the maximum discharge power and the current rating as the following [25].

$$U_{bank\_\min} = 20kW / 360A = 55.5V \quad (4)$$

It is assumed that the supercapacitor is charged by 2.43V, which is 90% to the maximum charging voltage of 2.7V, for consideration of 10% margin.

The Stern-tafel Equation can be expressed as:

$$-i_C(t) = Ai_0 \exp\left(\frac{\alpha F\left(\frac{V}{N_S} - \frac{V_{Max}}{N_S} - \Delta V\right)}{RT}\right)N \quad (5)$$

$$V = \frac{NN_S Qx_2}{N_P N^2 \in\in_0 A} + \frac{NN_S 2RT}{F}\alpha r \sinh\left(\frac{Q}{N_P N^2 A\sqrt{8RT \in\in_0 c}}\right) \quad (6)$$

The state of charge (SOC) for a fully charged supercapacitor is 100% and for an empty it is 0%.

The SOC is calculated as

$$SOC = \frac{Q_{init} - \int_0^t i(\tau)d\tau}{Q_T} \times 100 \quad (7)$$

The lowest discharged voltage is determined to be 2.1V using the following,

$$\text{Uunit\_min} = \sqrt{\frac{3}{4}}\,\text{Uunit\_max} = 2.1\text{V} \quad (8)$$

Therefore, the lowest discharge voltage and the minimum unit voltage determine the number of units to be connected in series as the following.

$$\text{N} = \frac{\text{Ubank\_min}}{\text{Uunit\_min}} = \frac{55.5}{2.1} = 26.5 \quad (9)$$

However, the bank can be designed using total 28 units of supercapacitors.

5. Operation of DC-DC Converter

The proposed DC/DC converter can operate in bi-directional mode. The converter has a wide voltage conversion range with simple control. The operation voltage of the supercapacitor bank is in the range between 60-75V, while the dc link voltage is about 700V. The converter should have high current rating at the bank side and high voltage rating at the DC link side. A DC/DC converter with two full-bridges is shown in below Fig.5.

In paper [6] described the application of Bi-directional full bridge DC-DC converters in UPQC using phase shifted control theory and analyzed in an isolated manner and this performance is to be implemented in an application. A filter reactor is inserted between the bank and the full-bridge to reduce the ripple of charging and discharging current. The full-bridge in bank side is as a current-fed converter and the full-bridge in DC link side works as voltage-fed converter. The DC/DC converter boosts the supercapacitor voltage up to the nominal DC link voltage in discharge mode. The supercapacitor voltage is controlled between 60-75V, while the DC link voltage increases up to 700V. The switches SC1 and SC2 operate with a duty ratio of higher than 0.5.

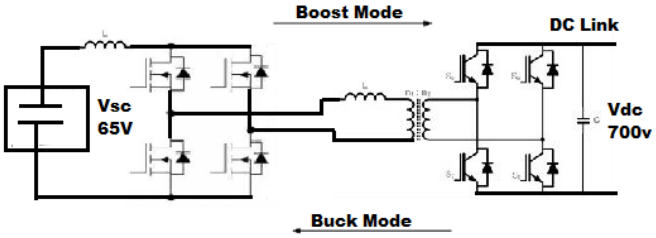


Fig. 5 DC-DC Converter

The current through transformer rises linearly and its peak value becomes larger than the current through the boost inductor. When the auxiliary switch is turned off then the magnetic energy stored in the leakage inductance of the transformer flows through the diode. So, the zero-voltage turn-on condition is provided. The DC/DC converter decreases the nominal DC-link voltage down to the level of supercapacitor voltage in charge mode.

The power in the primary side is transferred to the secondary side. The secondary voltage charges the capacitor through the reverse-connected diode of auxiliary switch S_a. If the charging voltage is high enough to make the charging current zero, switch S_{b1} turns off. Switch S_{b3} turns on with zero-voltage scheme while the capacitor C_1 is charged and the capacitor C_3 is discharged. When auxiliary S_a turns on, the voltage across the auxiliary capacitor affects the primary voltage of the coupling transformer. This voltage is applied to the leakage inductance L_{Lk} with reverse polarity. This makes the primary current zero and switch S_{b2} turns off with zero-current scheme.

6. Results and Discussions

The Fig.6 shows the Simulink diagram of the proposed system. The performance of the UPQC with supercapacitor for different supply disturbances is tested under various operating conditions. The proposed integrated supercapacitor - UPQC system is tested for different power quality events like voltage-sag, voltage swell, load balancing, harmonic compensation and power factor correction. The proposed system with the control algorithm is able to mitigate the above mentioned power quality problems successfully. Fig.7 shows the results for all the above mentioned power quality problems.

(a) Sag-Swell Compensation

A balanced sag of 50% in the source voltage (Vs) is introduced during 0.3 sec to 0.38 sec as shown in Fig.8(a) The supply voltage (V_S), Load Voltage (V_L), Voltage injected ($V_{\_inj}$), Load current (I_{Labc}), Source current (I_{sabc}) and shunt compensation current ($I_{\_Comp}$) are shown in the Fig.8(a). The RMS value of per phase injected voltage ($V_{\_inj}$), Supply voltage (V_S), Load voltage (V_L) are shown in the Fig. 8(b). Here the supercapacitor is supplying the required compensation power through the series compensator and it can be observed that the load voltage is almost maintained constant. Similarly a balanced swell of 50% is applied during 0.5sec to 0.58sec and the corresponding compensation voltage and the instantaneous waveforms of voltage (V_S), Load Voltage (V_L), Voltage injected ($V_{\_inj}$), Load current (I_{Labc}), Source current (I_{sabc}) and shunt compensation current ($I_{\_Comp}$) are shown in the Fig.9 (a) & (b).

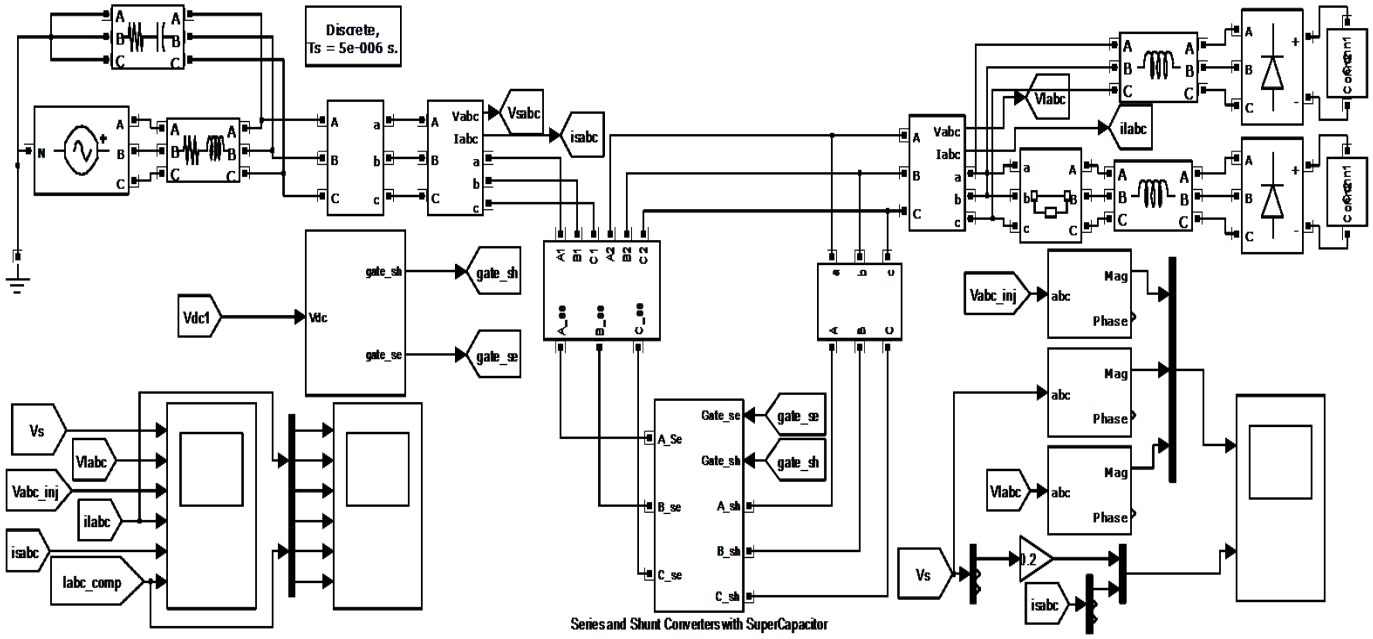
(b) Load Compensation

The performance of integrated supercapacitor - UPQC for load balancing is shown in Fig.10 where the load is unbalanced. An unbalance in the load is introduced by opening one of the phase of connected load during 0.7sec to

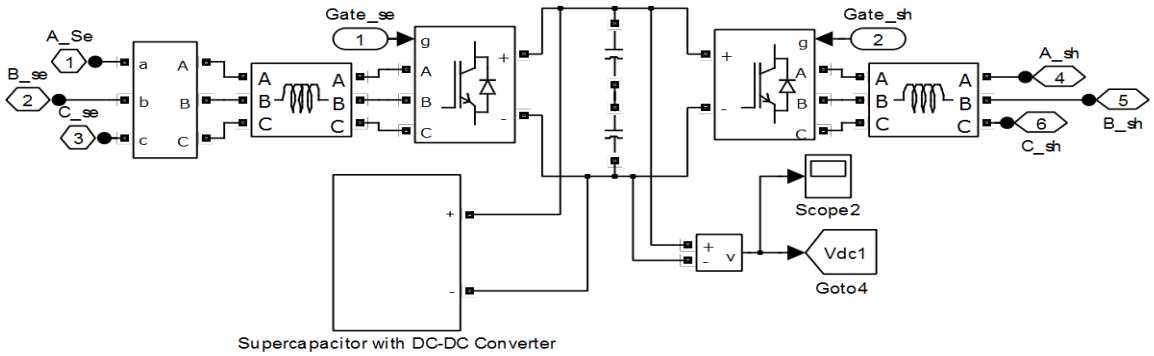
0.8sec Fig.10 shows the waveform of voltage (V_S), Load Voltage (V_L), Voltage injected ($V_{\_inj}$), Load current (I_{Labc}), Source current (I_{sabc}) and shunt compensation current ($I_{\_Comp}$). These results show satisfactory performance of the proposed integrated supercapacitor - UPQC system along with the control algorithm used

(c) harmonic Compensation and power factor correction

Fig. 11(a)–(d) shows the harmonic spectra of load current, source current, source voltage and the load voltage. From Fig.11 (a) & (b) it can be observed that the total harmonic distortion of the phase 'b' of load current is 29.85% and the source current has the THD of 3.32%. From Fig.11 (c) & (d) the THD of the source voltage and load voltage are 2.11% and 1.85%. The power factor at source terminal is improved to unity after compensation of reactive power which is shown in Fig.12.



(a)



(b)

Fig 6. (a) Simulink Diagram of the Proposed System (b) Simulink Diagram of the SC-with DC-DC converter connected at DC Bus of back to back connected series and shunt converters.

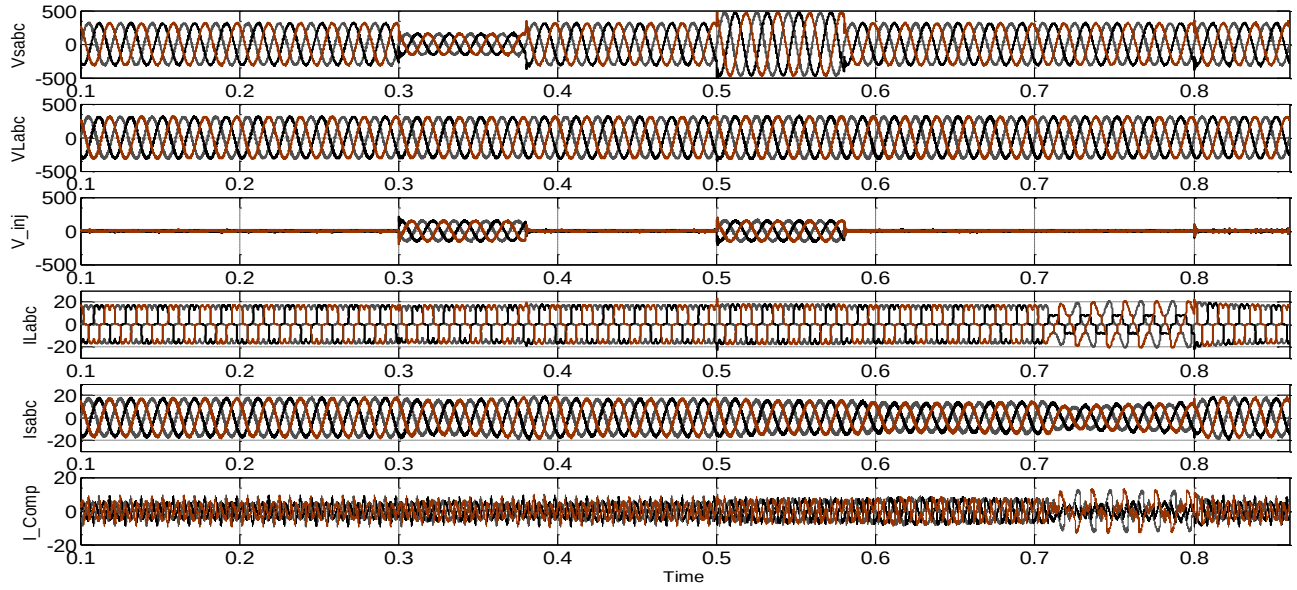
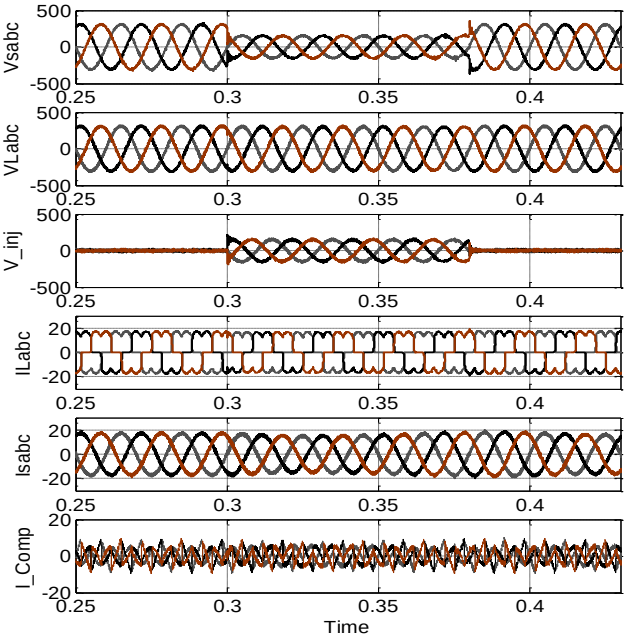
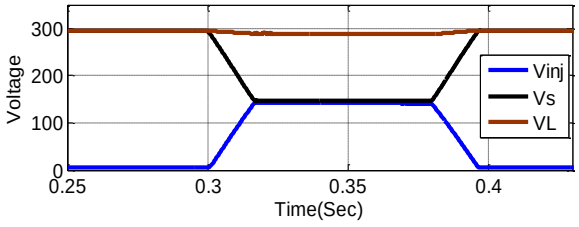


Fig 7. Results showing sag-swell in the source voltage and the unbalance in the load current.

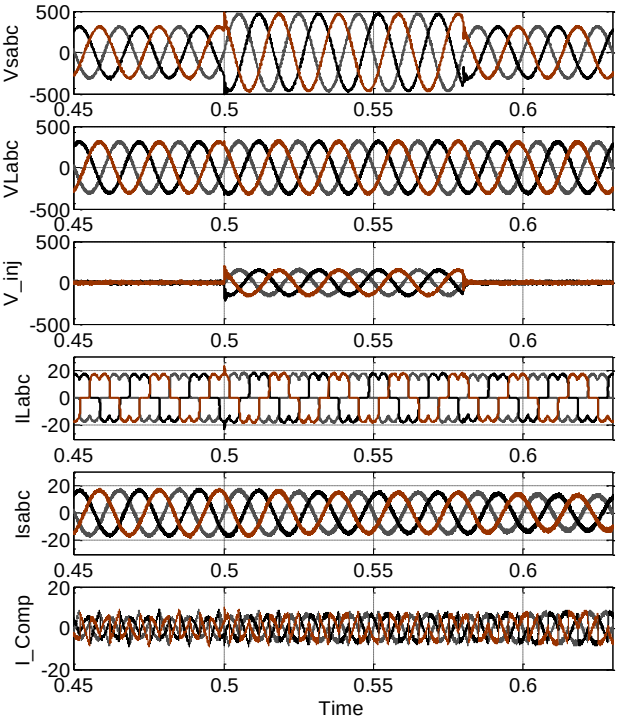


(a)



(b)

Fig 8. (a) Results showing V_{sabc}, V_{Labc}, $V_{\_inj}$, I_{Labc}, I_{sabc}, $I_{\_Comp}$ During sag condition (b) Result showing the magnitude of per-phase Source Voltage –Vs (Black), Load Voltage-VL (Red) and Injected Voltage-Vinj (Blue)



(a)

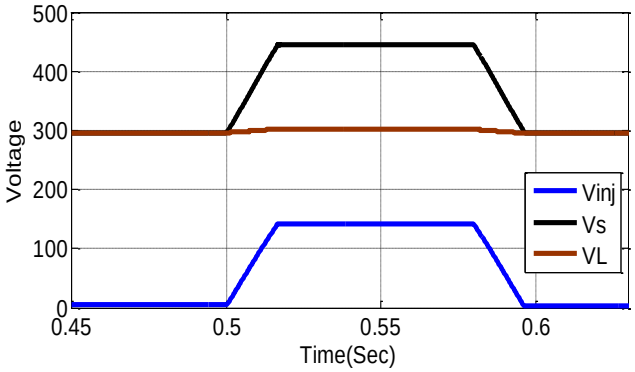


Fig 9. (a) Results showing V_{sabc}, V_{Labc}, V_inj, I_{Labc}, Isabc, I_Comp During swell condition (b) Result showing the magnitude of per-phase Source Voltage –Vs (Black), Load Voltage-VL (Red) and Injected Voltage-Vinj (Blue)

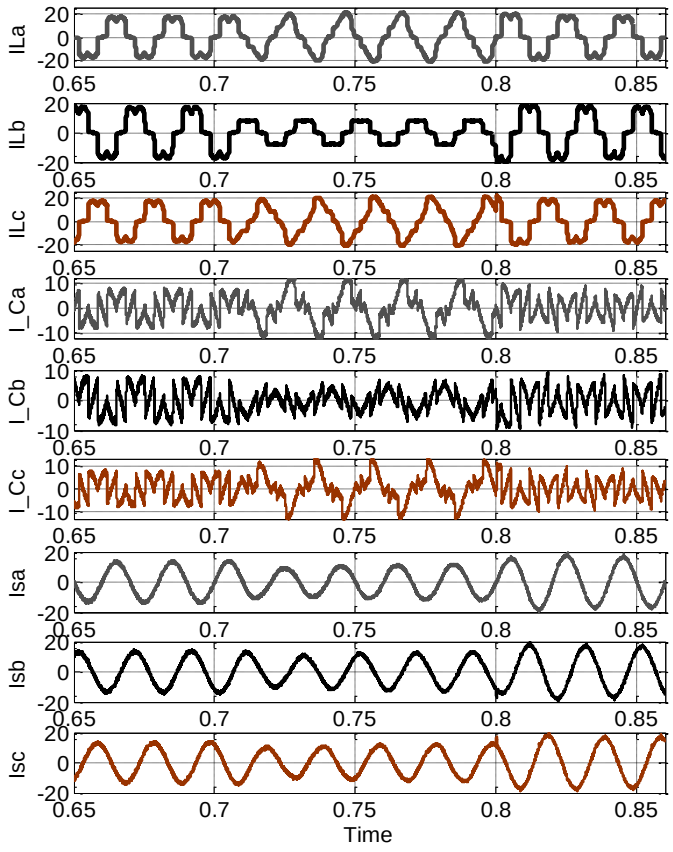
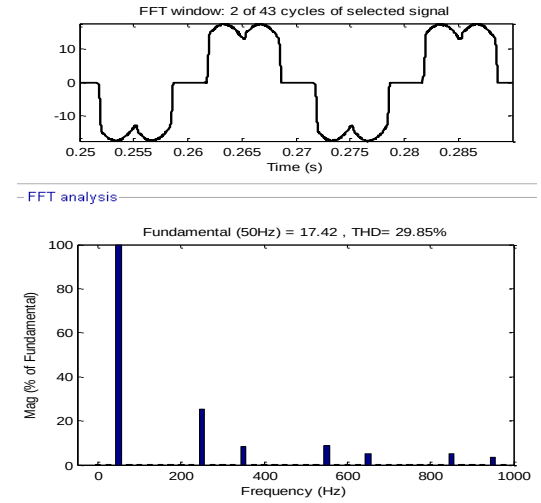
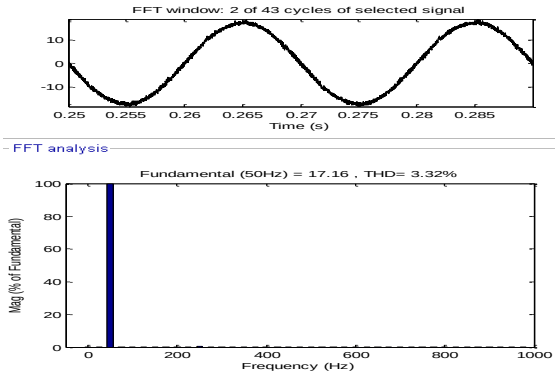


Fig 10. Results showing the load and harmonic compensation



(a)



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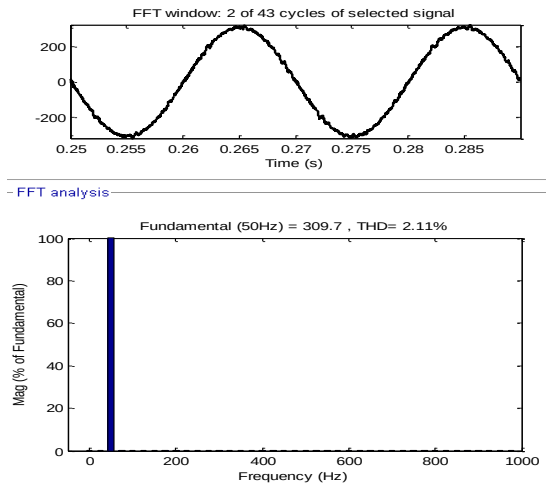
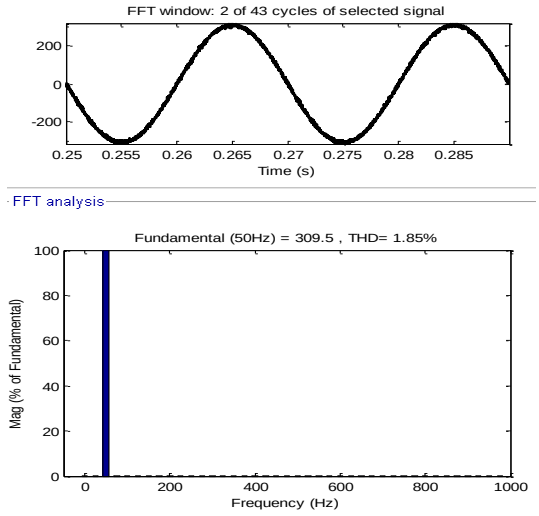


(c)



(d)

Fig 11. a) Load Currents %THD b) Source Currents %THD c) Source Voltage %THD d) Load Voltage %THD

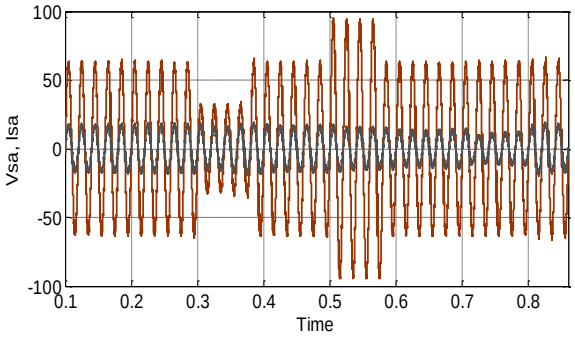


Fig 12. Results showing the power factor correction.

TABLE I
PERFORMANCE OF UPQC WITH SUPERCAPACITOR

Control Method	Parameter	Magnitude Voltage and Current per phase (Vrms & Irms)	%THD
UPQC with Supercapacitor	Source Voltage (V_{Sabc_rms})	220V	2.11%
	Load Voltage (V_{Labc_rms})	219.23 V	1.85%
	Source Current (A) i_{Sabc_rms}	12.13 A	3.32%
	Load Current (A) i_{Labc_rms}	12.31 A	29.85%

7. Conclusion

This paper proposes a new configuration of UPQC that consists of the DC/DC converter and the supercapacitor. The proposed UPQC compensated the reactive power, harmonic currents, voltage sag and swell, voltage unbalance, and the voltage interruption. In all the operating conditions the THD of source current has been observed within an IEEE 519-1992 standard limit of 5%. The operation of proposed system was demonstrated through simulation with MATLAB/SIMULINK software. The proposed UPQC has the ultimate capability of improving the power quality at the installation point in the distribution system.

8. Appendix

V_s = 440V, f = 50Hz, R_L = 10, L_L = 25mH, C_{dc} = 4700uF, V_{dc} = 700V, R_s = 0.01, L_s = 50uH, L_{sh} = 8mH, L_{se} = 2.5mH.

Supercapacitor Ratings: Crated = 1000F, R_{se} = 2.1mohms, V_{rated} = 65V, Surge Voltage = 75V, N_s = 28, N_p = 1,

Initial Voltage = 60V, leakage Current = 5.2mA, Temperature = 25 C

Stern-Tafel Parameters:

N = 6, r = $1.23*10^{-9}$, ΔV = 0.3V, α = 0.3, Charge Current=100A.

References

1. S. C. Smith, and P. K. Sen, B. Kroposki, "Advancement of energy storage devices and applications in electrical power system", *IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century* , 2008, pp.1-8.

2. P. Srithorn, M. Sumner, and L. Yao, R. Parashar, "A STATCOM with Super-Capacitors for enhanced power system stability" *4th IET Conference on Power Electronics, Machines and Drives* , 2008 , pp.96-100.

3. ZHANG Yi-cheng, WU. Lu-lu, ZHU Xue-jun, and LIANG Hai-quan, "Design of Super-Capacitor-based Energy Storage System for Metro Vehicles and Its Control Rapid Implementation" *IEEE Vehicle Power and Propulsion Conference*, Harbin, 2008, pp 1-4.

4. W. Lhomme, P. Delarue, P. Barrade, A. Bouscayrol, A. Rufer, " Design and Control of a SupercapacitorDesign Storage System for Traction Applications", *Industry applications conference*, 2005, Vol. 3, pp 2013 – 2020.

5. M.Siahi, M.Hoseynpoor, M.Najafi,, R. Ebrahimi "Design and Simulation of UPQC with Supercapacitorto Energy Storage and Improve Power Quality", *Australian Journal of Basic and Applied Sciences*, 5(3): 674-681, 2011.

6. Yang Zhang, Shengfa Zhang, Jiahong Chen "The Applications of Bidirectional Full-bridge DC-DC Isolated Converter in UPQC", Electrical Machines and Systems, 2008. ICEMS 2008, Wuhan, Oct. 2008, pp1916 – 1921.

7. Malabika Basu S. P. Das Gopal K. Dubey "Performance Study of UPQC-Q for Load Compensation and Voltage Sag Mitigation", *IEEE Conf*erence 2002, vol.1, pp 698 – 703.

8. Maurício Aredes and Rodrigo M. Fernandes "A Unified power quality conditioner with voltage sag/swell Compensation capability", *IEEE conference*, 2009, pp 218 - 224.

9. Vinod Khadkikar, *Member, IEEE*, and Ambrish Chandra, *Senior Member, IEEE* "UPQC-S: A Novel Concept of Simultaneous Voltage Sag/Swell and Load Reactive Power Compensations Utilizing Series Inverter of UPQC", *IEEE transactions on power electronics*, vol. 26, no. 9, September 2011.

10. P.B.Karandikar, D.B.Talange, Uday Mhaskar, Ramesh Bansal, "Development, characterization and modelling of aqueous metal oxide based Super-Capacitor", *Energy, Elsevier*, April 2012, Vol 40, pp 131-138.

11. P.B.Karandikar, D.B.Talange, Uday Mhaskar, Ramesh Bansal, Materials and manufacturing processes, "Investigations in to material and manufacturing aspects of aqueous Super-Capacitor", *Taylor and Francis*, November 2012, 27 (11), pg. 1164-1170 .

12. P.B.Karandikar, D.B.Talange, Uday Mhaskar, Ramesh Bansal, 'Validation of Capacitance and ESR Model of Manganese Oxide Based Aqueous Super-Capacitor", *Electric Power Components and Systems, Taylor and Francis*, vol. 40, no. 10, 2012, pp. 1105-1118.

13. P B Karandikar, D B Talange, Amit Singh, Raju Pal, Gary Singh, AnshumanSarkar, "Regenerative braking in electric two wheeler using Super-Capacitors", *843/MUM/2011*, Filed on 2011-03-23, Publication date 2011-09-16.

14. Sandwich type Supercapacitor making process, P B Karandikar, D B Talange, A. Dekate, Atul Singh, N S Prasun, 841/MUM/2011Filed on 2011-03-23, Publication date 2011-09-16.

15. P B Karandikar, D B Talange, "Method of manufacturing electrode for Super-Capacitor", *2858/MUM/2010*, Filed on 2010-10-14, Publication date 2011-01-07.

16. V.Kadkikar, A.Chandra "A new control philosophy for unified power quality conditioner (UPQC) to coordinate load – reactive power demand between shunt and series inverters," *IEEE Transactions on power delivery*, 23,2008, 2522-2534.

17. B. M. Han, B. Bae, "Unified power quality conditioner with super capacitor energy storage", *European Trans. On Electrical Power*, 18, 2007, 327-343.

18. Shailendra Kumar Jain, Pramod Agarwal ,"Design Simulation and Experimental Investigations, on a Shunt Active Power Filter for Harmonics, and Reactive Power Compensation" *Taylor and Francis*, June 2010, pg. 671-692.

19. Mohamed BOUTEBEL, Karim MOKRANI, "OPTIMAL STEADY STATE OPERATION OF UNIFIED POWER QUALITY CONDITIONNER FOR POWER LOSSES REDUCTION AND VOLTAGE REGULATION IMPROVEMENT", Journal of Electrical Engineering, Volume 14 / 2014 - Edition : 1, pp 1-8.

20. Seyedreza Aali "Unified Power Quality Conditioner Based on Neural-Network Controller for Mitigation of Voltage and Current Source Harmonics " ,Journal of Electrical Engineering, pp 1-6.

21. R. C. Dugan, M. F. McGranaghan and H. W. Beaty, Electric Power System Quality, 2nd Edition, *McGrawHill, New York*, 2006.

22. G. T. Heydt, *Electric Power Quality*, 2nd ed. *West Lafayette*, IN: Stars in a Circle, 1994.

23. N. Mohan, T. Udeland, andW. Robbins, *Power Electronics: Converters, Applications and Design*, 2nd ed. New York: Wiley, 1995.

24. D. A. Paice, *Power Electronic Converter Harmonics-Multi-PulseMethods for Clean Power*. New York: *IEEE Press*, 1996.

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Nomenclature

$\mathbf{R_L}$ - Load Resistance
$\mathbf{L_L}$ - Load Inductance
$\mathbf{C_{dc}}$ - DC Link Capacitance
$\mathbf{V_{dc}}$ - DC Link Voltage
$\mathbf{R_s}$ - Source Resistance

L_s - Source Inductance
L_{sh} - Shunt Inductance
Lse - Series Inductance
A - Interfacial area between electrodes and electrolyte (m^2)
c - Molar concentration (mol m −3) equal to c = 0.86/(8NAr^3)
F - Faraday constant
I - Current density (Am−2)
i_f - Leakage current (A)
i_0 - Exchange current density i0 = if/A (Am−2)
k - Stefan-Boltzmann constant
N - Number of layers of electrodes
NA - Avogadro constant
Np - Number of parallel supercapacitors
Ns- Number of series supercapacitors
Q - Electric charge (C)
R - Ideal gas constant
r - Molecular radius equal x2
x2 - Helmholtz layer length (m)
α - Charge transfer coefficient, Tafel equation (0<alpha<1)
ΔV - Over potential

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