SPACE-VECTOR HYSTERESIS MODULATION FOR NEUTRAL-DIODE-CLAMPED INVERTER IN ACTIVE POWER FILTER APPLICATIONS

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***Abstract*—*A space-vector hysteresis modulation (SVHM) technique is presented in this paper for three-level neutral-point-clamped (TL-NPC) multilevel inverter for active power filter (APF) applications. The main responsibility of this modulation technique is to force the actual current to reach the reference current and, simultaneously, balance the capacitor voltages. This scheme is implemented in the stationary reference frame (SRF) to avoid interphase dependency in three-phase floated neutral point (TP-FNP) systems. The space-vector-based method permits for the efficient application of zero-voltage vectors and avoids high switching frequencies triggered by phase interaction in TPFNP systems. The approach comprises of performing two alternative hysteresis strategies around the error vector in SRF. Then, based on the present location of it, the next voltage vector is selected to minimize the next error vector and also balance the capacitor voltages. The performance of the proposed technique is investigated and verified through detailed simulation studies for both steady-state and transient conditions.*
***Index Terms*—*APF, space-vector, NPC, current control.*

1. INTRODUCTION

The fast increasing use of power-electronics equipment in recent years has increased the number of nonlinear loads that draw harmonic currents from the power system [1]. The undesired current components cause stress to the power system, generating disturbed fundamental and harmonic voltage drops in the network impedances. They may add additional losses and even excite resonances [2]. The APF is a common approach to eliminate the undesired current components by injecting equal but opposite harmonic currents [3]. Active filtering can be based on various control strategies for obtaining the compensator current reference values, working either in the frequency domain or in the time domain.

Multilevel inverters [4] are becoming an established means for developing new high-power applications that require substantial increase of both current and voltage magnitudes. The advantages of multilevel inverters have been well known since the first NPC inverter was proposed in 1981 by Nabae et al. [5]. This particular topology increases the power rating because the blocking voltage of each switch is one-half of the dc-bus voltage. Moreover, their output-voltage harmonic content is much smaller than that of two-level inverters with the same switching frequency owing to the output-voltage waveform improvements [6].

In many voltage source inverter (VSI) applications such as microgrid-connected inverters, ac motor drive systems, uninterruptible power supplies and APFs, it is essential to regulate the inverter AC output current using a closed-loop controller [7-12]. The quality of the applied current controller significantly impacts the total control system operation. Hence, over the past few decades, extensive investigation has been completed on inverter current control methods. To date, three chief classes of VSI current controllers have developed comprising predictive controllers, linear proportional–integral (PI) controllers and hysteresis current controls (HCCs) [13]. Predictive controllers are the most difficult strategies demanding the knowledge about load parameters other than extensive hardware implementation. Linear PI current controller can limit the switching frequency of the inverter and produce a well-defined harmonic content. However, parameters of PI controllers must be carefully tuned with a trade-off between maintaining system stability over the whole operation range and achieving an adequate transient response during transients. This can result in degraded transient performance, which in turn, hinders the application of PI current controller in high-demanding situations such as APFs [12]. Finally, HCC has been widely used due to its simplicity, fast-response and inherent-peak current limiting capability without requiring system parameter information. It is well known that HCC has several drawbacks [12]. The main limitation of this simple control configuration is limited cycle operation at low voltages [14] meaning that when it is applied to TPFNP systems, the lack of coordination between three-phase hysteresis comparators (referred to as "interphases dependency") and asymmetrical hysteresis-band violation will cause very high switching frequency.

In this paper, a new SVHM technique for NPC-based APFs is proposed to overcome the drawbacks of the conventional HCC by implementing it in SRF and systematic application of the zero-voltage vectors. The proposed technique is designed based on the following steps: combining three error currents into a single space-vector, constructing two alternative hysteresis strategies in SRF around the error vector tip, detecting the region and the segment in which the error vector tip is located, and selecting a suitable voltage vector to bring the error vector back within the hysteresis boundaries and, at the same time, balance the capacitor voltages. Four case studies are considered here to evaluate the performance of the proposed modulation technique when applied to TPFNP systems. Detailed simulation results reveal that the proposed technique retains not only the advantages of HCC including simple implementation, quick current control action, peak current preventive capability, but also it presents more advantages comprising, interphase independency and capacitor voltage balancing.

2. ACTIVE POWER FILTER

Fig. 1(a) shows the topology of an APF configuration. This topology is composed of a TL-NPC inverter attached to the point of common coupling (PCC) through a first-order low pass filter. APF is controlled such that it removes the load current harmonics and supplies load reactive power to accomplish harmonic-free source currents at unity power factor.

The schematic of the direct current control (DCC) technique, used in this paper, is shown in Fig. 1(b). In the steady state, the active power supplied from the power network must be equal to the required load power. However, the active power balance between the power network and the load will not be kept if any change happens to the load power. This transient will deviate the average voltage of the dc-bus voltage away from the reference voltage. Therefore, the amplitude of the source current must be adjusted in order to keep the APF operation satisfactory. The active power provided by power network is formerly altered similarly to compensate the active power supplied/received by the dc-bus capacitor and match the active power used by the load. Hence, the network current magnitude can be attained by adjusting the dc-bus voltage as shown in Fig. 2(b) [15].

3. SPACE-VECTOR HYSTERESIS CURRENT-CONTROL MODULATION

A. Three-Level Half-Bridge NPC Inverter

Fig. 1(a) shows the configuration of a TL-NPC inverter. It is assumed that the upper-leg and lower-leg capacitor voltages are identical and equal to "$V_{dc}^*/2$". In this case, the phase-to-midpoint voltage of each phase can be written as:

$$v_{xN} = g_x V_{dc}/2,\ g_x \in \{1, 0, -1\}, x \in \{a, b, c\} \tag{1}$$

Then, the phase voltages of the TL-NPC inverter are given as:

$$\begin{cases} v_a = V_{dc}/3 & g_a - g_b/2 - g_c/2 \\ v_b = V_{dc}/3 & g_b - g_a/2 - g_c/2 \\ v_c = V_{dc}/3 & g_c - g_a/2 - g_b/2 \end{cases} \tag{2}$$

The output phase voltages of the TL-NPC inverter can be transformed to a vector represented in SRF, where $\mathbf{X}(t) = x_\alpha(t) + jx_\beta$ is defined by:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3}$$

Conduction states of the inverter legs determine the inverter output voltage vector at each instant, i.e., $\vec{v}_n$. Therefore, the TL-NPC inverter output voltage includes 24 non-zero vectors, i.e., $(\vec{v}_1 - \vec{v}_6)$, $(\vec{v}_8 - \vec{v}_{13})$, $(\vec{v}_{15} - \vec{v}_{26})$ and three zero vectors, i.e., ($\vec{v}_0$, $\vec{v}_7$ or $\vec{v}_{14}$).

B. Proposed SVHM Technique

To have a correct operation, the proposed modulation technique has to produce the correct voltage vector to keep the inverter current within the hysteresis boundaries, create proper multilevel voltages and, simultaneously, balance the capacitor voltages. Fig. 2 shows the proposed switching technique of the TL-NPC inverter-based APF. As observed, it comprises of four units, a measurement unit, an error computation unit, an region and segment detection unit and a voltage vector selection unit. To produce the switching signals, the output currents initially need to be measured. This procedure is performed in the measurement unit. Then, the output currents along with the reference currents obtained from the reference current circuit are transferred to SRF. Here, the error vector can be calculated simply by subtracting the reference current from the measured current in SRF. By defining the error vector magnitude and angle, the region and segment detection unit can define the segment where the error vector resides. After this step, the proper voltage vector is selected using the voltage vector selection unit. As mentioned earlier, apart from keeping the error vector within the hysteresis boundaries and produce correct multilevel voltages, the proposed technique must be able to balance the capacitor voltages as well. To do this, two alternative hysteresis strategies have been taken into account as shown in Figs. 3(a) and 3(b). The first strategy is designed with the purpose of utilizing the medium- and large-voltage vectors (shown in Fig. 3(c)) to keep the error vector within the hysteresis boundaries, while the second one is developed according to the small-voltage vectors (shown in Fig. 3(c)) to balance the capacitor voltages. It is to be noted that this modulation technique is designed with inspiration of the method proposed in [16].

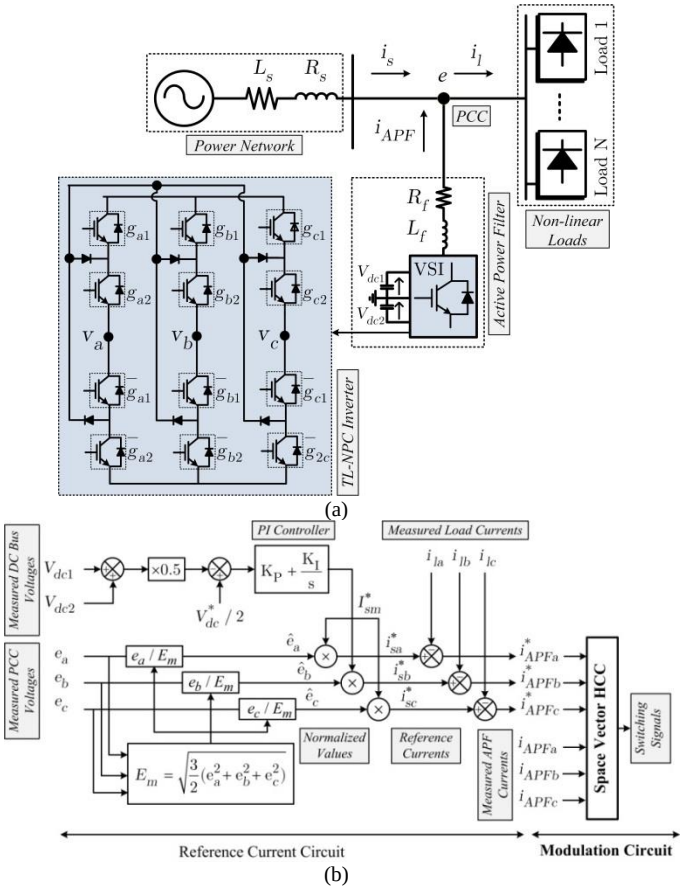


Fig. 1. (a) APF compensation principle. (b) DCC strategy.

C. Region and Segment Detection Unit

As shown in Fig. 3, the tip of the reference current vector moves on a circle around the origin of the coordinate system. The analysis is performed in SRF; hence the transformation of the three hysteresis-bands into this frame results in two circular hysteresis-bands and three regions in total. These regions are chosen in order to use the zero-, medium- and large-voltage vectors of Fig. 3(c) when the capacitor voltages are balanced and the zero and small-voltage vectors of Fig. 3-

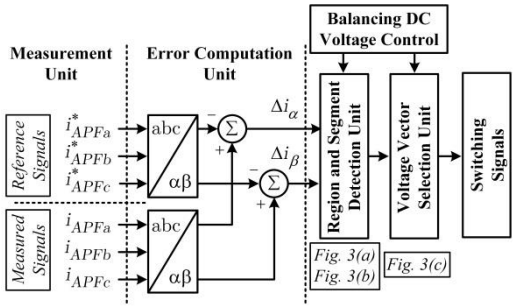


Fig. 2. SVHM modulation technique.

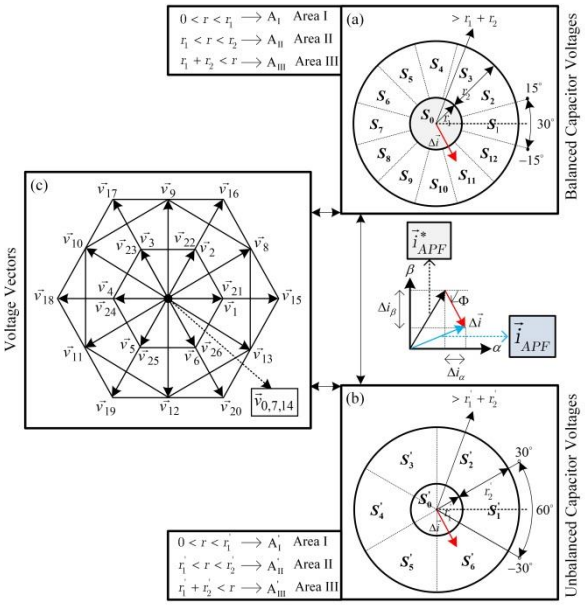


Fig. 3. Alternative hysteresis strategies. (a) Balanced capacitor voltages. (b) Unbalanced capacitor voltages. (c) Voltage vectors.

(c) when the capacitor voltages are unbalanced. The per-phase reference current and actual current can be expressed in a complex form as follows:

$$i^*_{APF} = i^*_{APF\alpha} + ji^*_{APF\beta} \tag{4}$$

$$i_{APF} = i_{APF\alpha} + ji_{APF\beta} \tag{5}$$

Correspondingly, the error vector is expressed as:

$$\Delta i = i_{APF} - i^*_{APF} \tag{6}$$

Then, it is written in SRF as:

$$\Delta i = \Delta i_\alpha + j\Delta i_\beta \Longrightarrow \|\Delta i\| = \sqrt{\Delta i_\alpha^2 + \Delta i_\beta^2} \tag{7}$$

The error vector tip can be located in one of the three regions of Fig. 3(a) (A_I, A_{II}, or A_{III}) or Fig. 3(b) (A'_I, A'_{II}, or A'_{III}). Regions A_I and A'_I characterize one segment, i.e., S_0 and S'_0, respectively. Region A_{II} is subdivided into twelve segments: S_1 through S_{12} associated with the zero-, medium- and large-voltage vectors and region A'_{II} is subdivided into six segments: S'_1 through S'_6 associated with the zero- and small-voltage vectors. The angle between any two consecutive segments is 30° for Fig. 3(a) because there are 12 distinct medium- and large-voltage vectors and 60° for Fig. 3(b) because there are 6 distinct small-voltage vectors. The tip of the error vector lies in a segment that is detected according to its region and angle Φ with respect to the α-axis.

TABLE I
DEFINITION OF SEGMENTS FOR UNBALANCED CAPACITOR VOLTAGES (C: CHARGING, D: DISCHARGING)

Angle **Φ** (Deg.)	Segment	Voltage vector	Charging Mode C_1/C_2
$\mathbf{0^\circ \le \Phi < 360^\circ}$	S'_0	$\vec{v}_0\ (ZZZ)$ $\vec{v}_7\ (PPP)$ $\vec{v}_{14}\ (NNN)$	-
$\mathbf{-30^\circ \le \Phi < 30^\circ}$	S'_1	$\vec{v}_4\ (ZPP)$ $\vec{v}_{24}\ (NZZ)$	D/C C/D
$\mathbf{30^\circ \le \Phi < 90^\circ}$	S'_2	$\vec{v}_5\ (ZZP)$ $\vec{v}_{25}\ (NNZ)$	D/C C/D
$\mathbf{90^\circ \le \Phi < 150^\circ}$	S'_3	$\vec{v}_6\ (PZP)$ $\vec{v}_{26}\ (ZNZ)$	D/C C/D
$\mathbf{150^\circ \le \Phi < 210^\circ}$	S'_4	$\vec{v}_1\ (PZZ)$ $\vec{v}_{21}\ (ZNN)$	D/C C/D
$\mathbf{210^\circ \le \Phi < 270^\circ}$	S'_5	$\vec{v}_2\ (PPZ)$ $\vec{v}_{22}\ (ZZN)$	D/C C/D
$\mathbf{270^\circ \le \Phi < 330^\circ}$	S'_6	$\vec{v}_3\ (ZPZ)$ $\vec{v}_{23}\ (NZN)$	D/C C/D

Table I give the conditions that require to be met for the error vector to reside in each particular segment to charge and discharge the capacitors when the capacitor voltages are unbalanced.

D. Voltage Vector Selection Unit

Considering Figs. 3(a) and 3(c), when the error vector tip is located in region A_I (segment S_0), the error vector magnitude is small and measured satisfactorily within the required accuracy for tracking the reference current. Then, one of the three zero-voltage vectors ($\vec{v}_0$, $\vec{v}_7$ or $\vec{v}_{14}$) closest to the previous switching is applied, and no connection is made. For the second region A_{II}, if the error vector tip is located in any of the even numbered segments, i.e., S_{l2}, S_4, S_6, S_8, S_{10} or S_{12}, one of the medium-hexagon-voltage vectors ($\vec{v}_8$, $\vec{v}_9$, $\vec{v}_{10}$, $\vec{v}_{11}$, $\vec{v}_{12}$, or $\vec{v}_{13}$) will be selected. Otherwise, one of the large-hexagon-voltage vectors ($\vec{v}_{15}$, $\vec{v}_{16}$, $\vec{v}_{17}$, $\vec{v}_{18}$, $\vec{v}_{19}$, or $\vec{v}_{20}$) will be applied when the error-vector tip is located in one of the odd numbered segments, i.e., S_1, S_3, S_5, S_7, S_9 or S_{11}.

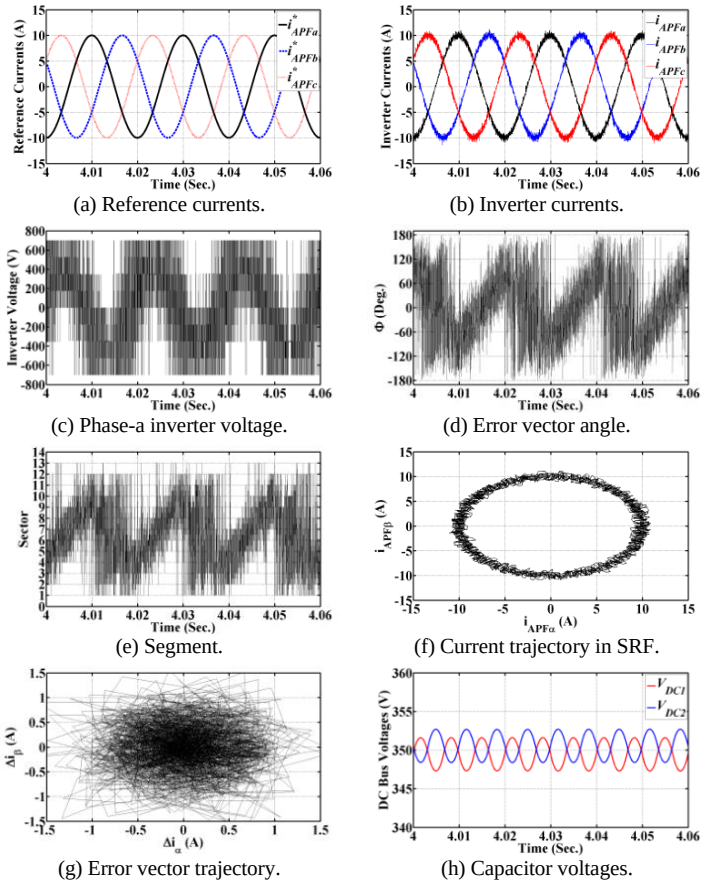
In view of Fig. 3(b), Fig. 3(c) and Table I, when the error vector tip is located in region A'_I (segment S'_0), the error vector magnitude is small and measured satisfactorily within the required accuracy for tracking the reference current. Then, one of the three zero-voltage vectors closest to the previous switching is applied, and no connection is made. But for the second region A'_{II}, if the capacitor C_1 needs to be charged, one of the charging pattern, i.e., $\vec{v}_{21}$, , $\vec{v}_{22}$, $\vec{v}_{23}$, $\vec{v}_{24}$, $\vec{v}_{25}$ or $\vec{v}_{26}$, will be selected. Otherwise, one of the discharging pattern, i.e., $\vec{v}_1$, , $\vec{v}_2$, $\vec{v}_3$, $\vec{v}_4$, $\vec{v}_5$ or $\vec{v}_6$, will be selected.

4. SIMULATION RESULTS

To verify the performance of the proposed modulation technique, four case studies are considered in this paper. The system parameters are $L_{filter} = 10\ mH$, $C_1 = C_2 = 2800\ \mu$F and $V_{dc} = 700\ V$.

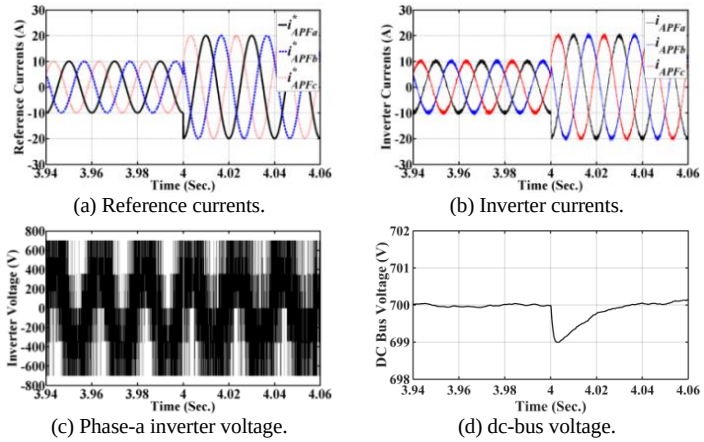
A. Case 1: Steady-State Performance of SVHM for a Grid Connected NPC inverter

In this case, the aim is to investigate the steady-state performance of the proposed technique when it is employed for the grid connected TL-NPC inverter of Fig 1(a) when the neutral point of the system is floated. The three-phase reference currents to be generated by the TL-NPC inverter



(a) Reference currents. (b) Inverter currents.
(c) Phase-a inverter voltage. (d) Error vector angle.
(e) Segment. (f) Current trajectory in SRF.
(g) Error vector trajectory. (h) Capacitor voltages.

Fig. 4. Case 1; TL-NPC Inverter producing the reference signals using SVHM under steady-state.



(a) Reference currents. (b) Inverter currents.
(c) Phase-a inverter voltage. (d) dc-bus voltage.

Fig. 5. Case 2; TL-NPC Inverter producing the reference signals using SVHM under transient.

are as follows:

$$\begin{cases} I^*_{APFa} = 10\sin\ \omega t - pi/2 \\ I^*_{APFb} = 10\sin\ \omega t - 2pi/3 - pi/2 \\ I^*_{APFc} = 10\sin\ \omega t + 2pi/3 - pi/2 \end{cases} \quad (1)$$

Figs. 4(a-h) display the simulation results with the applied proposed SVHM. As realized in Figs. 4(b) and 4(c), the actual inverter currents follow their references appropriately and the phase-a inverter voltage is created correctly. In addition, the capacitor voltages are maintained at the reference value and balanced, as shown in Fig. 4(h). This case study shows that the proposed technique works properly when applied to the TP-FNP system of Fig. 1(a) in generating the reference currents. It is to be noted that the maximum switching frequency of the proposed SVHM technique can be adjusted by selecting the outer hysteresis bands of Figs. 3(a) and 3(b).

B. *Case 2: Transient Performance of SVHM for a Grid Connected NPC inverter*

In this case, the transient performance of the proposed SVHM strategy is investigated for the grid connected TL-NPC inverter shown in Fig. 1(a). The inverter is assigned to produce the following reference currents:

$$\begin{cases} I^*_{APFa} = 10\sin\ \omega t - pi/2 \\ I^*_{APFb} = 10\sin\ \omega t - 2pi/3 - pi/2 \\ I^*_{APFc} = 10\sin\ \omega t + 2pi/3 - pi/2 \end{cases} \quad 0 < t\ < 4\ s. \quad (2)$$

$$\begin{cases} I^*_{APFa} = 20\sin\ \omega t - pi/2 \\ I^*_{APFb} = 20\sin\ \omega t - 2pi/3 - pi/2 \\ I^*_{APFc} = 20\sin\ \omega t + 2pi/3 - pi/2 \end{cases} \quad 4\ s. < t \quad (3)$$

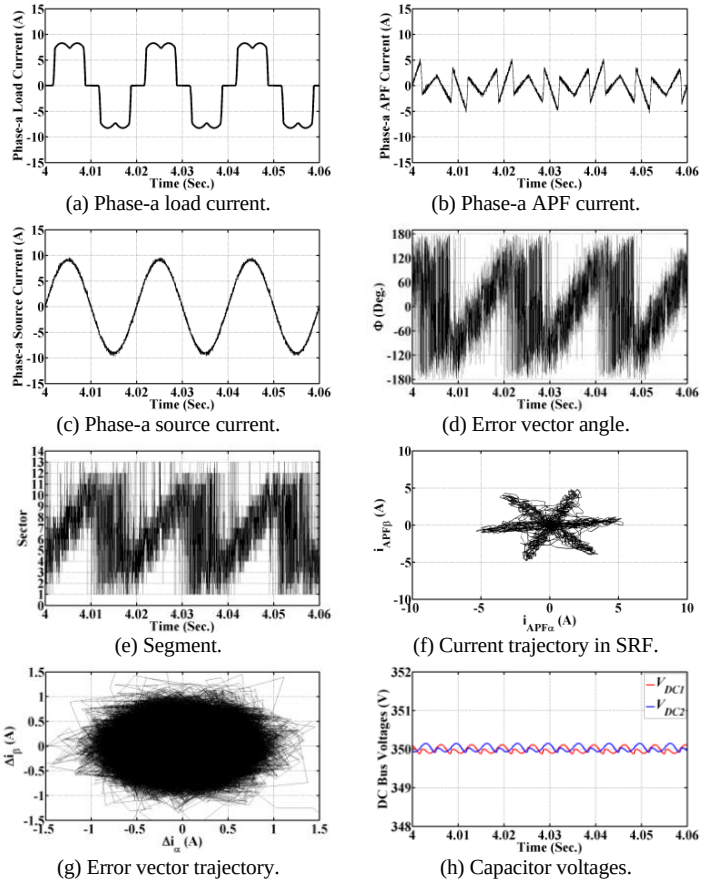
Figs. 5(a-h) depict the simulation results including the reference signals, the inverter currents, the phase-a inverter voltage and the dc-bus voltage. Figs. 5(b) and 5(d) show that the actual inverter currents and the dc-bus voltage follow their references quickly after the reference change verifying the effectiveness of the proposed technique in transient conditions.

C. *Case 3: Steady-State Performance of SVHM for an APF Compensating Nonlinear Loads*

Here, the aim is to use the proposed modulation technique for APF application. Therefore, the structure of Fig. 1(a) is simulated for the steady-state condition when its neutral point is floated. The APF control strategy is shown in Fig. 1(b). In this figure, APF attempts to recover the power quality of the system by compensating the nonlinearity of the load currents using meaning that it injects a nonlinear current (equal in magnitude but opposite in phase) to cancel the load current harmonics and impose a sinusoidal source current. This task of APF is not completed unless the modulation technique used in the control structure works properly. The modulation technique used in APFs becomes very critical when it is applied in TP-FNP systems. Here, for the sake of simplicity, the phase-a load, APF and source currents are shown. As can be observed in Figs. 6(a-h), the phase-a APF current follows its reference and compensates the load current appropriately such that the source current is almost sinusoidal locked in-phase with the source voltage and, at the same time, the capacitor voltages are kept balanced.

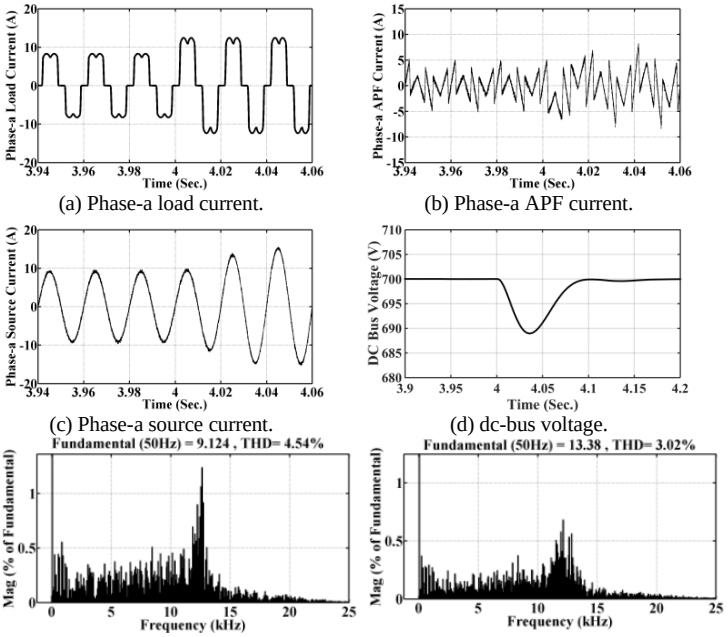
D. *Case 4: Transient Performance of SVHM for an APF Compensating Nonlinear Loads*

Here, the structure of Fig. 1(a) is simulated for a transient condition (a sudden load change, i.e., a 100% increase shown in Fig. 7(a)). As can be comprehended in Figs. 7(a-f), the phase-a APF current follows its reference and compensates the load current very quickly after the load change. The harmonic spectrums of the source current before and after load change are shown in Fig. 7(e) and Fig. 7(f), respectively. The THD percentage of the source current is kept lower than 5%, which is the standard value in the distribution level, while the THD percentage of the load current is 27% [17]. These figures also verify the proposed technique capability in avoiding high switching frequencies triggered by phase interaction due to the floated neutral point of Fig. 1(a).



(a) Phase-a load current. (b) Phase-a APF current.
(c) Phase-a source current. (d) Error vector angle.
(e) Segment. (f) Current trajectory in SRF.
(g) Error vector trajectory. (h) Capacitor voltages.

Fig. 6. Case 3; APF compensating nonlinear loads using SVHM under steady-state.



(a) Phase-a load current. (b) Phase-a APF current.
(c) Phase-a source current. (d) dc-bus voltage.
(e) Harmonic spectrum of phase-a source current before load change.
(f) Harmonic spectrum of phase-a source current after load change.

Fig. 7. Case 4; APF compensating nonlinear loads using SVHM under transient.

5. Conclusion

This paper presents a new space-vector HCC modulation approach implemented in SRF. The application is the three-level NPC-based APF. The procedure has been done in SRF by converting the three error-currents to a single vector that can be located in 12 segments of the first hysteresis strategy associated with the zero-, medium- and large-voltage vectors and 6 segments of the second hysteresis strategy associated with the zero- and small-voltage vectors for balanced and unbalanced capacitor voltages, respectively. As a result, the interphases dependency, which causes high switching frequency in TP-FNP systems, is prevented. The validity of the proposed method is shown through extensive simulation investigations applied to TP-FNP systems for both the steady-state and transient conditions.

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