REDUCING THE POWER DISTURBANCES IN MULTI FEEDERS BY USING MC-UPQC WITH MICROGRID BASED RENEWABALE GENEREATION UNITS

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Abstract: *Multiple bus or Multiple Feeders for compensation of Voltage and Current Systems by using unique Multi-Converter Unified Power Quality Conditioning (MC-UPQC) System is presented in this paper. This proposed scheme can be adapted to the nearby power supplies to correct the voltage and receiving end current deviations in the central power supply and complete rectification of the power supply deviations in the remaining power supplies. By employing MC-UPQC here, power quality is upgraded to renewable energy based systems. On the DC side of all the inverters are connected to one side of the other and support a common condenser connection. So that power can be shifted from a power supply to nearby power supplies to rectify interruptions and voltage drops. The principle of grinding and various control strategies that are used based on ANNs and PI regulators. The MC-UPQC execution and control process is represented by MATLAB for two power feeders / bus scheme.*

Keywords: *Unified Power-Quality Conditioner (UPQC), Proportional Integral (PI) controller, Voltage-Source Converter (VSC), Power Quality (PQ), Artificial Neural Network (ANN).*

*I. I*ntroduction

Today is a day with the increased use of power electronics devices and non-linear load applications in industrial sectors power schemes have Power Quality (PQ) problems. PQ troubles such as dip / surge increase, transients and interruptions are caused by capacitor bank switching, lightning effect on transmission lines, and various types of faults. [1].

Some kind of compensation must be incorporated into the system to overcome PQ problems. To compensate for current connected problems for example reactive power compensation, active power filters (APFs) are coupled in parallel with loads [2]. To overcome the voltage-related problems, such as dip/ overvoltage, active power filters [3] are applied.

Distribution schemes incorporate applications of FACTS devices that result in modern rectifying devices. UPQC is a custom power device and is the elongation of the unified power flow controller (UPFC). UPQC is composed of series and shunt converters for concurrent rectification of voltage and current deviations in the power supply [4] - [7]. In order to control the multi-line power flow, multi-inverter devices (FACTS) are used as the interline power flow controller (IPFC) [8] and the generalized unified power flow controller (GUPFC) [9]. IPFC has to be used to control the power flow of two lines initiating at the same substation. An IPFC have two serial VSCs and its DC capacitors are paired so that the active energy is circulated between the VSCs.

To get better power quality for multiple converter structures are built in such a way that the main power bus is powered by variable wind speed and another feeder was powered by the solar source. UPQC comprises a series and one of the shunt converters and coupled among two feeders for controlling the bus voltage of one of the feeder and the voltage across a quick to respond load on the additional feeder. Shunt-VSC is used to control the voltage in one of the feeders. A large quantity of current has to be required to improve the bus voltage in the event of a drop or overvoltage because the source impedance is very low and the dynamic performance is very poor due to the unregulated dc link condenser voltage.

UPQC is a novel facility called MC-UPQC as proposed in this document. The structure is enhanced by inserting a VSC series into the nearby power supply. This setting is used to balance voltage and current deviations by distributing power capacities between power supplies the nonbinding scheme without battery storage. The correction principle and various manage strategies that are used are based on ANNs and PI controllers. The execution of MC-UPQC and process control is represented by MATLAB for two power feeders / bus scheme.

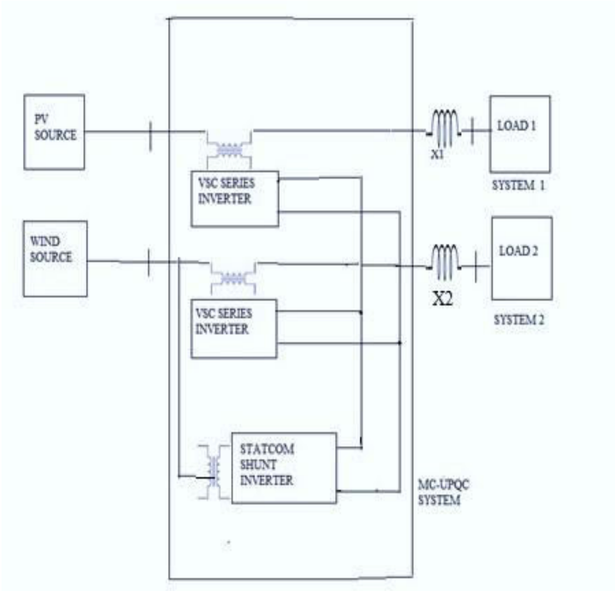

Fig.1.Block diagram of MC-UPQC with STATCOM

II. MC-UPQC Scheme

A. Circuit arrangement

Linear illustration of a Distribution Scheme by a MC-UPQC is revealed in Fig.1.In These two power supplies are coupled to two separate substrates L1 and L2 loaders loaded with STATCOM. MC-UPQC is BUS1 and BUS2 merged for voltages u_{t1}andu_{t2} respectively. Load current i_{l1} view is connected to the shunt part of the MC-UPQC. Power voltages are represented as u_{s1} and u_{s2} while receiving end voltages are u_{l1}andu_{l2}. Lastly, power currents are represented by i_{s1} and i_{s2} and receiving end currents are i_{l1}andi_{l2}.

Voltage dip/surge is caused due to disturbance in bus voltages u_{t1} and u_{t2}. Ideal sinusoidal voltage for a proper operation since the load L1 is a sensitive or non linear load. Similarly, a sinusoidal voltage ideal for accurate action is needed as L2 load is a linear / load sensitive and fully protected against dip / drop distortion and disturbance. These types of loads principally consists of manufacture companies and important service providers, such as medicinal laboratories, airports, or information publishing centers where voltage disturbance can result in waste of financial losses or man power loss. In this arrangement using a FACT device which is MC-UPQC for mitigation of voltage and current variations and it consists of series connected VSC's for using the non-liner loads i.e. nothing but sensitive loads those produce the current harmonics which are injects in to the system. When the current harmonics are injected the voltage disturbances are occurring in the system. So at this time we are deleting the current harmonics for effective operation of the scheme without disturbances. Here we are taken the MC-UPQC technique for effective solution of eliminating the current harmonics and maintain constant voltage giving to the load for the operation of reactive power compensation. the MC-UPQC is placed in between the multi-feeders for protecting the feeders from harmonic distortions and it should maintain the power quality through the line and protects the load from power quality problems.

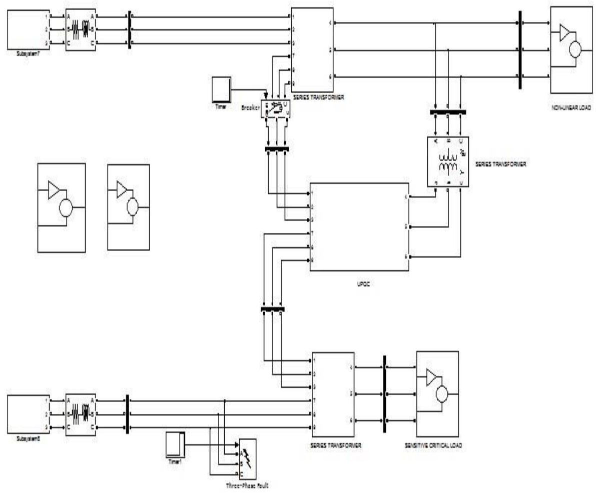

Fig.2 Simulation of typical MC-UPQC block diagram used in the power supply scheme

B. MC-UPQC Structure

The inside construction of the MC-UPQC is give details in FIG. 2. It include several VSCs (VSC1, VSC2 and VSC3), which are side by side through a common DC link capacitor. VSC1 is sequentially associated with BUS1 and VSC2 is laterally bound to load L1 in the last part of Feeder1. VSC3 is sequentially associated with BUS2 at the Feeder2 end and the three VSCs in Fig. 2 are executed by a three-phase converter having a switching reactor and a high-pass output filter shown in Fig. 3. The reactor (L_f) and the high-pass output filter (R_f, C_f) are combined to interrupt the movement of the control harmonics in the power scheme as shown in Fig. 3.

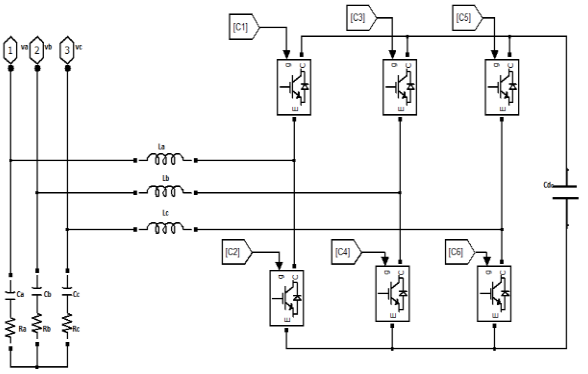

Fig.3 Schematic structure of a VSC

Each converter is equipped with a common intermediate circuit capacitor and is coupled to the delivery scheme with the transformer. Secondary (distribution) series connected transformer sides are coupled in sequence with BUS1 and BUS2, and the secondary side (distribution) of the parallel linked transformer joins lateral load L1. . The main objectives of the MC-UPQC display in Figure 2 are:

1. For charge voltage control (u_{l1}) immersion / overvoltage and troubles in the scheme to preserve nonlinear / reactive L1 load;
2. To check the charge voltage (u_{l2}) against dip/surge, interruption and scheme noise to preserve the sensitive / critical load L2;
3. To rectify reactive components and nonlinear receiving end current harmonics (i_{l1}).

To accomplish these objectives, the VSC series (i.e., VSC1 and VSC3) functions as voltage controllers at the same time as the VSC shunt (i.e., VSC2) functions as a current regulator.

C. Control Strategy

Fig.4 displays the MC-UPQC consists of series VSCS (VSC1 and VSC3) and one shunt VSCs(VSC3) which are managed separately. The operation of switches for series and shunt VSCs are choose to be sinusoidal Pulse width-modulation (SPWM), control of voltage and hysteresis current correspondingly. Procedure of the managed method i.e. *d-q* method [10], will be explained afterwards.

Shunt-VSC: Activities of the shunt-VSC are:

1. Reductions of the Reactive component in receiving end current L1;
2. Reduction of the Harmonic components in receiving end current L1;
3. Controls the voltage of the common dc-link capacitor.

The determined receiving end current ($i_{l_{abc}}$) is reconstructed into the synchronous *dq0* reference frame by using

$i_{l\_dq0} = T_{abc}^{dq0}\, i_{l\_abc}$ ---------------- (1)

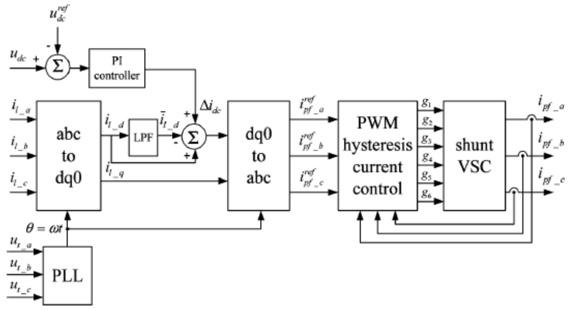

Fig. 4 Displays the block illustration for shunt VSC control.

Where the conversion matrix is revealed in (2).

$T_{abc}^{dq0} = \frac{2}{3}$2)

From this alteration, the direct sequence key element, that is reconstructed in DC quantities on axes d and q, can simply be derived from low-pass filters (LPFs). All harmonic elements are rebuilt in alternating current quantities with a fundamental frequency variation

$i_{l\_d} = \bar{i}_{l\_d} + \tilde{i}_{l\_d}$--(3)

$i_{l\_q} = \bar{i}_{l\_q} + \tilde{i}_{l\_q}$--(4)

Receiving end current d-q factors are i_{l_d}, i_{l_q} and $\bar{i}_{l\_d}$, $\bar{i}_{l\_q}$ are dc elements, where as $\tilde{i}_{l\_d}$, $\tilde{i}_{l\_q}$ are ac elements of i_{l_d} and i_{l_q}.

Feeder current is i_s and i_{pf} is the shunt VSC current therefore i_s=i_l-i_{pf}, and *d-q* elements of the shunt VSC reference current are characterized as follows:

$i_{pf\_d}^{ref} = \tilde{i}_{l\_d}$ -----------------------------(5)

$i_{pf\_q}^{ref} = i_{l\_q}$-------------------------------(6)

Therefore the *d-q* elements of the feeder current are

$i_{s\_d} = \tilde{i}_{l\_d}$ ----------------------------------- (7)

$i_{s\_q} = 0$ ---------------------------------(8)

From the above equations we can say that no harmonic and reactive elements in the power supply. The capacitor voltage dc link is reduced due to the reduction of switching losses.

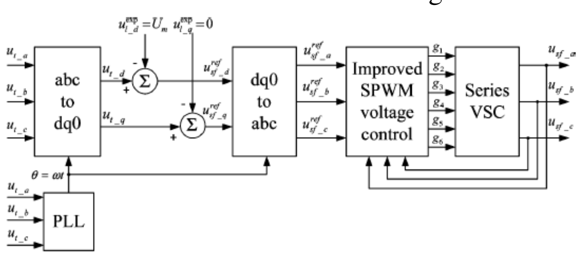

Fig.5.Control block diagram of the series VSC

Additional disturbances such as sudden receiving end changes affect the dc link. The proportional-integral controller (PI) is used to adjust the DC link voltage as shown in Figure 4. The difference between the actual capacitor voltage (u_{dc}) and its reference value (u_{dc}^{ref}) is given as input to PI controller. A new reference current is obtained by summing the output of the PI controller (i.e.,Δi_{dc}) and the component d of the reference current shunt-VSC

$$\begin{cases} i_{pf\_d}^{ref} = \tilde{i}l\_d + \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \text{-------------------(9)}$$

As displayed in Fig. 4, the reference current (9) is then changed again to the abc reference. Transient output voltages in each phase are carried out using PWM control current hysteresis.

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc} i_{pf\_dq0}^{ref}; \quad (T_{dq0}^{abc} = T_{abc}^{dq0-1}) \text{---- (10)}$$

Series-VSC: VSC series activities in each power supply are:

1) To reduce the voltage drop at receiving end;

2) Correct the distortion of voltage as harmonics;

3) Disturbances are remunerated. (In Feeder2 only).

The control block drawing of each VSC series displayed in Fig. 5. The voltage bus (u_{t_abc}) is recognized and therefore the synchronous reference converted synchronous dq0 using

$$u_{t\_dq0} = T_{abc}^{dq0} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th} \text{------(11)}$$

Where

$$\begin{cases} u_{t1p} = [u_{t1p_d} u_{t1p_q} \ 0]^T \\ u_{t1n} = [u_{t1n\_d} u_{t1n\_q} \ 0]^T \\ u_{t10} = [0 \ 0 \ u_{00}]^T \\ u_{th} = u_{th\_d} u_{th\_q} u_{th\_0}]^T \end{cases} \text{------------(12)}$$

u_{t1p}, u_{t1n} and u_{t10} are positive fundamental frequencies, negative and zero components, correspondingly, and u_{th} is the harmonic component of the bus voltage.

Despite variations in the bus voltage, charging voltage must be maintained sinusoidal stable with amplitude control based on the MC-UPQC targets. The dq0 voltage charging family synchronous reference ($u_{l\_dq0}^{exp}$) has a single value.

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0} u_{l\_abc}^{exp} = \begin{bmatrix} u_m \\ 0 \\ 0 \end{bmatrix} \text{-----------------(13)}$$

The receiving end voltage in the *abc* reference frame ($u_{l\_abc}^{exp}$) is represented as

$$u_{l\_abc}^{exp} = \begin{bmatrix} u_m \cos(wt) \\ u_m \cos(wt - 120^0) \\ u_m \cos(wt + 120^0) \end{bmatrix} \text{-------------(14)}$$

The reference voltage with the synchronous reference dq0 ($u_{sf\_dq0}^{ref}$) is represented as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \text{------------------(15)}$$

This means that u_{t1p_d} to (12) should continue to U_m while remaining not needed apparatus should be ignored. The reference voltage compensation (15) is converted to the reference abc.

The compensation voltage output of the VSC series can be determined using an enhanced SPWM voltage control method (while the PWM feedback is less) [11].

D. Designing & Training of ANN

Nonlinear elements join in to form the artificial neural network (ANN) have the potential to study and implement. ANNs are described using its construction based on how they communicate, trained and the ability to calculate information [12]. ANN's becomes a feasible control tool due to error tolerance, instinct accuracy and ease of use.

To get better the quality of the control [13], hard drivers are replaced with intelligent controllers, which have become a substitute for neural controllers instead of fuzzy controllers. A feed network functions three layers as clearing signals has been designed. The input layer consists of seven neurons, the unseen layer 21 and includes the output layer has three neurons. Commencement jobs are selected as pure sigmoid and linear in concealed layers and output correspondingly.

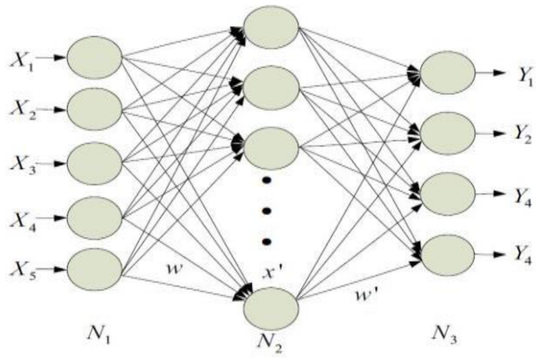

Fig.6 System structure of ANN

Levenberg Marquardt back propagation (LMBP) training algorithm is used. Mat lab coding of ANN working out is given in the referred paper [14].

Based on the input compensator and output evolution is determined. The network selected up to seven inputs for the three charge voltage reference three of which for the current source and rest is output of the PI controller. For fundamental reference output currents [15] the neural network is trained and received signals are compared with the current regulator for signal hysteresis band switching[16]. The component blocks of the ANN equalizer has to be mentioned and displayed in fig.7.

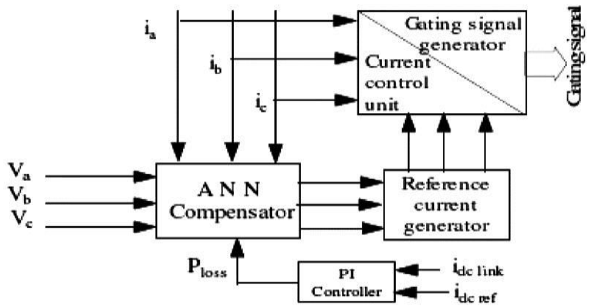

Figure.7 Functional drawing of ANN-based equalizer

III. Power-rating analysis of the MC-UPQC

Two UPQC models, including the finest model that requires nominal power, while the power of every VSC in MC-UPQC configuration is calculated are selected because the rated power of MC-UPQC is a cost-effective feature. There is two models of UPQC i.e. compensation quadrature (Q-UPQC) and phase compensation (UPQC-P). Steady state true power is exhausted from the VSC series because the fed voltage is in phase quadrature by power supply. If UPQC reduces the voltage drop it became a symbolic advantage. The nominal VSC-mitigated power rating because the VSC-series also shares the VAR (VAR) volts with the VSC-tangential.

Phasor establishment in a typical receiving end power factor lacking sinking voltage shown in Figure 8. The injected series voltage (U_{sf}) is zero if the bus voltage is at the preferred value (U_l = U_t= U_0) [Fig.8(a)]. The reactive load component I_c is injected by VSC shunt resulting from the input power unit. Harmonic apparatus of the receiving end current are remunerated by the responsive VSC shunt component. Subsidence sag reparation in this model requires the injection of the quadrature series voltage as revealed in Fig. 8 (b).

When power is balanced, the fed voltage is in phase with the power supply voltage in UPQC-P. The vector diagram of Fig. 8 (c) explains how the scheme is in case of voltage sag case.

For special sag conditions and receiving end power factors a contrast is made between UPQC-P and UPQC-Q replicas [13]. For a factor of less than or equal to 0.9, the rated power of the shunt-VSC in the UPQC-Q model is inferior than the UPQC-P, and the nominal VSC power rating in the UPQC-P model is inferior than the UPQC- Q. If VAR load demand is heavy, then the total UPQC-Q power is inferior than UPQC-P.

Shunt Feeder1 VSC and VSC Feeder2 series provide the power needed to compensate Feeder2 breaks. The powers of these VSCs are over and above those of a standard one in Feeder1. If UPQC-Q is selected in Feeder1 and UPQC-P in Feeder2, the rated power of the VSC shunt and VSC series (in feeder2), which is an essential condition for realistic purposes, will be reduced.

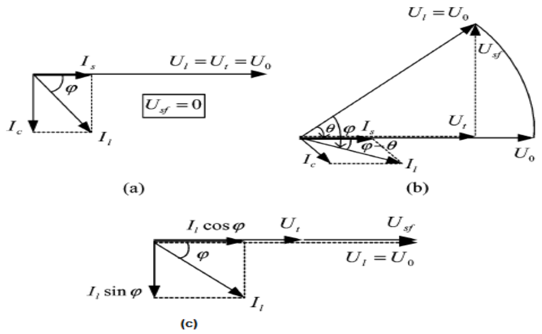

Fig.8.Phasor compensation quadrature diagram. (a)Non considering voltage droop (b) Considering voltage droop (c) Phase-phase compensation Scheme (droop voltage)

According to the linear load at the primary frequency, the power calculation is performed for MC-UPQC. To indicate the parameters of the feeder 1, the suffix 1 in figure 6 and the suffix power supply 2 parameters are added in Figure 2. The receiving end currents in both power supplies remain unchanged at their nominal value (i.e., I_{01} and I_{02} respectively) Voltage variations in both power supplies remain unchanged in U_0.

$$U_{l1} = U_{l2} = U_0 \text{ -------------------------------- } (16)$$

$$\begin{cases} I_{l1} = I_{01} \\ I_{l2} = I_{02} \end{cases} \text{ -----------------------------------}(17)$$

$\cos\varphi_1$ and $\cos\varphi_2$ are the receiving end power factors in Feeder1 and Feeder2 respectively and the per-unit sags, these should be remunerated in Feeder1 and Feeder2, are made-up to be x_1 and x_2.

Considering MC-UPQC has losses, the demand for wattful energy Feeder1 consists of two parts: Demand load of active power in Feeder1; Demand for active power by subsidence and switch off Feeder2.

Thus, the feeder1 current (I_{s1}) can be determined as

$$U_{t1}I_{s1} = U_{l1}I_{l1}\cos\varphi_1 + U_{sf2}I_{l2}\cos\varphi_2 \text{-------}(18)$$

$$(1 - x_2)U_0I_{s1} = U_0I_{01}\cos\varphi_1 + x_2U_0I_{02}\cos\varphi_2 \text{-}(19)$$

$$(1\text{-}x_1)I_{s1} = I_{01}\cos\varphi_1 + x_2I_{02}\cos\varphi_2 \text{--------}(20)$$

$$I_{s1} = \frac{I_{01}\cos\varphi_1}{(1-x_1)} + \frac{x_2I_{02}\cos\varphi_2}{(1-x_1} - - - - - - -(21)$$

In Figure 6, the voltage fed by the VSC series into the feeder 1 is to be give as in (22) and therefore the rated power of the converter (S_{VSC1}) can be formulated as

$$U_{sf1} = U_{t1}\tan\theta = U_0(1 - x_1)\tan\theta \text{--------}(22)$$

$$S_{VSC1}=3U_{sf1}I_{s1}=3U_0(1-x_1)\tan\theta\times\left(\frac{I_{01}\cos\varphi_1}{1-x_1}+\frac{x_2I_{02}\cos\varphi_2}{1-x_1}\right)\text{--}(23)$$

The VSC shunt current is divided into two parts.

1) The primary element (i.e., I_{c1}) balances for the (harmonic and reactive factors) current element Feeder1 and can be formulated from Fig. 6 as

$$I_{c1}=\sqrt{I_{l1}^2+I_{s1}^2-2I_{l1}I_{s1}\cos(\varphi_1-\theta)}$$

$$=\sqrt{I_{01}^2+I_{s1}^2-2I_{01}I_{s1}\cos(\varphi_1-\theta)}\text{-------}(24)$$

Where I_{s1} is calculated in (21). This ingredient of the current VSC shunt only interacts reactive power (Q) among the scheme.

2) The secondary element supplies the real power (P), which is desirable to balance for droop or collapse Feeder2. For that reason, the nominal power of the VSC shunt can be formulated as

$$S_{VSC2}=3U_{l1}I_{pf}=3\sqrt{Q^2+P^2}$$

$$=3\sqrt{(U_{l1}I_{c1})^2+(U_{sf2}I_{l2}\cos\varphi_2)^2}$$

$$=3U_0\sqrt{I_{c1}^2+(x_2I_{02}\cos\varphi_2)^2}\text{----------------}(25)$$

Where I_{c1} is formulated in (24).

Finally, the rated power of VSC series Feeder2 can be formulated(26). For the most awful situation (i.e. clearing off), you should consider x_2=1. Therefore

$$S_{VSC3}=3U_{sf2}I_{l2}=3x_2U_0I_{02}\text{-----------------}(26)$$

IV. Design of MC-UPQC using FUZZY

For representing unclear, imperfect and uncertain information Fuzzy logic is an adoptable and capable tool and also helps to model tough and even incurable problems. For figure outing the system performance in detail all the control algorithms are approved by MATLAB simulation. For designing the control law no mathematical modeling is required in Fuzzy logic and it is the main advantage. Based on system behavior, information and control experience, a set of control rules are used by fuzzy controllers. Even if the mechanical parameters are varied Fuzzy controllers cannot mould themselves to the operation conditions variations like PID controllers. An innovative adaptive fuzzy control law is constructed in this paper.

Fuzzy logic is a new control approach with great potential for real time applications Fig 5.3 shows the structure of the fuzzy logic controller (FIS-Fuzzy inference system) in MATLAB Fuzzy logic toolbox. .Load voltage and load current taken as input to fuzzy system. For a closed loop control, error input can be selected as current, voltage or impedance, according to control type . To get the linearity triangular membership function is taken with 50% overlap. The output of fuzzy controller taken as the control signal and the pulse generator provides synchronous firing pulses to switches as shown in fig.10.

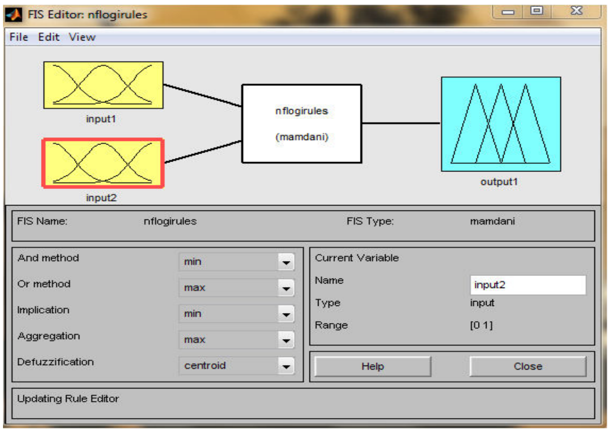

Fig.9. Fuzzy interface scheme

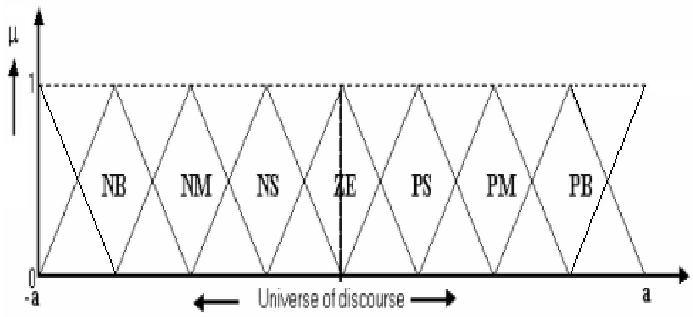

Fig.10 Triangular membership functions

Fuzzy classifiers are one application of fuzzy theory. Expert knowledge is used and can be expressed in a very natural way using linguistic variables , which are described by fuzzy sets Now the expert knowledge for this variables can be formulated as a rules like IF feature A low AND feature B medium AND feature C medium AND feature D medium THEN Class = class 4The rules can be combined in a table calls rule base.

As the number of linguistic variables increases, the computational time and required memory increases. Therefore a compromise between the quality of control and computational time is needed to choose the number is seven. Each linguistic variables NB, NM, NS, ZE, PS, PM, PB which stands for negative big, negative medium, negative small, zero positive small, positive medium, positive big respectively. For simplicity it is assumed that the membership functions are symmetrical and each one overlaps the adjacent functions by 50% i.e., triangle shaped function, the other type of functions used are trapezoidal-shaped and Bell-shaped. Figure 10 shows the seven linguistic variable and the triangular membership function with 50% overlap and the universe of discourse from – a to a.

Load current \ Load voltage	NL	NM	P	PM	PB
NL	PB	PB	NM	NM	NL
NM	PB	PB	NM	P	NL
P	P	PM	NM	NM	P
PM	NM	P	NM	NM	PM
PB	NL	NM	NM	NL	NL

Table 1. Membership function rules

V. Simulation results

MC-UPQC and ANN verify methods evaluated using MATLAB and MC-UPQC scheme behavior are represented.

The power supply of Fig. 2, comprising two 3-phase 3-wire 380v (rms), L-L, 50 Hz utility. The BUS1 (voltage is u_{t1}) and BUS2 (voltage is u_{t2}) voltage is the seventh harmonic of the order of 22% and the fifth Harmonic of 35%. BUS1 voltage has a 25% drop of 0.1 s <t <0.2 s and a 20% increase of 0.2 s <t <0.3 s. BUS2 voltage is having a fall of 35% between 0.15 s <t <0.25 s and 30% between 0.25 s <t <0.3 s. Nonlinear / Sensitive Load L1 is a three-phase rectifier load RC values 10Ω and 30µF and L2 critical load balancing RL values 10 Ω and 100 mH.

MC-UPQC lights up at t = 0.02 s. The BUS1 voltage, the VSC1 voltage fed and the voltage load L1 displayed in Fig. 11. In each and every one figure, no more than the phase waveform revealed.

In the same way, BUS2 voltage, VSC2 injected voltage and receiving end voltage L2 displayed in Fig. 12. The BUS1 and BUS2 disturbances properly compensated by loads L1 and L2 with a superior dynamic response.

The nonlinear receiving end current, the injected compensated current for VSC2 and the supply current 1 and the DC condenser circuit voltage shown in Fig. 13. The total harmonic distortion (THD) of the supply current is decreased to 5% from 28.5%. Despite all the conflicts as dip / overvoltage on both power supplies, DC voltage control has worked successfully. (MC-UPQC) of the rectified source voltage, receiving end current, and minimize any variation in current, over-current in the network. By comparing different manage strategies, the results of the simulation are shown in Figures 11, 12, 13 and 14.

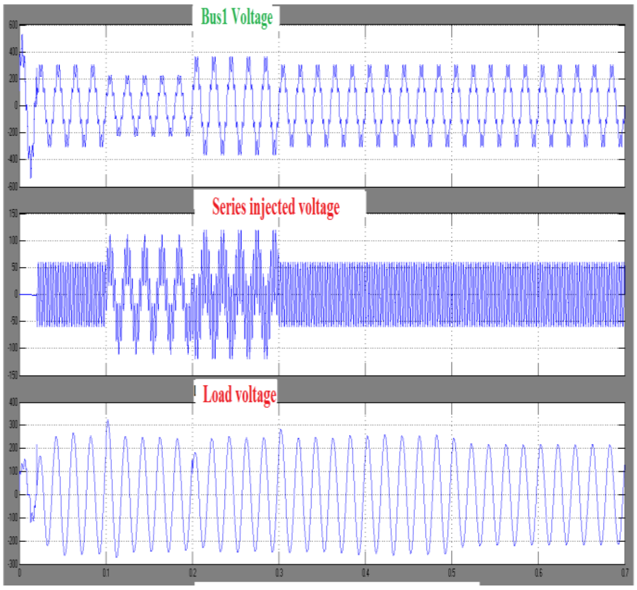

Fig.11 Parameters of feeder1 (Bus1 voltage, series injected voltage and receiving end voltage) Distortion and dip/surge on the Bus voltage

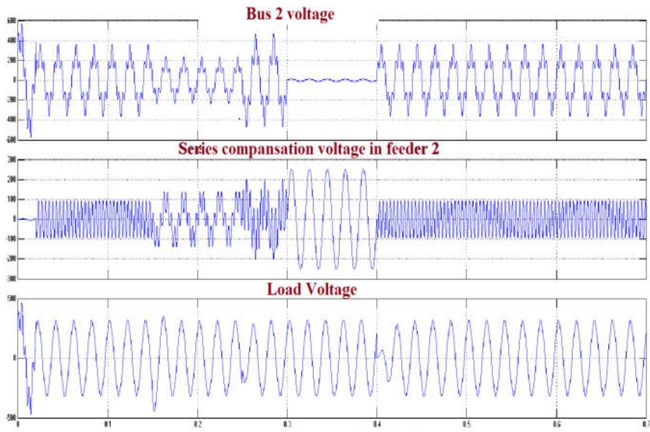

Fig.12 Parameters of feeder2 (Bus2 voltage, series injected voltage and receiving end voltage)

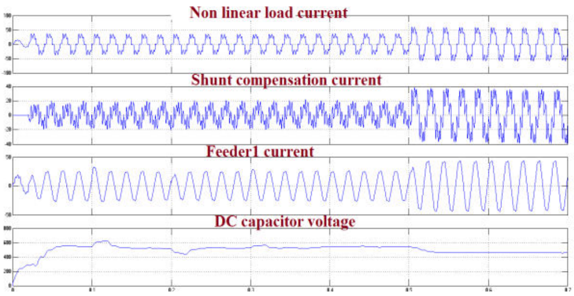

Fig.13 Nonlinear loads; shunt compensation current, feeder1 current and DC capacitor voltage

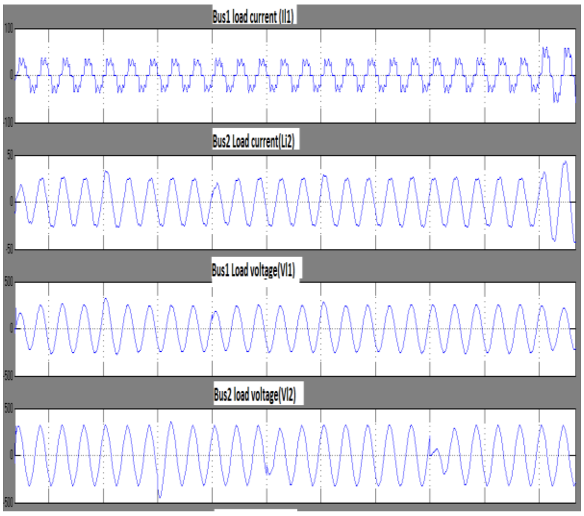

Fig 14. Bus1, bus2 receiving end currents, bus1 and bus 2 receiving end voltages

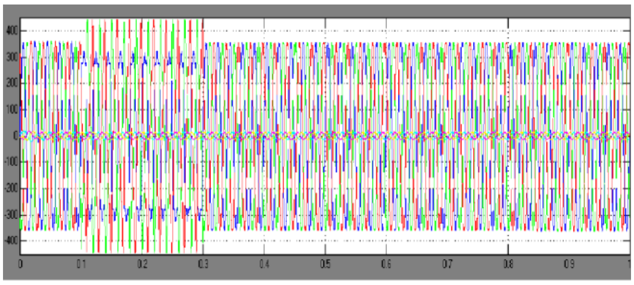

Fig 15. Three phase source voltage (V_a, V_b, V_c) wave form

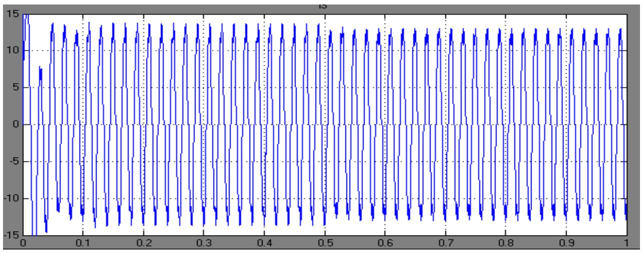

Fig.16 Receiving end current with ANN controller

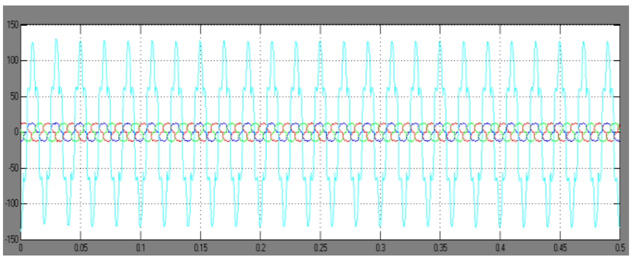

Fig.17 Receiving end voltage with ANN Controller

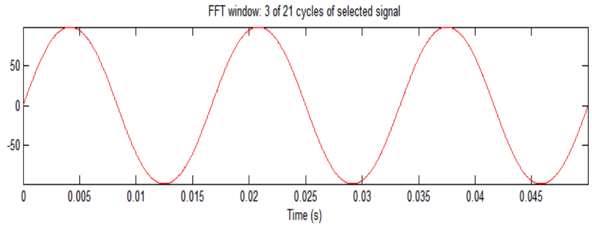

Fig.18 Input voltage

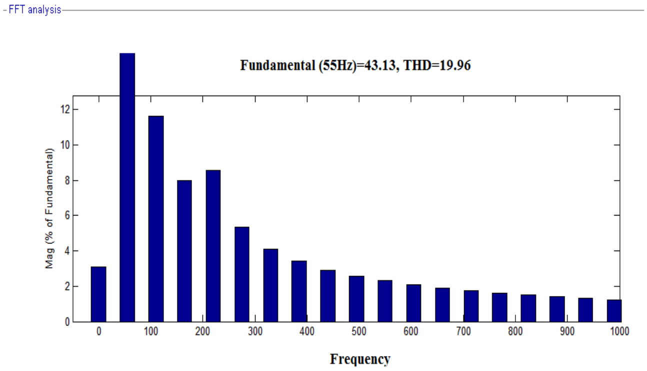

Fig.19 Total Harmonics Distortion with PI Controller

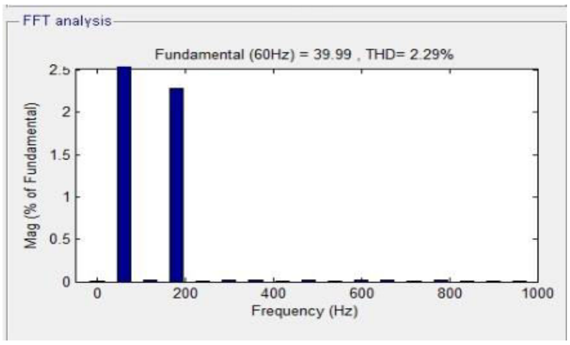

Fig.20 Total Harmonics Distortion with the ANN Controller

VI. Conclusion

For the compensation of voltage as well as current in the neighboring feeders MC-UPQC is proposed. It can completely protect critical loads and sensitive distortions against, fall / disturbance wave and the system cause at normal UPQC Responsive Power Supplies Insertion, more VSC series method this extends to multi-power / multi-bus schemes. To improve the quality of energy in a more unconventional method ANN base power supplies play a role and from important ones. Assessing Disruption Implementation Conditions in Various Proposals MC-UPQC has some benefits, easy battery and Necessary Storage Scheme will not be offset by interruptions.

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