# COMPARATIVE ANALYSIS OF SINUSOIDAL PWM STRATEGIES FOR THREE PHASE SYMMETRICAL CASCADED H-BRIDGE SEVENTEEN LEVEL INVERTER WITH REDUCTION OF SWITCHES

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***Abstract –*** *This paper presents the comprehensive analysis of three phase symmetrical cascaded H-bridge (CHB) seventeen level inverter with reduced number of switches. Different bipolar Multicarrier level shifted Pulse Width Modulation (MCPWM) techniques such as Phase Disposition PWM (PDPWM), Carrier Overlapping PWM (COPWM) and Variable Frequency PWM (VFPWM) with sinusoidal reference are used to implement the proposed multilevel inverter (MLI) topology. The proposed MLI uses reduced number of switching devices thereby reducing losses and Total Harmonic Distortion (THD) compared to the conventional MLI topology. The time domain simulation of the proposed seventeen level inverter is carried out in Matlab/Simulink environment. The various performance factors such as %THD, $V_{RMS}$, and $V_{PEAK}$ are calculated for two different modulation indices and the results are compared. The results demonstrate that the PDPWM technique provides relatively low %THD and the COPWM technique provides relatively higher fundamental RMS output voltages for the proposed seventeen level inverter having unity modulation index.*

***Keywords: CHBMLI, COPWM, MCPWM, PDPWM, Reduced switches, THD, VFPWM.***

## 1. Introduction

The multilevel inverters have drawn tremendous interest in the power industry. It may be easier to produce a high-power, high-voltage inverter with the multilevel structure because of the way in which device voltage stresses are controlled in the structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual device can increase the power rating. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without the use of transformer or series connected synchronized switching devices. As the number of voltage levels increases, the harmonic content of the output voltage waveform decreases significantly [1, 2]. There are three types of multilevel inverter topologies [3]: (i). Diode-clamped, (ii). Flying-capacitors, and (iii). Cascade multilevel inverter. The cascaded H-bridge inverter requires least number of components to achieve the same number of voltage levels compared to diode-damped and flying-capacitor inverters. Multilevel inverters have more advantages with respect to the traditional two-level configurations. They offer a low output voltage THD, and a high efficiency and power factor [4, 5]. However, the main disadvantages of multilevel structures against the traditional two-level configurations are the requirement of more number of switching elements, and so the inverter circuit and control scheme will be complex. Hence, the cost of inverter, losses, and installation area are increased, and the efficiency and reliability of the inverter are reduced.

Table 1 Comparison of Efficiency and Cost of commercial multilevel converters

| Inverter | Power (VA) | Peak Efficiency (%) | No-load Power (W) | Mean Price (€) |
|---|---|---|---|---|
| Phoenix 48/3000/35 | 3000 | 95.0 | 10.0 | 2.8 |
| Studer C3548 | 3500 | 95.0 | 12.0 | 1.8 |
| Dakar 48/3000/50 | 3000 | 90.0 | 4.8 | ---- |
| SMA Sunny Island 3324 | 3300 | 94.5 | 22 | 2.3 |
| SMA Sunny Island | 3300 | 92.0 | < 10 | ---- |
| Trace SW3048 | 3300 | 95.0 | 16.0 | ---- |
| Xantrex SW2548 | 2500 | 95.0 | < 20 | 1.8 |

The Table 1 shows the comparative assessment of efficiency and cost of some commercial multilevel converters available in the market [6]-[11]. In Table 1, the prices of selected commercial inverters are given [12]. However, the slightly improved efficiency and slightly reduced cost can further be achieved with the reduced switch count solution for the large multilevel converters. Therefore, reducing the number of circuit devices is the main concern from the design point of view.

Many topologies were presented in the last decade focusing on minimizing the drawbacks of the basic MLI topologies. Some authors proposed multilevel topologies based on the concept of nested arrangement [13]. Such topologies are called nested multilevel converters, since the central point of the legs are connected at the same point, with the external legs involving the internal ones. Nested configurations present advantages as compared to the equivalent neutral point clamped topologies in terms of reduced number of diodes and consequently higher efficiency.

An emerging hybrid cascaded converter was developed by some authors [14]. It offers the dc side short circuit proof feature at reduced loss and footprint compared to the existing multilevel and other hybrid converters. Its operating principle, modulation, and capacitor voltage balancing strategies are described in detail in [14]. Furthermore, hybrid converter scalability to high voltage applications is investigated [14]. A new topology of cascaded multilevel inverter using a reduced number of switches, insulated gate driver circuits and reduced voltage standing on switches is proposed by some authors. The proposed topology results in reduction of installation area and cost, and has simplicity of control system [15]. Some authors presented a new class of three phase seven level inverter based on a multilevel DC link and a bridge inverter to reduce the number of switches [16]. In [17], a new multilevel converter topology was introduced, which can synthesize all possible additive and subtractive combinations of input DC levels in the output voltage waveform with fewer power electronic switches. An appropriate modulation scheme has also been proposed for low switching frequency operation of the proposed topology. A new group for multilevel converter that operates as symmetric and asymmetric state is presented in [18]. The proposed multilevel converter generates DC voltage levels similar to other topologies with less number of semiconductor switches. It results in the reduction of the number of switches, driver circuits, losses, installation area, and converter cost.

A new design and implementation of a three-phase hybrid multilevel inverter (MLI) using space vector modulation was presented by some authors [19]. The proposed MLI consists of a reduced number of dc sources and switches to minimize the control complexity. The developed topology consists of two stages: main stage and auxiliary stage. The main stage is a conventional three-phase inverter with one high-voltage input dc source and six switches. The auxiliary stages contain three individual cells. Each cell consists of two switches and one low-voltage input dc source. The special feature of the proposed system is its capability to maximize the number of voltage levels using a reduced number of isolated dc voltage sources and electronic switches.

The design and operational principles of a three-phase three-level nine switch voltage source inverter is described in [20]. The proposed topology consists of three bi-directional switches inserted between the source and the full-bridge power switches of the classical three-phase inverter. As a result, a three-level output voltage waveform and a significant suppression of load harmonic contents are obtained at the inverter output. Analytical solutions of PWM strategies for multilevel inverters are used to identify that alternative phase opposition disposition PWM for diode-clamped inverters produces the same harmonic performance as phase-shifted carrier PWM for cascaded inverters, and hybrid PWM for hybrid inverters, when the carrier frequencies are set to achieve the same number of inverter switch transitions over each fundamental cycle [21].

In [22], the various sinusoidal and trapezoidal reference PWM strategies like Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD), Carrier Overlapping (CO), and Variable Frequency (VF) were proposed for a three phase seven level inverter. A comprehensive analysis of various bipolar multicarrier PWM strategies with trapezoidal reference for three phase trinary source nine level cascaded inverter has been presented by some authors [23].

This paper suggests a modular configuration for the three phase symmetric multilevel voltage source inverter. This inverter can generate a great number of levels using lower number of circuit components. This paper is divided into various sections. The concept of proposed seventeen level inverter is presented in section

2. The switching scheme for the inverter is discussed in section 3. The concept of various PWM strategies is given in section 4. The simulation results and discussions are presented in section 5. This is followed by the conclusion in section 6.

## 2. Three phase symmetrical cascaded H-bridge seventeen level inverter

The proposed three phase symmetrical cascaded H-bridge seventeen level inverter having minimum number of switches with a three phase star connected resistive load of 50 Ω/phase is shown in Fig. 1. It consists of three-single phase inverters with 'n' number of isolated DC voltage sources ($E_1 = E_2 = E_3$, …., $= E_n = V_{DC}$) for each phase for producing 2n+1 levels. This inverter with 2n+2 switches is able to produce zero or positive and negative polarity voltages. Here, eight numbers of DC sources and eighteen numbers of switches are used for the proposed seventeen level inverter. It is a modular type and it can be extended for extra large number of output voltage levels by additional modular stages. Each switch is composed of Insulated Gate Bipolar Transistor (IGBT) with an anti-parallel diode. The switches in the left leg and right leg are complementary pairs which mean the switches $T_1$ and $T_1$' don't operate simultaneously. For symmetrical input, the voltage stress produced by switch pair ($T_1$, $T_1$') and ($T_{n+1}$, $T_{n+1}$') is equal to $V_{DC}$, whereas for all other switches, the voltage stress would be equal to $2V_{DC}$. For this inverter, always n+1=9 number of switches should be turned ON in various operating modes. The load voltage is equal to the sum of the output voltage of all the three legs that are connected in series. In this inverter, the number of switches used is reduced considerably compared to the conventional one and that of recently proposed [24]. The comparison of number of switches used in the proposed inverter with conventional one is shown in the Table 2.

Table 2 Comparison of power component requirements of proposed inverter with conventional inverter

| Inverter type | No. of DC sources | No. of Switches | No. of output levels | No. of on-state switches |
|---|---|---|---|---|
| Conventional cascaded MLI | n | 4n | 2n+1 | 2n |
| Cascaded MLI proposed in [24] | n | 2n+4 | 2n+1 | n+2 |
| Proposed cascaded MLI | n | 2n+2 | 2n+1 | n+1 |

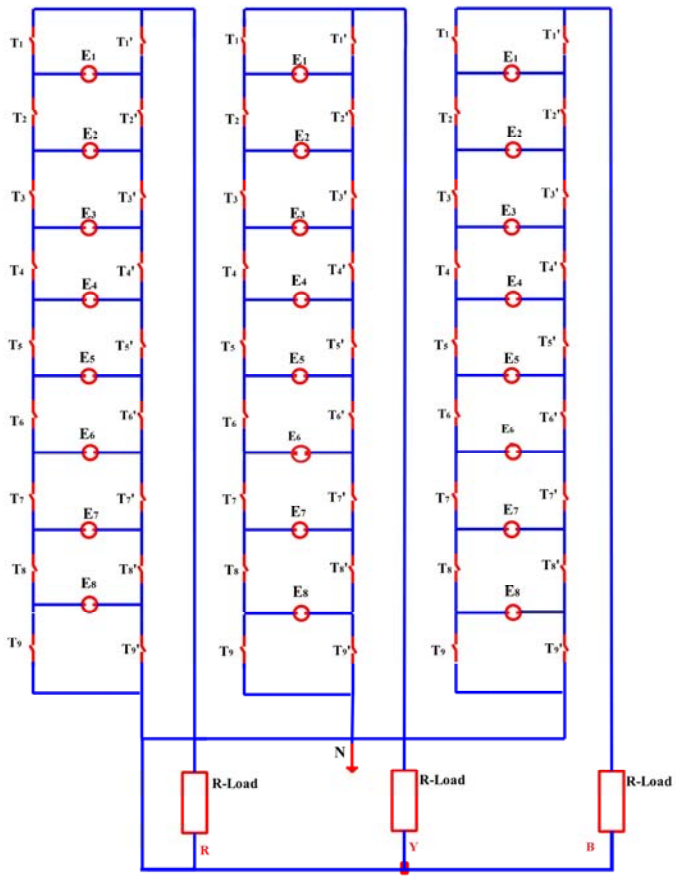

Fig. 1. The proposed three phase seventeen level inverter

## 3. Switching scheme for the proposed inverter

The proposed three phase symmetrical cascaded H-bridge seventeen level inverter consists of three-single phase inverters with each phase containing eight number of isolated DC voltage sources ($E_1 = E_2 = E_3 = E_4 = E_5 = E_6 = E_7 = E_8 = V_{DC}$) and nine pair of switches namely ($T_1$, $T_1$'), ($T_2$, $T_2$'), ($T_3$, $T_3$'), ($T_4$, $T_4$'), ($T_5$, $T_5$'), ($T_6$, $T_6$'), ($T_7$, $T_7$'), ($T_8$, $T_8$') and ($T_9$, $T_9$'). The bidirectional switches used are MOSFET / IGBT. The operations of different switches are shown in Table 3. It is understood from the Table 3 that at a time nine number of switches should be made on to get a particular output level. The seventeen level output voltages are $+8V_{DC}$, $+7V_{DC}$, $+6V_{DC}$, $+5V_{DC}$, $+4V_{DC}$, $+3V_{DC}$, $+2V_{DC}$, $+1V_{DC}$, $0V_{DC}$, $-1V_{DC}$, $-2V_{DC}$, $-3V_{DC}$, $-4V_{DC}$, $-5V_{DC}$, $-6V_{DC}$, $-7V_{DC}$ and $-8V_{DC}$. These stepped voltage levels form an approximate AC sinusoidal waveform.

## 4. Multicarrier sinusoidal PWM strategies

A number of PWM strategies are used in multilevel inverter power conversion applications. They are generally classified into three categories:

| Table 3 Switching table for the proposed seventeen level inverter | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sl. No. | Switching states | | | | | | | | | | | | | | | | | | Output voltages |
| | $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T_5$ | $T_6$ | $T_7$ | $T_8$ | $T_9$ | $T_1$' | $T_2$' | $T_3$' | $T_4$' | $T_5$' | $T_6$' | $T_7$' | $T_8$' | $T_9$' | |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | $+8V_{DC}$ |
| 2 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | $+7V_{DC}$ |
| 3 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | $+6V_{DC}$ |
| 4 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | $+5V_{DC}$ |
| 5 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $+4V_{DC}$ |
| 6 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | $+3V_{DC}$ |
| 7 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $+2V_{DC}$ |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $+1V_{DC}$ |
| 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $0V_{DC}$ |
| 10 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $-1V_{DC}$ |
| 11 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $-2V_{DC}$ |
| 12 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $-3V_{DC}$ |
| 13 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | $-4V_{DC}$ |
| 14 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | $-5V_{DC}$ |
| 15 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | $-6V_{DC}$ |
| 16 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | $-7V_{DC}$ |
| 17 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | $-8V_{DC}$ |

(i). Multistep staircase or fundamental switching frequency modulation strategy
(ii). Space vector PWM technique
(iii). Carrier based PWM technique

Under carrier based PWM, the level shifted multi carrier bipolar PWM technique has been used. The advantage of multicarrier PWM strategies is that it can be easily implemented to low voltage modules. In this technique, a triangular carrier signal is compared with sinusoidal reference waveform and the pulses obtained are used for switching of devices. This technique is used to reduce the THD of the output. There are various multicarrier bipolar PWM techniques. Of these techniques, Phase Disposition (PD), Variable Frequency (VF), and Carrier Overlapping (CO) PWM techniques are tried in this paper because of their advantages over the others.

The principle of PDPWM strategy is to use the several carrier signals with single modulating waveform. In Phase Disposition strategy, all the carriers are in phase and the carriers are disposed so that the bands they occupy are contiguous. For an m-level inverter, (m-1) carriers with same frequency $f_c$ and same peak-to-peak amplitude $A_c$ are used. The reference waveform has amplitude $A_m$ and frequency $f_m$, and is placed at zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices will be switched off. The modulation wave is centered in the middle of the carrier set. The frequency ratio $m_f$ is defined in the PWM strategy as follows:

$$m_f = \frac{f_c}{f_m} \tag{1}$$

The amplitude modulation index $m_a$ of this method is:

$$m_a = \frac{2A_m}{(m-1)A_c} \tag{2}$$

The multicarrier arrangement for PDPWM technique is shown in Fig. 2, for $m_a = 0.9$ and $m_f = 40$.

In Variable Frequency PWM (VFPWM) technique, sixteen carrier signals with same amplitude and variable frequency are used to generate seventeen level output. The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as

illustrated in Fig. 3 in which the carrier frequency of the intermediate switches is properly increased to balance the number of switchings for all the switches. For intermediate switches, $m_f$ = 80, and for all other switches, $m_a = 0.9$ and $m_f = 40$.

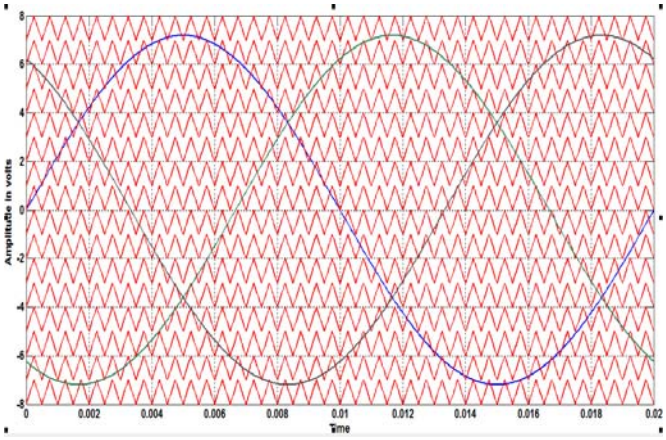


Fig. 2. Sine reference and carrier waveform arrangement for PDPWM strategy

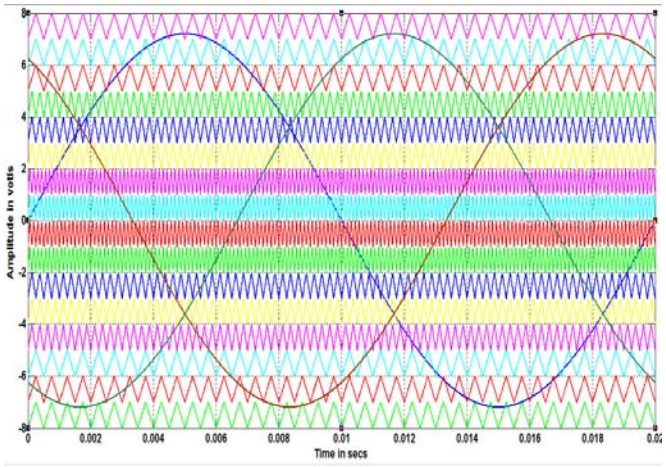


Fig. 3. Sine reference and carrier waveform arrangement for VFPWM strategy

In Carrier Overlapping PWM (COPWM) technique, 'm' level inverter requires (m-1) carriers with the same frequency $f_c$ and same peak-to- peak amplitude $A_c$. The (m-1) carriers are disposed such that the bands they occupy overlap each other as shown in Fig. 4. The overlapping vertical distance between each carrier is $A_c / 2$. The reference waveform has amplitude $A_m$ and frequency $f_m$ and it is centered in the middle of the carrier signals. The multicarrier arrangement for COPWM strategy is shown in Fig. 4 for $m_a$ = 0.9 and $m_f$ = 40. The amplitude modulation index for carrier overlapping PWM technique is:

$$m_a = \frac{A_m}{0.25 m A_c} \tag{3}$$

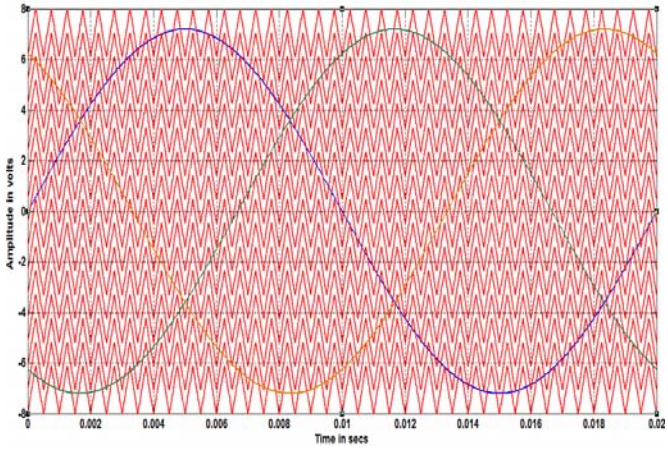


Fig. 4. Sine reference and carrier waveform arrangement for COPWM strategy

## 5. Simulation results and discussion

The proposed three phase seventeen level inverter is simulated in Matlab/Simulink environment using Power System block set. The bipolar multicarrier sinusoidal PWM strategies are used for developing switching signals for the inverter. The proposed PWM techniques are PDPWM, COPWM and VFPWM with sinusoidal wave reference. The frequency of the sine wave is $f_m$ = 50 Hz and that of triangular carrier signal is $f_c$ = 2 kHz for $m_a$ = 40 and $f_c$ = 4 kHz for $m_a$ = 80 in case of VFPWM technique.

The simulations are performed for $m_a$ = 0.9 and $m_a$ = 1. The simulated output waveforms of both the phase voltage and line voltage for the three phase cascaded seventeen level inverter and the corresponding FFT plots for a sample value of $m_a = 0.9$ only are shown in Figs. 5-16. The corresponding % Total Harmonic Distortion (%THD) is measured using the FFT block and their values are given in Table 4. The Table 4 also shows the values of $V_{RMS}$ of fundamental and $V_{PEAK}$ of inverter output for $m_a = 0.9$ and $m_a$ = 1. It is verified through simulation that the better performance of the inverter is obtained for the values of modulation index $m_a \geq 0.9$.

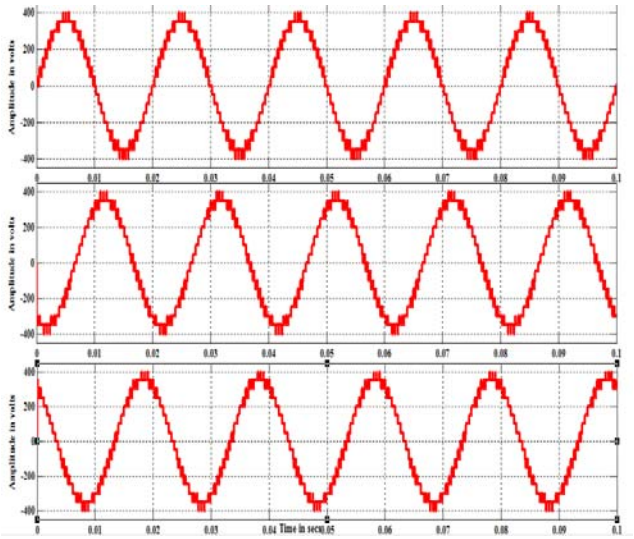


Fig. 5. Seventeen level inverter output phase voltage generated by PDPWM strategy

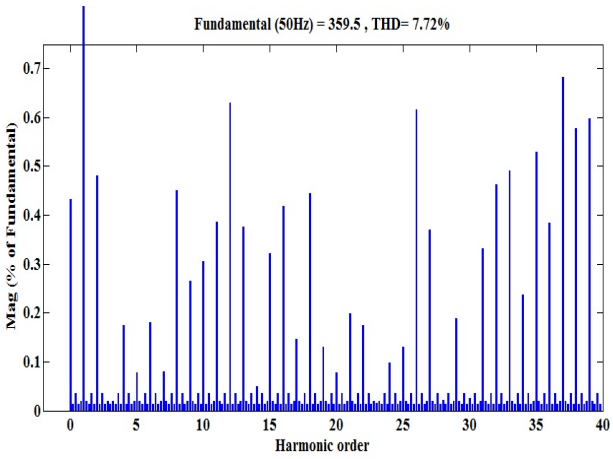


Fig. 6. FFT plot for seventeen level inverter output phase voltage of PDPWM strategy

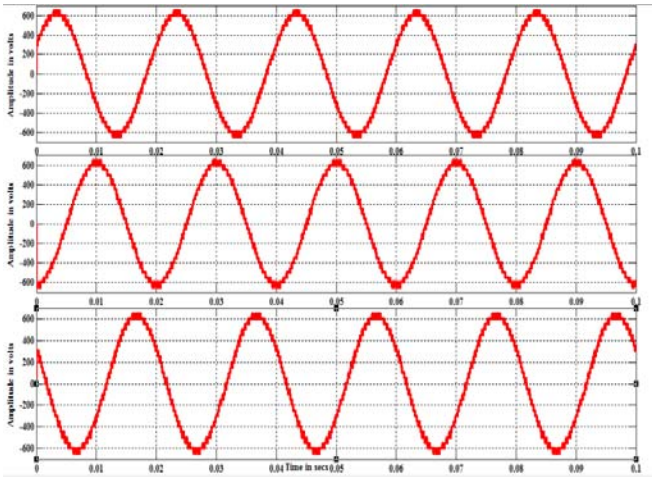


Fig. 7. Seventeen level inverter output line voltage generated by PDPWM strategy

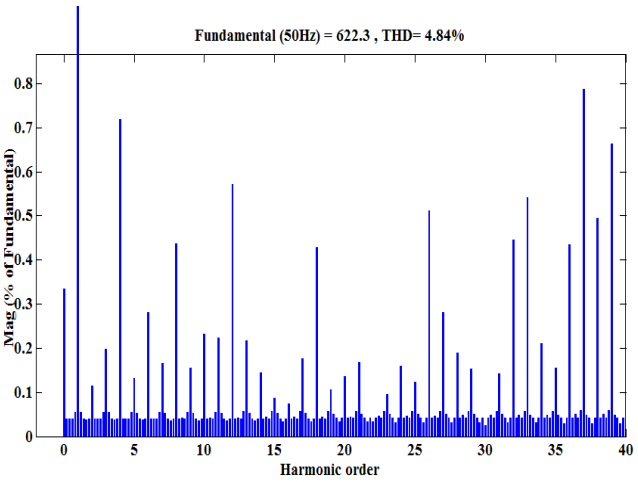


Fig. 8. FFT plot for seventeen level inverter output line voltage of PDPWM strategy

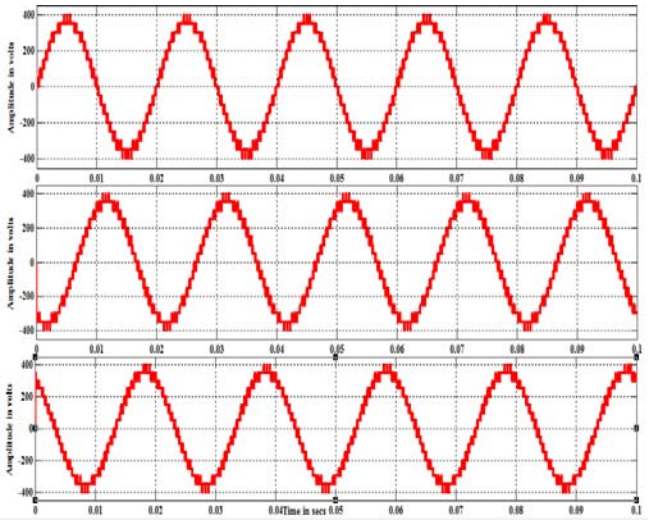


Fig. 9. Seventeen level inverter output phase voltage generated by VFPWM strategy

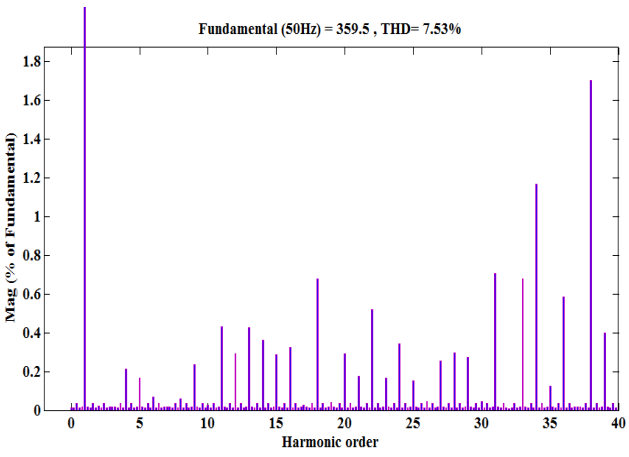


Fig. 10. FFT plot for seventeen level inverter output phase voltage of VFPWM strategy

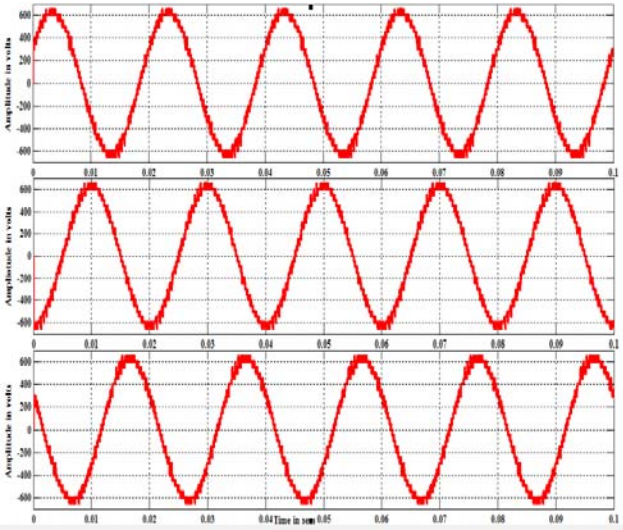

Fig. 11. Seventeen level inverter output line voltage generated by VFPWM strategy

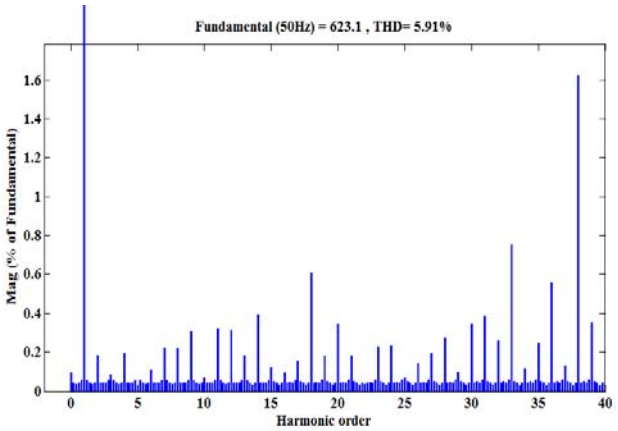


Fig. 12. FFT plot for seventeen level inverter output line voltage of VFPWM strategy

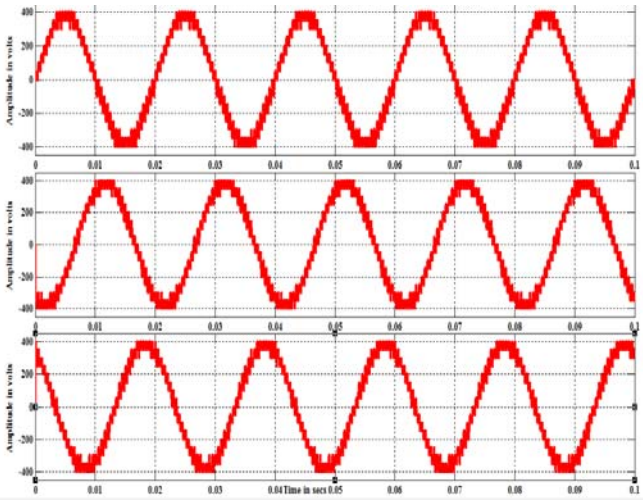

Fig. 13. Seventeen level inverter output phase voltage generated by COPWM strategy

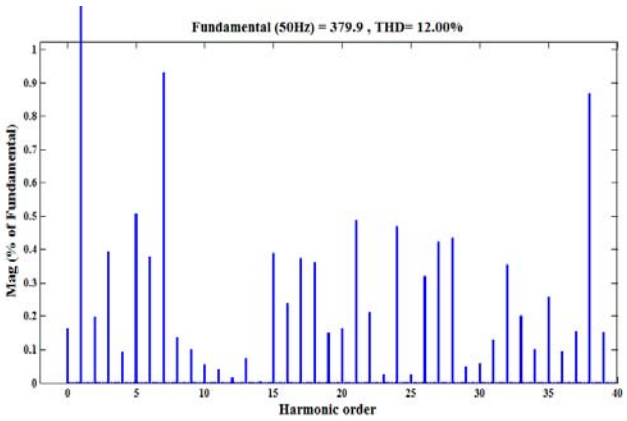


Fig. 14. FFT plot for seventeen level inverter output phase voltage of COPWM strategy

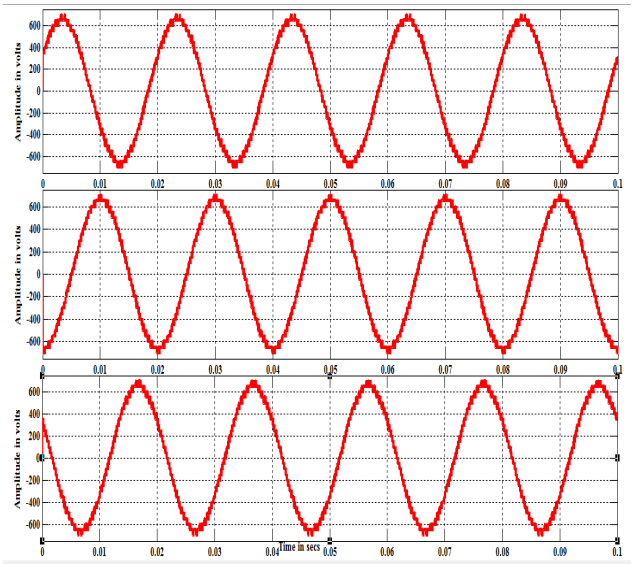

Fig. 15. Seventeen level inverter output line voltage generated by COPWM strategy

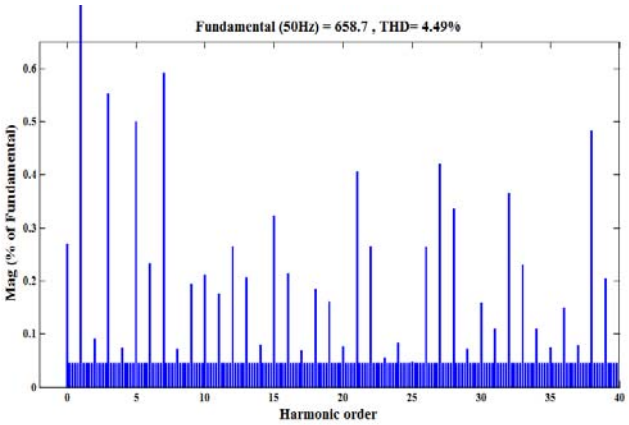


Fig. 16. FFT plot for seventeen level inverter output line voltage of COPWM strategy

Table 4 Comparison of performance factors for various sinusoidal PWM strategies

| Performance factors | Sinusoidal PWM strategies | | | | | |
|---|---|---|---|---|---|---|
| | PDPWM | | COPWM | | VFPWM | |
| | $m_a$= 0.9 | $m_a$=1 | $m_a$= 0.9 | $m_a$=1 | $m_a$= 0.9 | $m_a$=1 |
| %THD for phase voltage | 7.72 | 7.0 | 12 | 10.12 | 7.53 | 7.03 |
| %THD for line voltage | 4.84 | 4.14 | 4.49 | 5.26 | 5.91 | 5.33 |
| $V_{RMS}$ for phase voltage (V) | 359.5 | 399.5 | 379.9 | 414.6 | 359.5 | 400 |
| $V_{RMS}$ for line voltage (V) | 622.3 | 691.8 | 658.7 | 717 | 623.1 | 692 |
| $V_{PEAK}$ for phase voltage (V) | 508.4 | 564.9 | 537.2 | 586.3 | 508.4 | 565.7 |
| $V_{PEAK}$ for line voltage (V) | 880.1 | 970.3 | 931.5 | 1014 | 881.7 | 978.6 |

From the Table 4, it is observed that the harmonic contents of phase voltage and line voltage waveforms are found to be minimum in PDPWM strategy for the modulation index $m_a = 1$. The $V_{RMS}$ of fundamental and $V_{PEAK}$ of inverter output for both phase and line values are found to be maximum in COPWM strategy for the modulation index $m_a = 1$.

## 6. Conclusion

In this paper, various multicarrier sinusoidal PWM strategies such as PDPWM, COPWM, and VFPWM have been presented for the chosen three phase symmetrical cascaded H-bridge seventeen level inverter topology. The time domain simulations have been carried out in Matlab/Simulink platform and the results validate the effectiveness of the chosen sinusoidal PWM strategies in improving the performance of the proposed inverter. The various performance factors like %THD, $V_{RMS}$, and $V_{PEAK}$ have been calculated and analyzed. It is observed that the PDPWM method provides lower %THD than the other methods, and the COPWM method provides relatively higher values of RMS and peak voltages for high value of modulation index (Table 4). According to the requirement of performance measure, the appropriate PWM methods may be selected and employed for a particular application of the proposed inverter. The proposed topology utilizes the reduced number of power switches compared to the conventional MLI topologies. However, the proposed topology has the limitation of isolated DC sources requirement.

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