NEW ASYMMETRIC SEVEN LEVEL INVERTER WITH MINIMUM NUMBER OF VOLTAGE SOURCES AND SWITCHES

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Abstract: *The main objective of this paper is to propose a new single phase asymmetrical type seven level inverter with minimum number of DC voltage sources and switches. The proposed multilevel inverter consists of two parts namely, level creator part which generate positive levels of outputs and polarity changing part which helps to change the polarity of the output voltage. The proposed inverter consist of two DC voltage sources, three main switches and four switches of H-bridge inverter to generate seven level output. Different methods used to calculate the switching angles are presented and the results are compared. The simulation is performed using MATLAB/SIMULINK software to verify the function of the proposed inverter.*

Key words: *Seven level, inverter, Switching angle, Asymmetric, THD.*

1. Introduction

In 1975, the concept of multilevel inverters is introduced which began with basic three-level converter topology [1]. The multilevel inverter synthesize the staircase output voltage from the several independent DC voltage sources. It enables the use of renewable energy resources as inputs. T advantages of multilevel inverter includes low distortion, robustness, high power quality, low dv/dt stress, minimum switching losses, better electromagnetic interference and ease of control [2]. The conventional topologies of multilevel inverters are diode-clamped, flying capacitor and cascaded H-bridge inverters[2-6]. The multilevel inverter can be symmetric or asymmetric. If all the voltage sources are of same magnitude, then it is called as symmetric inverter. On other hand, if the voltage sources have different magnitude, then it is known as asymmetric inverter. The major drawback of the multilevel inverter is it requires greater number of power electronic switches and associated gate driver circuit to achieve higher output levels.

To overcome these drawbacks, many researchers has focused on developing new topologies of multilevel inverters, novel pulse-width modulation (PWM) techniques and improved control techniques to improve the performance. The major drawback of this inverter topology is it have different structure for even and odd number of DC voltage sources. Rodríguez et al presented the control and modulation methods for diode-clamped inverter, capacitor-clamped inverter, and cascaded multicell inverter with separate DC sources [7]. Sirisukprasert S. et al [8] proposed a modulation technique for multilevel voltage source converters suitable for high-voltage power supplies and flexible ac transmission system devices. The switching devices of the main power stage switch only once per cycle for all modulation index. Babaei E. et. al. proposed the asymmetric multilevel inverter in Ref. [9]. This inverter have the capability to bypass or conduct the DC voltage sources separately to generate the desired voltage levels. A single and double source sub-multilevel inverter has been proposed in Ref. [10]. A single phase symmetrical type seven level inverter is proposed in [11]. But this inverter topology uses six switches and three DC voltage sources to produce seven level output voltage. Another multilevel inverter topology for inductor motor drive applications has been proposed in Ref. [12]. This inverter topology uses 9 switches and 3 voltage sources to generate seven level output during symmetrical mode of operation. Gnana Prakash et. al. proposed a multilevel inverter with reduced number of switches in Ref. [13]. The proposed method is suitable for a high power application and it built with three DC sources and six switches.

This paper proposes a new multilevel inverter with reduction in number of power electronic switches and DC sources. The proposed inverter produces seven level output voltage with minimum THD using seven switches and two DC sources. Section-2 describes the modes of operation of the proposed inverter. The different methods of calculating the switching angles are presented in section-3. The simulation results are discussed in Section-4. The conclusion are presented in section-5.

2. Proposed Multilevel Inverter

The proposed multilevel inverter is shown in Fig. 1.

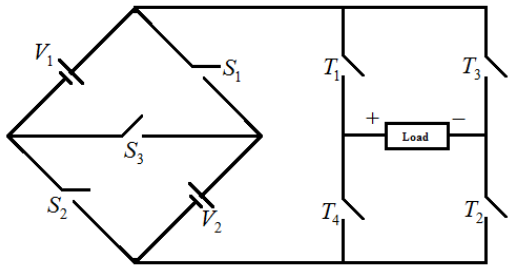
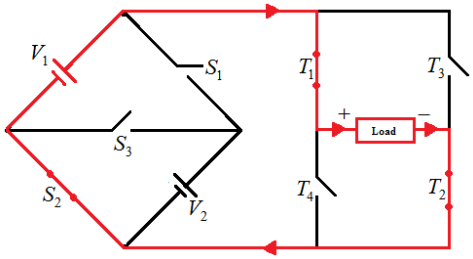


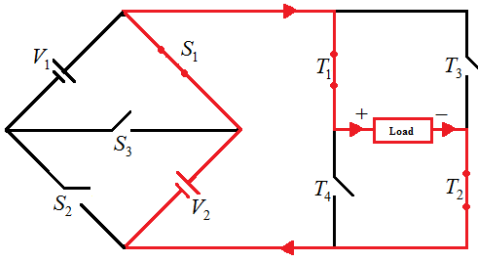
Fig. 1. Proposed topology of Multilevel Inverter

The proposed inverter consists of two parts: (1) level creator part and (2) polarity changing part. The level creator unit consist of 2 DC voltage sources and 3 main switches. This level creator part helps to produce unidirectional output voltage with various voltage levels as 0, V_{dc} and $2V_{dc}$. The magnitude of each DC voltage sources are different and hence it is known as an "Asymmetric inverter". The conventional H-bridge inverter acts as a polarity changing part which helps to convert the unidirectional output voltage of the level creator part into bidirectional output voltage. When the switches T_1 and T_2 are ON, positive levels of voltages are obtained. Similarly, negative levels of voltages are obtained when the switches T_3 and T_4 are ON.

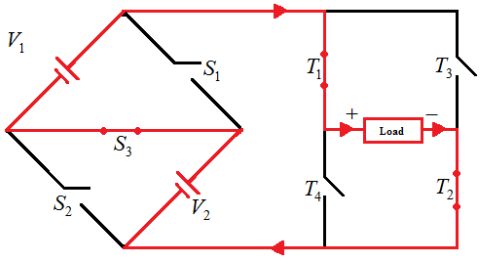
The different modes of operation of the proposed multilevel inverter are shown in Fig. 2.



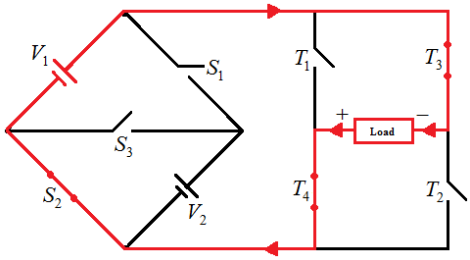
(a) Mode -1



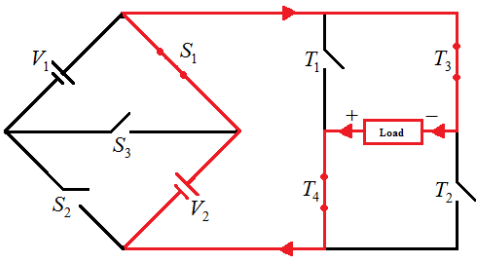
(b) Mode - 2



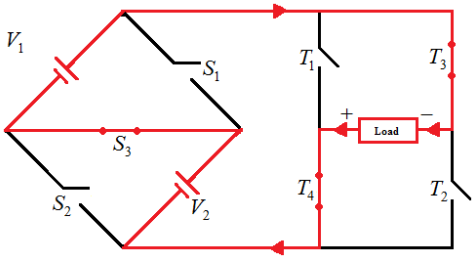
(c) Mode - 3



(d) Mode - 4



(e) Mode - 5



(f) Mode - 6

Fig. 2. Modes of operation

In mode-1, the switches S_2, T_1 and T_2 are ON and hence the voltage V_1 is obtained across the load. During mode-2, the switches S_1, T_1 and T_2 are ON and the voltage V_2 is obtained. The switches S_3, T_1 and T_2 are ON during the mode-3 operation and the voltage $V_1 + V_2$ is obtained. The mode-1, 2 and 3 are positive modes of operation where the voltages obtained are positive. The mode-4, 5 and 6 are negative modes of operation since the obtained voltages are negative. In mode-4, the switches S_2, T_3 and T_4 are ON and hence the voltage $-V_1$ is obtained across the load. During mode-5, the switches S_1, T_3 and T_4 are ON and the voltage $-V_2$ is obtained. The switches S_3, T_3 and T_4 are ON during the mode-6 operation and the voltage $-(V_1 + V_2)$ is obtained.

The switching states of the proposed multilevel inverter is given in Table 1.

Table 1
Switching states

S. No	S_1	S_2	S_3	T_1	T_2	T_3	T_4	Voltage
1	0	0	1	1	1	0	0	$V_1 + V_2 = 3V_{dc}$
2	1	0	0	1	1	0	0	$V_2 = 2V_{dc}$
3	0	1	0	1	1	0	0	$V_1 = V_{dc}$
4	x	x	x	1	0	1	0	0
5	0	0	1	0	0	1	1	$-V_1 = -V_{dc}$
6	1	0	0	0	0	1	1	$-V_2 = -2V_{dc}$
7	0	1	0	0	0	1	1	$-(V_1 + V_2) = -3V_{dc}$

The comparison of the output voltage levels with the number of DC voltage sources and the number of switches for different topologies of multilevel inverter are given in Table 2.

Table 2
Comparison of different Multilevel Inverters

Inverter	Number of DC Sources	Number of Switches	Number of level
Diode Clamped inverter	6	12	7
Flying Capacitor inverter	6	12	7
Cascaded H-bridge inverter	3	12	7
Ref. [1]	2	5	5
Ref. [11]	3	6	7
Ref. [12]	3	9	7
Ref. [13]	3	6	7
Proposed inverter	**2**	**7**	**7**

From the above table, it is clear that the proposed multilevel inverter uses minimum number of switches and DC voltage sources to achieve seven level output voltage.

3. Switching Angle Calculation

Switching angles has an important role in the reduction of total harmonic distortion (THD). There are 2(n-1) switching angles has to be determined for 'n' level inverter[14]. The switching angles corresponding to the period 0 to π/2 are called as main switching angles. An 'n' level inverter has (n-1)/2 main switching angles. It is enough to determine the (n-1)/2 main switching angles and the other switching angles are obtained from the main switching angles using the following relations [14]:

1. For period 0 to π/2
   = $\theta_1, \theta_2, \ldots, \theta_{(n-1)/2}$.
2. For period π/2 to π
   = $\theta_{(n+1)/2}. . ., \theta_{(n-1)}. = (\pi-\theta_{(n-1)/2}),. . .,(\pi-\theta_1)$.
3. For period π to 3π/2
   = $\theta_n, . . ., \theta_{3(n-1)/2} = (\pi+\theta_1),. . .,(\pi+\theta_{(n-1)/2})$.
4. For period 3π/2 to 2π
   = $\theta_{(3n-1)/2}, . . ., \theta_{2(n-1)} = (2\pi-\theta_{(n-1)/2}),. . .,(2\pi-\theta_1)$.

The switching angles of n-level inverter is shown in Fig. 3. The different methods of calculating switching angles are given below:

Method - 1

$$\theta_j = j\frac{180^0}{n} \text{ where, } j = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 2

$$\theta_j = j\frac{180^0}{n+1} \text{ where, } j = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 3

$$\theta_j = \frac{1}{2}\sin^{-1}\left(\frac{2j-1}{n-1}\right) \text{ where, } j = 1,2,...,\left(\frac{n-1}{2}\right)$$

Method - 4

$$\theta_j = \sin^{-1}\left(\frac{2j-1}{n-1}\right) \text{ where, } j = 1,2,...,\left(\frac{n-1}{2}\right)$$

For the proposed multilevel inverter, there are three main switching angles and are determined using the above mentioned methods are given in Table 3.

Table 3
Switching Angles

Angle	Main Switching Angles (in degree)			
	Method- 1	**Method- 2**	**Method- 3**	**Method- 4**
θ_1	25.7143	22.5	4.797	9.5941
θ_2	51.4286	45	15	30
θ_3	77.1429	67.5	28.2213	56.4427

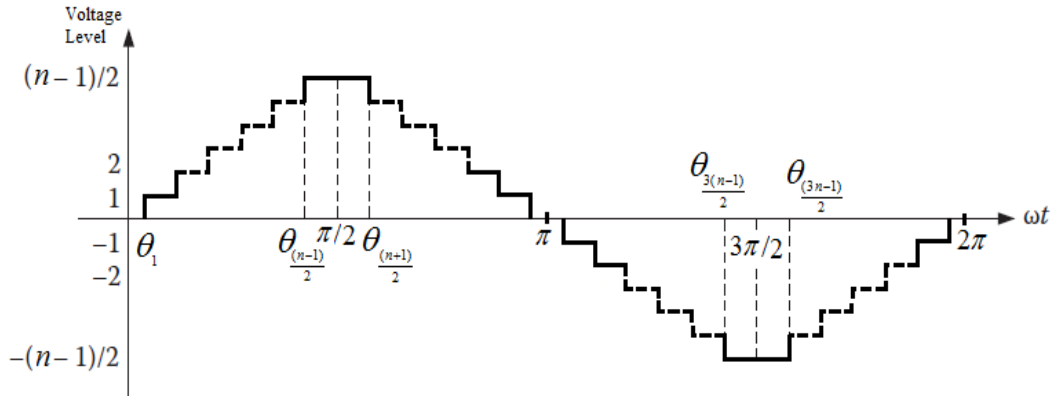
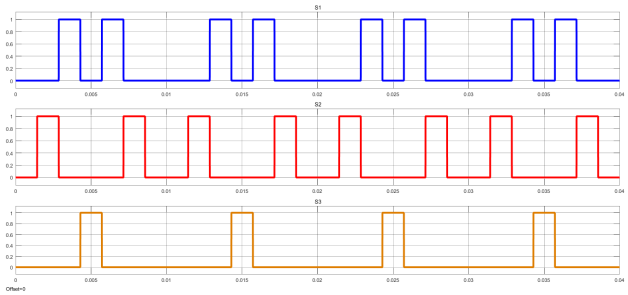
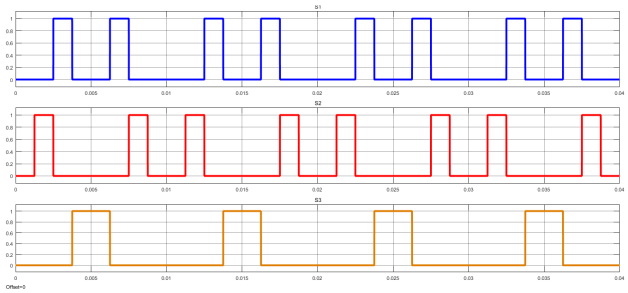


Fig. 3. Output Voltage with switching angles of 'n' level inverter

The switching pulses generated using the different methods are shown in Fig. 4.



(a)



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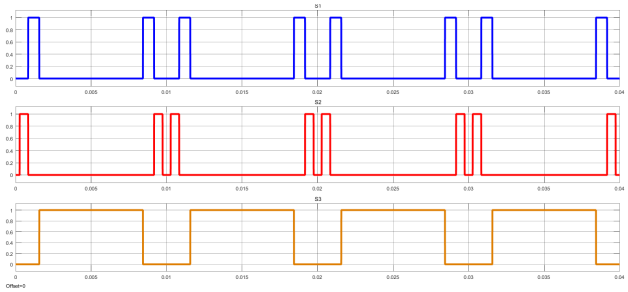

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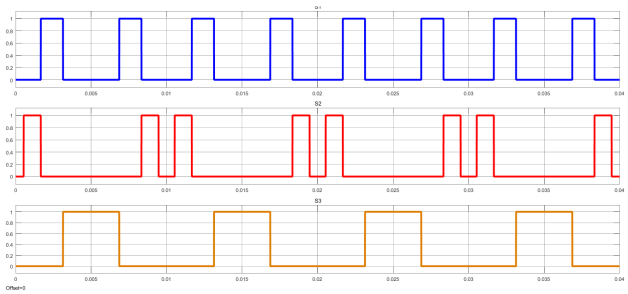
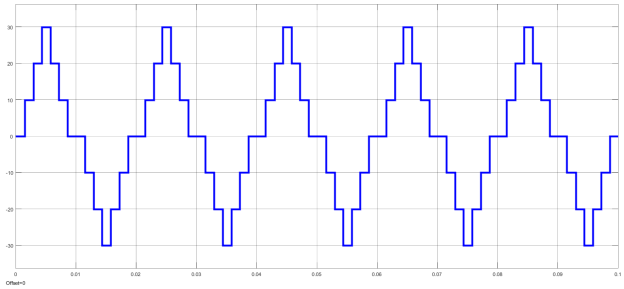


(d)

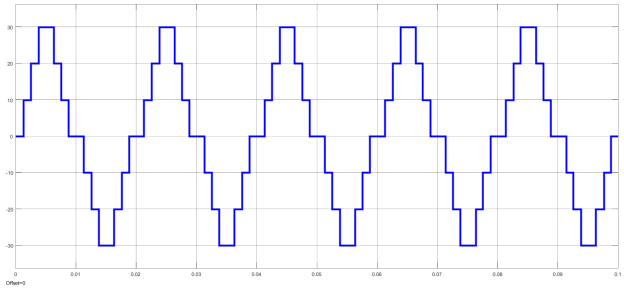
Fig. 4. Gate pulses generated using (a) Method - 1 (b) Method - 2 (c) Method - 3 and (d) Method - 4

4. Simulation Results

The simulation results are presented in this section. The different voltage sources have values $V_1 = V_{dc} = 10V$ and $V_2 = 2V_{dc} = 20V$. The maximum output voltage obtained is 30V (i.e. V_1+V_2). The output voltage of the proposed seven level inverter for different methods are shown in Fig. 5. The output voltage has 7 levels (i.e., 3 positive, 3 negative and 1 zero).



(a)



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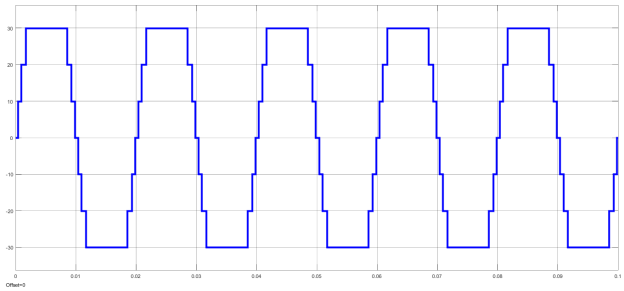

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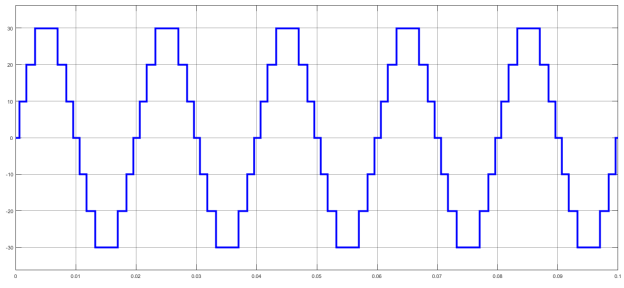
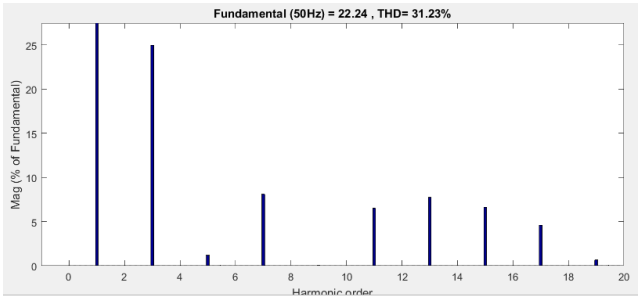


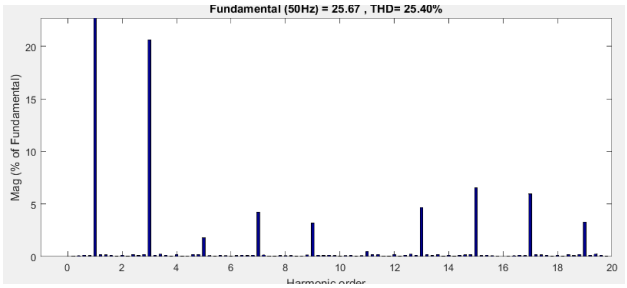
(d)

Fig. 5. Output Voltage (a) Method - 1 (b) Method - 2 (c) Method -3 and (d) Method - 4.

The FFT analysis of the output voltage of the proposed seven level inverter for different methods are shown in Fig. 6. The result shows that the method - 4 gives the output voltage similar to the sinusoidal output with minimum THD of 12.17% corresponding to the fundamental output voltage of 30.64 V.



(a)



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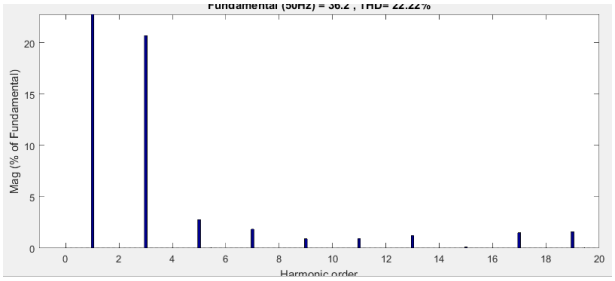

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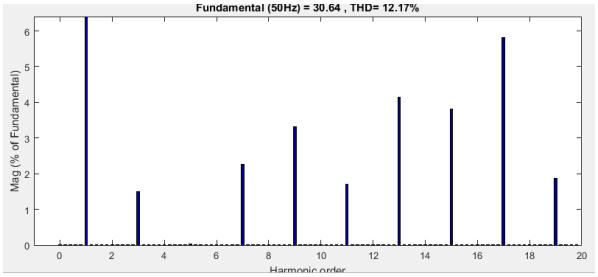

(d)

Fig. 6. FFT Analysis (a) Method - 1 (b) Method - 2 (c) Method - 3 and (d) Method - 4

Table 4 shows the comparison of the THD of the output voltage waveform and fundamental output voltage obtained using different methods.

Table 4
Comparison of THD and Fundamental output voltage

Method	THD (%)	Fundamental output Voltage (V)
Method - 1	31.23	22.24
Method - 2	25.40	25.67
Method - 3	22.22	36.2
Method - 4	**12.17**	30.64

The above table shows that the proposed seven level inverter achieves minimum THD and higher output level with minimum number of voltage sources and switches.

Table 5 shows the comparison of the THD of the output voltage waveform with the available references.

Table 5
Comparison of THD

THD	Ref[2]	Ref[3]	Proposed
THD (%)	17.76	17.27	12.17

The above table shows that the proposed seven level inverter achieves minimum THD as compared with the references.

5. Hardware setup

This hardware setup of the proposed seven level inverter is shown in Fig. 7.

Fig. 7. Proposed topology of Multilevel Inverter

The gate pulses are generated using PIC16F87XA. The operating frequency of PIC16F87XA is 20 MHz. The output of the inverter is observed using CRO. The experimental results justify the simulated response and the practical feasibility of the proposed seven level inverter topology for use in the field.

6. Conclusion

This paper proposed a new topology of seven level inverter with minimum number of components. The proposed inverter achieves seven level output voltage with 2 DC voltage sources, 3 main switches and 4 H-bridge switches. Each voltage sources have different voltage magnitudes. The four methods of calculating the switching angles are presented. A comparison of the proposed inverter topology with other existing topologies is presented in this paper. The performance of the proposed inverter is analysed

using MATLAB software and the result exhibit the good performance and feasibility of the proposed inverter. The result shows that maximum voltage obtained is 3Vdc =30 V and the method - 4 achieves minimum THD of the output voltage waveform.

References

[1] Baker, R. H. and Bannister, L. H.: *Electric Power Converter*. In: U.S. Patent 3 867 643, Feb. 1975.

[2] Boora, A. A., Nami, A., Zare, F., Ghosh, A. and Blaabjerg, F.: *Voltage sharing converter to supply single-phase asymmetric four-level diode clamped inverter with high power factor loads.* In: IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507–2520, Oct. 2010.

[3] Khazraei, M., Sepahvand, H., Corzine, K. A. and Ferdowsi, M.: *Active Capacitor Voltage Balancing in Single-Phase Flying-Capacitor Multilevel Power Converters.* In:IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 769-778, Feb. 2012.

[4] Rodriguez, J., Bernet, S., Steimer, P. and Lizama, I.: *A survey on natural point clamped inverters.* In: IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[5] Ding, K., Cheng, K. W. E., and Zou, Y. P.: *Analysis, of an asymmetric modulation methods for cascaded multilevel inverters*. In. IET Power Electron., vol. 5, no. 1, pp. 74–85, Jan. 2012.

[6] Babaei, E., Kangarlu, M. F., Sabahi, M. and Alizadeh Pahlavani, M. R.: *Cascaded multilevel inverter using sub-multilevel cells.* In. Electr. Power Syst. Res., vol. 96, pp. 101–110, Mar. 2013.

[7] José Rodríguez, Jih-Sheng Lai and Fang Zheng Peng: *Multilevel Inverters: A Survey Topologies, Controls, and Applications*. In: Proceedings of the IEEE Transactions on Industrial Electronics, July 2002, Vol. 49, no. 4, pp. 724 - 738.

[8] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu: *Optimum harmonic reduction with a wide range of modulation indices for multilevel converters*. In: Proceedings of the IEEE Transactions on Industrial Electronics, Aug 2002, vol. 49, no. 4, pp.875– 881.

[9] Babaei, E., Kangarlu, M. F. and Mazgar, F.N: *Symmetric and asymmetric multilevel inverter topologies with reduced switching devices*. In: Electric Power Systems Research, Vol.86, pp122–130, 2012.

[10] Ramani, K., Sathik ,M. A. J., and Sivakumar, S.: *A New Symmetric Multilevel Inverter Topology Using Single and Double Source Sub-Multilevel Inverters.* In: Journal of Power Electronics, Vol. 15, No. 1, pp. 96-105, January 2015.

[11] Venkataramanan K., Shanthi B., and Sivakumaran T.S.: *Investigations on Inverted Sine PWM Strategies for Symmetric Multilevel Inverter.* In: Journal of Electrical Engineering, Vol. 16, No. 3, pp. 83-88, 2016.

[12] Prasadarao V. S., and Malligunta Kirankumar.: *Simulation of a Novel Multilevel Inverter Topology for Induction Motor Drive Applications.* In: Journal of Electrical Engineering, Vol. 15, No. 1, pp. 280-286, 2015.

[13] Gnana Prakash M, Balamurugan M, Umashankar S.: A *New Multilevel Inverter with Reduced Number of Switches.* In: International Journal of Power Electronics and Drive System, Vol. 5, pp. 60-70, 2014.

[14] Luo F. L. and Ye H.: *Advanced DC/AC Inverters*. In: CRC Press LLC, 2013.. ISBN: 978-1-4665-1138-5.