SIMULATION ANALYSIS AND EXPERIMENTAL VALIDATION OF SYMMETRICAL AND ASSYMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTERS FOR PV APPLICATION

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Abstract: A solar inverter or PV inverter converts the variable direct current (DC) output of a photovoltaic (PV) solar panel into a utility frequency alternating current (AC) that can be fed into a commercial electrical grid or used by a local, off-grid electrical network. It is a critical component in a photovoltaic system, allowing the use of ordinary commercial appliances. Solar inverters have special functions adapted for use with photovoltaic arrays, including maximum power point tracking and anti-islanding protection. This paper deals with symmetrical five level inverter topology along with asymmetrical seven and nine-level inverter topologies for photo-voltaic systems. This paper explains the simplified method to generate gate pulses for the inverter topologies. With this type of simple logic circuit for generation of pulses, the number of snubber circuits becomes less. The number of gate drives will also become less and the control strategy is very easy to implement. The inverter type Hybrid H-Bridge produces greater voltage levels while using less number of switching devices. Reducing the number of switches also reduces switching losses and THD. The results were developed using Matlab/Simulink and these results were validated with hardware comparisons.

Keywords: cascaded H-bridge (CHB), Photovoltaic (PV), Hybrid H-Bridge inverter, Switching devices, THD, Switching losses.

I. INTRODUCTION

A photovoltaic array (also called a solar array) consists of multiple photovoltaic modules, casually referred to as solar panels, to convert solar radiation (sunlight) into usable direct current (DC) electricity. A photovoltaic system for residential, commercial, or industrial energy supply normally contains an array of photovoltaic (PV) modules, one or more DC to alternating current (AC) power converters (also known as inverters), a tracking system that supports the solar modules, electrical wiring and interconnections, and mounting for other components. Optionally, a photovoltaic system may include any or all of the following: renewable energy credit revenue-grade meter, maximum power point tracker (MPPT), battery system and charger, GPS solar tracker, energy management software, solar concentrators, solar irradiance sensors, anemometer, or task-specific accessories designed to meet specialized requirements for a system owner [1-2]. The number of modules in the system determines the total DC watts capable of being generated by the solar array; however, the inverter ultimately governs the amount of AC watts that can be distributed for consumption. A photovoltaic array (or solar array) is a linked collection of solar panels. The power that one module can produce is seldom enough to meet requirements of a home or a business, so the modules are linked together to form an array. Most PV arrays use an inverter to convert the DC power produced by the modules into alternating current that can power lights, motors, and other loads [2-4]. The modules in a PV array are usually first connected in series to obtain the desired voltage; the individual strings are then connected in parallel to allow the system to produce more current.

A solar inverter or PV inverter converts the variable direct current (DC) output of a photovoltaic (PV) solar panel into a utility frequency alternating current (AC) that can be fed into a commercial electrical grid or used by a local, off-grid electrical network. Photovoltaic (PV) inverters become more and more widespread within both private and commercial circles. These grid-connected inverters convert the available direct current supplied by the PV panels and feed it into the utility grid [5-6]. There are many different power circuit topologies and control strategies used in inverter designs [7-10]. Different design approaches address various issues that may be more or less important depending on the way that the inverter is intended to be used. Normally the conventional H-bridge inverter produces a square output, which contains infinite number of odd harmonics and dv/dt stress is also high. Normal PWM inverter can reduces the THD, but switching losses are high and also this inverter is restricted to low power applications [11-13]. A relatively new class called multilevel inverters has gained widespread interest. Normal operation of CSIs and VSIs

can be classified as two-level inverters because the power switches connect to either the positive or the negative DC bus. If more than two voltage levels were available to the inverter output terminals, the AC output could better approximate a sine wave. For this reason multilevel inverters, although more complex and costly, offer higher performance [14-16].

II. MULTI-LEVEL INVERTER

Nowadays, multilevel inverters have become more attractive for their use in high-voltage and high-power applications. In multilevel inverters, the desired output voltage is achieved by suitable combination of multiple low dc voltage sources used at the input side. As the number of dc sources is increased, the output voltage becomes closer to a sinusoidal waveform. Some advantages of multi-level inverters are good power quality, low switching losses and electromagnetic compatibility due to the low dv/dt transitions. Some of the fundamental multilevel topologies include the cascaded H-bridge structures, flying capacitor and diode-clamped converter. Other proposed configurations for multilevel converters are mainly derived from these three basic topologies. Among these three topologies, cascaded multilevel converter has got more attention in literatures. This paper particularly focuses on cascaded multilevel converters. This topology is divided into two symmetrical and asymmetrical structures. If all dc voltage sources are equal, then the inverter is called as symmetrical multilevel inverter, otherwise as an asymmetrical multilevel inverter. In asymmetrical multilevel inverters, the number of produced output voltage levels is high when compared to symmetrical multilevel inverter with the same number of dc-voltage sources and switches. One of the main challenges in multilevel inverters is to reduce the number of power electronic switches while considering operational conditions.

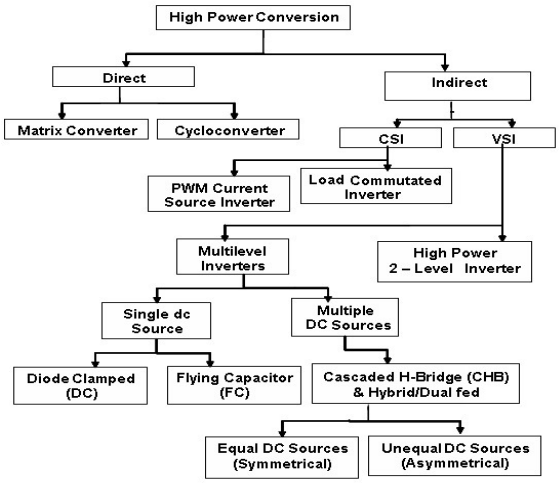

Fig. 1 Classification of High power Converters

Fig. 1 shows the classification of high power converters. Out of all converters Cascaded bridge configuration is more popular. Cascaded bridge configuration is again classified into 2 types 1) Cascaded Half Bridge 2) Cascaded Full Bridge or Cascaded H-Bridge.

A. Cascaded H-Bridge Five level Inverter:

The structure of five-level single-phase cascade H-Bridge inverter is shown in Fig. 2. In conventional structure DC link voltage is shared equally among the DC voltage sources and should be regulated to the equal value at $V_{dc}/2$ if DC voltage across two voltage sources is boosted to V_{dc}. As it is clear, five output voltage levels can be generated based on different switching states.

Table 1: Output voltage according to switching ON-OFF condition for a symmetrical five level inverter

S1	S2	S3	S4	S5	S6	S7	S8	V_O
ON	OFF	OFF	ON	ON	OFF	OFF	ON	V_{dc}
ON	OFF	OFF	ON	OFF	ON	OFF	ON	$V_{dc}/2$
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{dc}/2$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	$-V_{dc}$

B. Cascaded H-Bridge Asymmetrical seven level Inverter:

A seven level cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H1consists of a separate DC source $V_{dc}/3$, whereas the second H-Bridge H2 consists of a dc source $2V_{dc}/3$ as shown in Fig. 2. Let the output of H-Bridge-1 be denoted as $V_1(t)$ and the output of H-Bridge-2 be denoted as $V_2(t)$. Hence the total output voltage is given by $V(t) = V_1(t) + V_2(t)$. By alternate closing and opening of different switching configurations we can get different voltage levels.

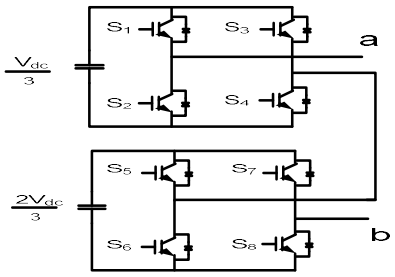

Fig. 2 cascaded H-bridge Asymmetrical seven level Inverter

Fig. 2 shows the cascaded seven level H-Bridge inverter circuit and Table 2 gives the corresponding output voltages

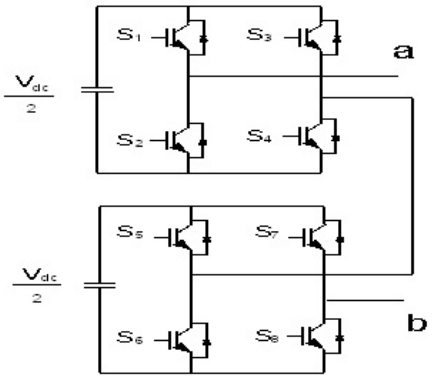

Fig. 3 (a) Cascaded H-Bridge Five level Inverter

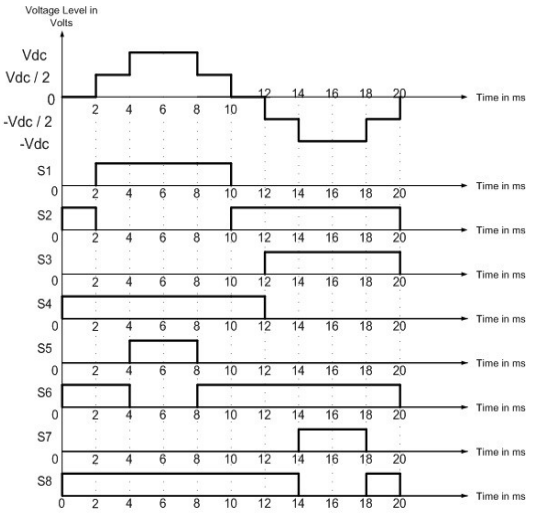

Fig. 3 (b) Switching wave form for Cascaded H-Bridge Five level Inverter

Table 2: Switching operation for a five level Cascaded H-Bridge inverter

S1	S2	S3	S4	S5	S6	S7	S8	V_o
ON	OFF	OFF	ON	ON	OFF	OFF	ON	V_{dc}
ON	OFF	OFF	ON	OFF	ON	OFF	ON	$V_{dc}/2$
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{dc/2}$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	$-V_{dc}$

The circuit diagram along with switching wave forms are shown in Fig. 3 (a) and 3 (b). The switching sequence for the respective switches is shown in Table 2. The Table 1 shows the corresponding output voltages for the corresponding switching operation of the power switching devices. Fig. 3 (a) shows the complete circuit diagram of a Five level H-Bridge inverter along with its switching ON-OFF conditions. Individual ON times and OFF times of individual switches were also represented in Fig. 3 (b).

Table 3: Output voltage according to switching ON-OFF condition for an asymmetrical seven level inverter

S1	S2	S3	S4	S5	S6	S7	S8	V_o
ON	OFF	OFF	ON	ON	OFF	OFF	ON	V_{dc}
OFF	ON	OFF	ON	ON	OFF	OFF	ON	$2V_{dc}/3$
ON	OFF	OFF	ON	OFF	ON	OFF	ON	$V_{dc}/3$
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{dc}/3$
OFF	ON	OFF	ON	OFF	ON	ON	OFF	$-2V_{dc}/3$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	$-V_{dc}$

C. Cascaded H-Bridge Asymmetrical 9 level Inverter:

A Nine level cascaded multilevel inverter consists of two H-Bridges. The first H-Bridge H1consists of a separate DC source $V_{dc}/4$, whereas the second H-Bridge H2 consists of a dc source $3V_{dc}/4$ as shown in Fig. 4. Let the output of H-Bridge-1 be denoted as $V_1(t)$ and the output of H-Bridge-2 be denoted as $V_2(t)$. Hence the total output voltage is given by $V(t) = V_1(t) + V_2(t)$. By alternate closing and opening of different switching configurations we can get different voltage levels.

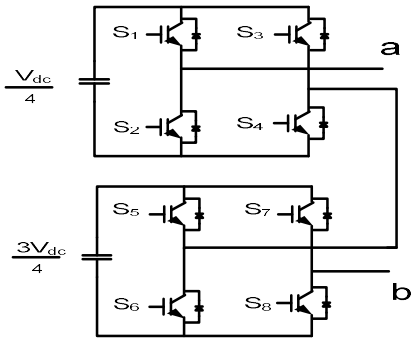

Fig. 4 Cascaded H-Bridge Asymmetrical Nine level Inverter

Table 4: Output voltage according to switching ON-OFF condition for an asymmetrical nine level inverter

S1	S2	S3	S4	S5	S6	S7	S8	V_O
ON	OFF	OFF	ON	ON	OFF	OFF	ON	V_{dc}
OFF	ON	OFF	ON	ON	OFF	OFF	ON	$3V_{dc}/4$
OFF	ON	ON	OFF	ON	OFF	OFF	ON	$2V_{dc}/4$
ON	OFF	OFF	ON	OFF	ON	OFF	ON	$V_{dc}/4$
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	ON	$-V_{dc}/4$
ON	OFF	OFF	ON	OFF	ON	ON	OFF	$-2V_{dc}/4$
OFF	ON	OFF	ON	OFF	ON	ON	OFF	$-3V_{dc}/4$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	$-V_{dc}$

Fig. 4 shows the cascaded Nine level H-Bridge inverter circuit and Table 4 gives the corresponding output voltages for the corresponding switching operation of the power switching devices.

D. Hardware schematic Diagram:

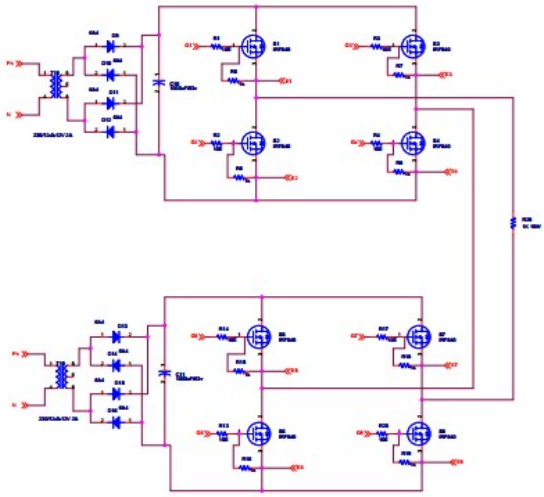

Fig. 5 Schematic Diagram of Hardware model

Fig. 5 shows the general schematic diagram of hardware model of multilevel inverter. By proper adjusting the values of two input DC voltages we can obtain the operation for symmetrical five level, asymmetrical seven and nine level inverter topologies as required for the same schematic model as in Fig. 5.

Table 5: Effectiveness of different multi-level topologies

Parameters	No.of Switches	No.of Protective circuits	No.of Gate drives	Cost
Symmetrical 7-Level (Voltage stress of Vdc/3)	12	12	12	High
Asymmetrical7-Level (Voltage stress of Vdc/3)	8	8	8	Low
Symmetrical 9-Level (Voltage stress of Vdc/4)	16	16	16	High
Asymmetrical 9-Level (Voltage stress of Vdc/4)	8	8	8	Low

Table 5 shows the effectiveness of different multi-level topologies comparing their cost, number of switches required, number of protective circuits, number of gate drive circuits and maximum voltage stress across each switch. With this comparison the optimum multi-level topology can be employed for a particular application. In cascaded multi-level inverter H-Bridge topology the number of switches reduces in asymmetrical level with reduction in number of gate drivers, number of protective devices. The cost effectiveness also increases in asymmetrical topology when compared to symmetrical topology.

III. MATLAB/SIMULINK AND HARDWARE IMPLEMENTATIONS

Case-1: Symmetrical five level inverter

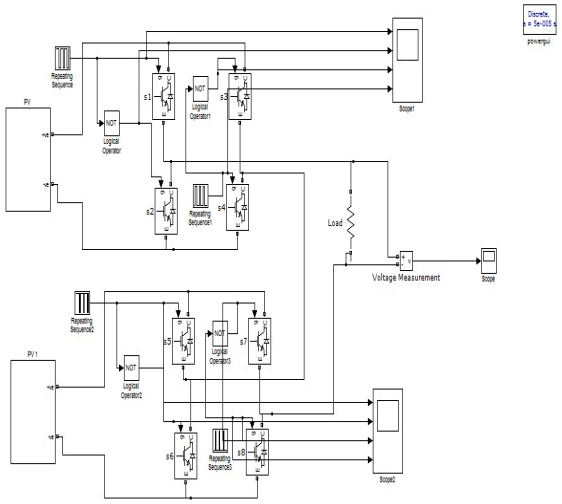

Fig. 6 Matlab/Simulink Power circuit of Cascade Five Level H-Bridge Inverter

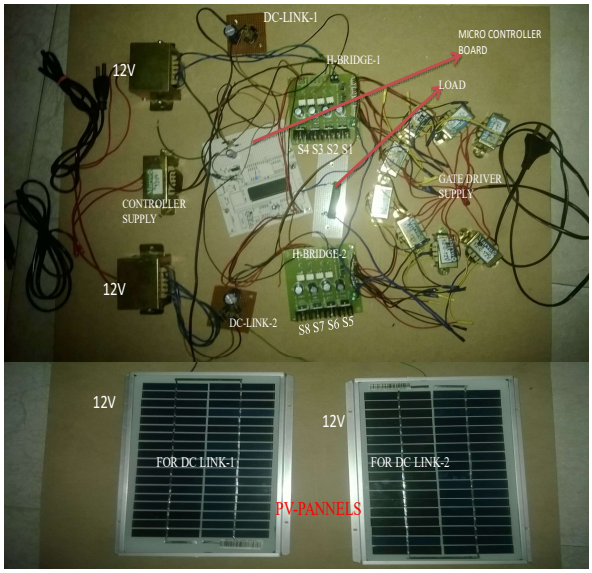

Fig. 7 Hardware Power circuit of Cascade Five Level H-Bridge Inverter

Asymmetrical configuration consists of unequal voltages. Fig. 6 shows Matlab/Simulink Power circuit of Cascade Five Level H-Bridge Inverter and Fig. 7 gives Hardware Power circuit of Cascade Five Level H-Bridge Inverter. Hardware circuit employs 8051 microcontroller to generate required control signals. Hardware circuit shows the two 12V solar panels used as DC link voltage sources. Fig. 8 shows Hardware Switching pulses for Cascade Five Level H-Bridge Inverter and Fig. 9 shows Matlab/Simulink Switching pulses for Cascade Five Level H-Bridge Inverter.

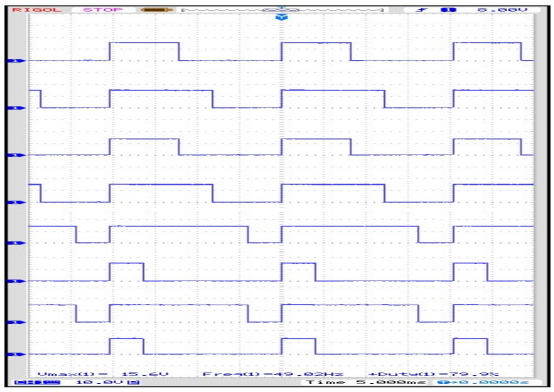

Fig. 8 Hardware Switching pulses for Cascade Five Level H-Bridge Inverter

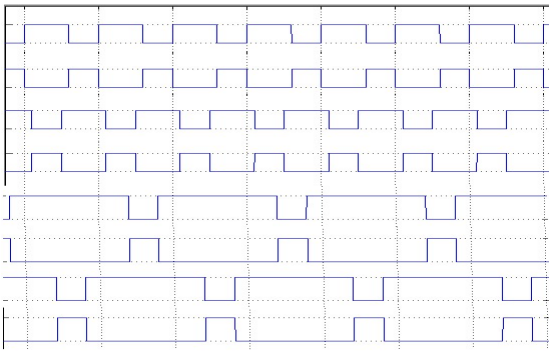

Fig. 9 Matlab/Simulink Switching pulses for Cascade Five Level H-Bridge Inverter

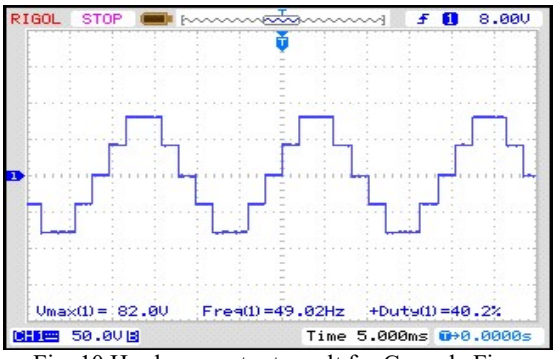

Fig. 10 Hardware output result for Cascade Five Level H-Bridge Inverter

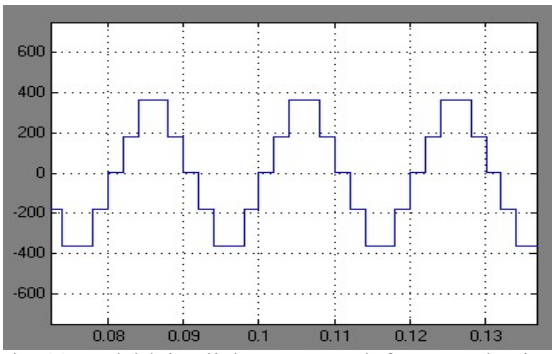

Fig. 11 Matlab/Simulink output result for Cascade Five Level H-Bridge Inverter

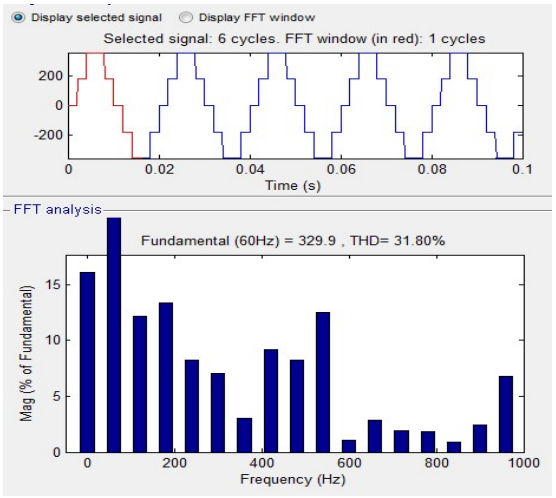

Fig. 12 FFT of Cascade Five Level H-Bridge Inverter

Fig. 10 and Fig. 11 shows the comparison of Hardware and Matlab/Simulink output results for Cascade Five Level H-Bridge Inverter. Also Fig. 12 shows the FFT window for Cascade Five Level H-Bridge Inverter which shows THD as 31.80%.

Case-2: Asymmetrical seven level inverter:

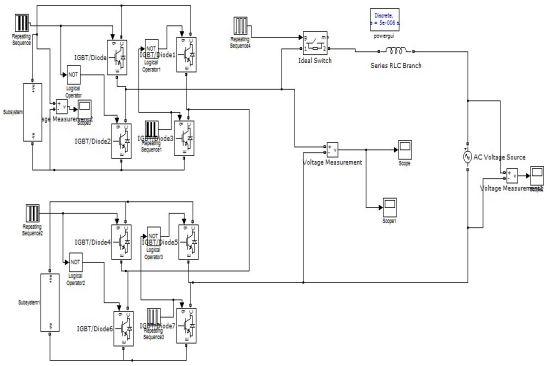

Fig. 13 Matlab/Simulink Power circuit of Cascade seven Level H-Bridge Inverter

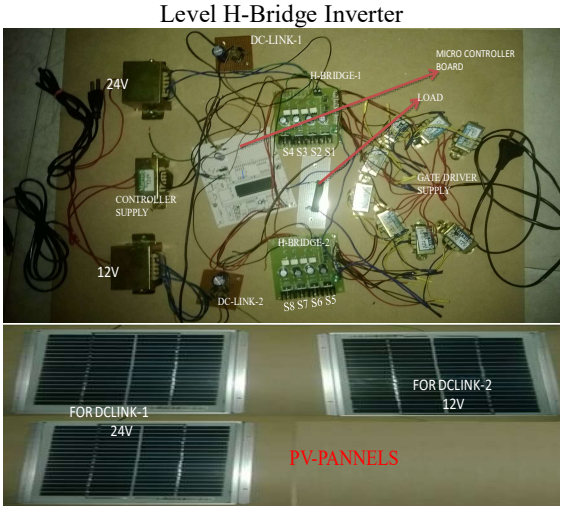

Fig. 14 Hardware Power circuit of Cascade seven Level H-Bridge Inverter

Fig. 13 shows Matlab/Simulink Power circuit of Cascade seven Level H-Bridge Inverter and Fig. 14 gives Hardware Power circuit of Cascade seven Level H-Bridge Inverter. Hardware circuit employs 8051 microcontroller to generate required control signals. Hardware circuit shows the two sets of solar panels 12V and 24V used as DC link voltage sources. To obtain 24V, two 12V panels were connected in series. Fig. 15 shows Hardware Switching pulses for Cascade seven Level H-Bridge Inverter and Fig. 16 shows Matlab/Simulink Switching pulses for a cascade Seven level H-Bridge Inverter.

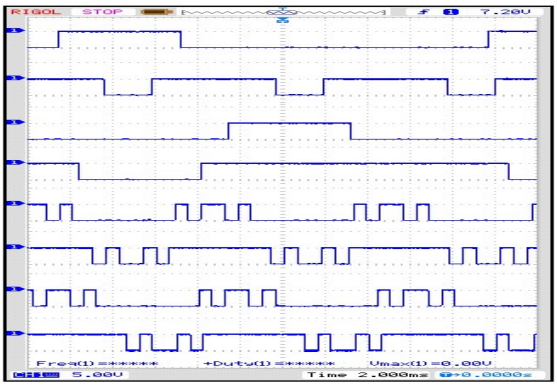

Fig. 15 Hardware Switching pulses for Cascade seven Level H-Bridge Inverter

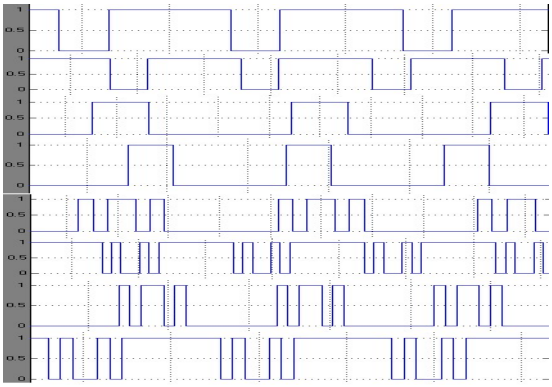

Fig. 16 Matlab/Simulink Switching pulses for Cascade seven Level H-Bridge Inverter

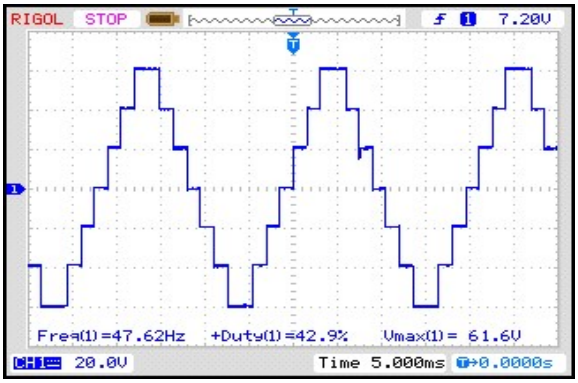

Fig. 17 Hardware and Matlab/Simulink output results for Cascade seven Level H-Bridge Inverter

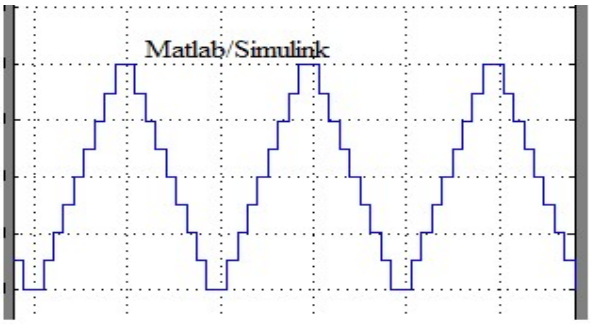

Fig. 18 Hardware and Matlab/Simulink output results for Cascade seven Level H-Bridge Inverter

Fig. 17 and Fig. 18 shows the comparison of Hardware and Matlab/Simulink output results for Cascade seven Level H-Bridge Inverter. Also Fig. 19 shows the FFT window for Cascade Five Level H-Bridge Inverter which shows THD as 18.17%.

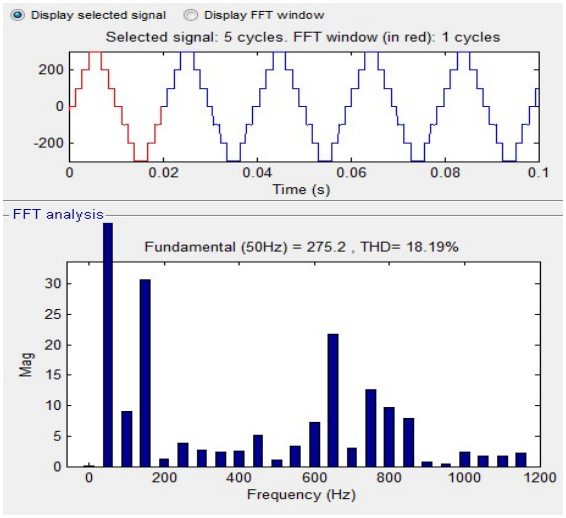

Fig. 19 FFT of Cascade seven Level H-Bridge Inverter

Case-3: Asymmetrical nine level inverter:

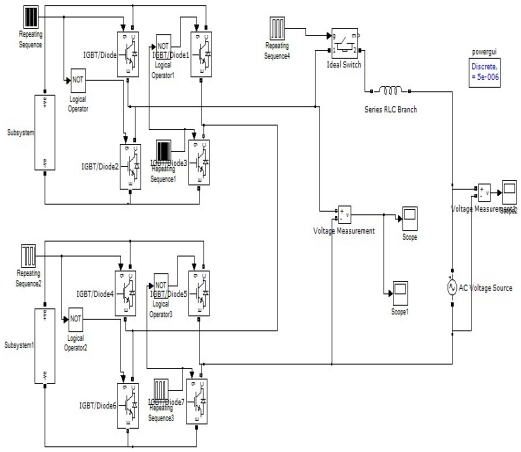

Fig. 20 Matlab/Simulink Power circuit of Cascade nine Level H-Bridge Inverter

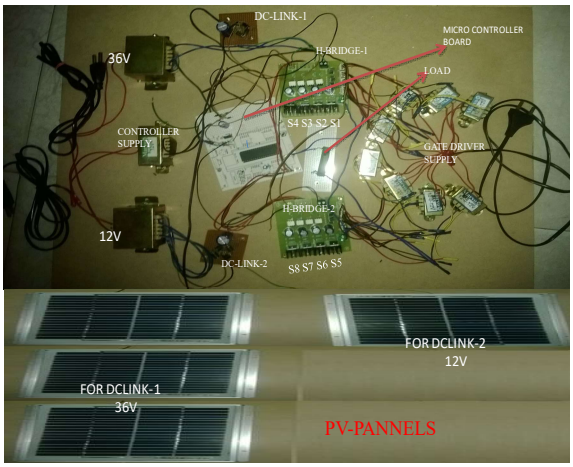

Fig. 21 Hardware Power circuit of Cascade nine Level H-Bridge Inverter

Fig. 20 shows Matlab/Simulink Power circuit of Cascade nine Level H-Bridge Inverter and Fig. 21 gives Hardware Power circuit of Cascade nine Level H-Bridge Inverter. Hardware circuit employs 8051 microcontroller to generate required control signals. Hardware circuit shows the two sets of solar panels 12V and 36V used as DC link voltage sources. To obtain 36V, three 12V panels were connected in series. Fig. 22 shows Hardware Switching pulses for Cascade nine Level H-Bridge Inverter and Fig. 23 shows Matlab/Simulink Switching pulses for a cascade Nine level H-Bridge Inverter

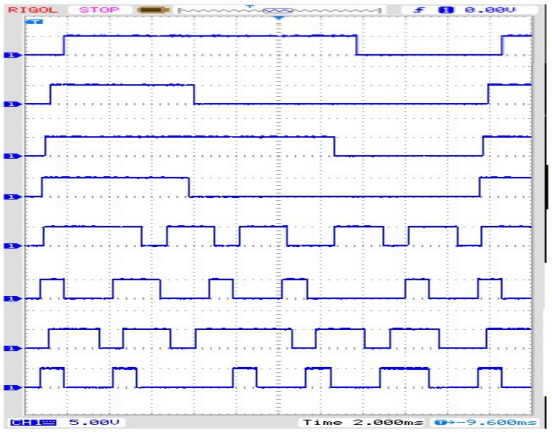

Fig. 22 Hardware Switching pulses for Cascade nine Level H-Bridge Inverter

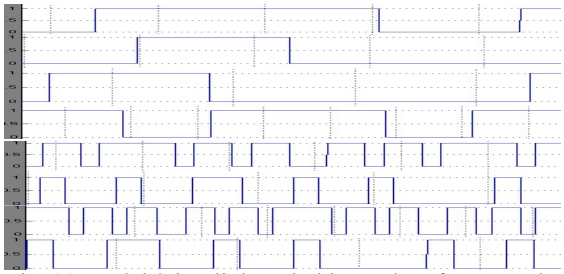

Fig. 23 Matlab/Simulink Switching pulses for Cascade nine Level H-Bridge Inverter

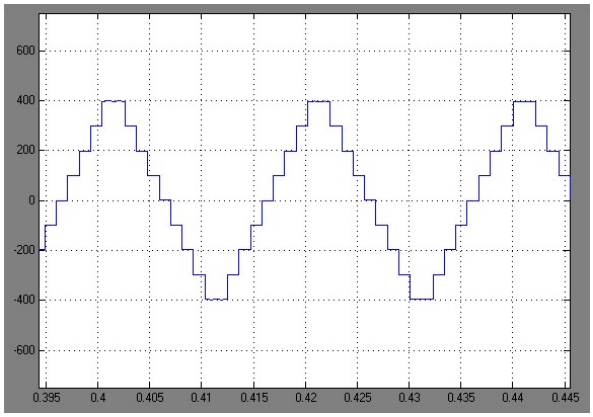

Fig. 24 Hardware and Matlab/Simulink output results for Cascade nine Level H-Bridge Inverter

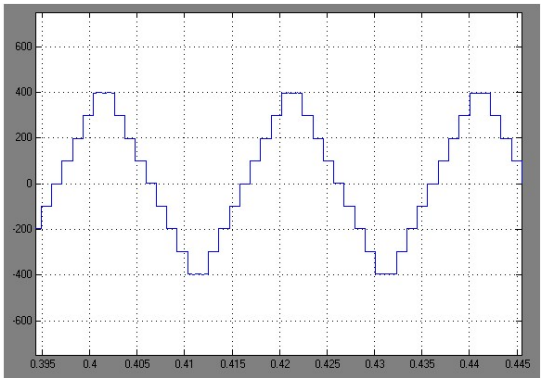

Fig. 25 Matlab/Simulink output results for Cascade nine Level H-Bridge Inverter

Fig. 24 and Fig. 25 shows the comparison of Hardware and Matlab/Simulink output results for Cascade nine Level H-Bridge Inverter. Also Fig. 26 shows the FFT window for Cascade Five Level H-Bridge Inverter which shows THD as 15.70%.

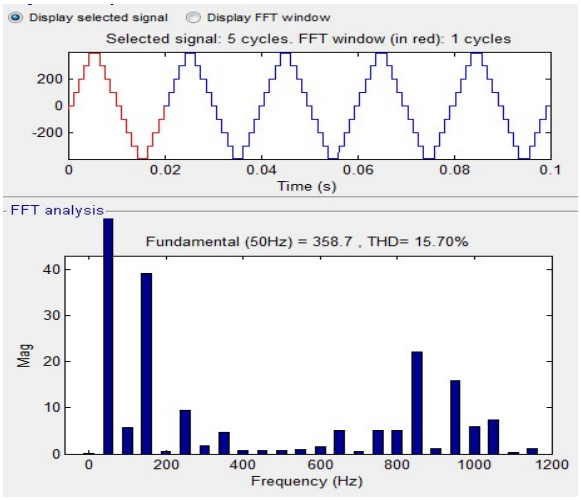

Fig. 26 FFT analysis of Cascade nine Level H-Bridge Inverter

Table 6: THD's of Voltage in different levels of inverter topologies

Configuration	Symmetrical 5-Level	Asymmetrical 7-Level	Asymmetrical 9-Level
THD	31.8 %	18.19 %	15.7 %

Table 6 represents the different THD values for different configurations of multi-level inverter topologies. Table 6 shows that as the level is been increased, the THD value decreases.

IV. CONCLUSION

By using multi level inverters we can increase the number of output levels. This multi level inverter concept is used to attain nearer sinusoidal wave at the output. Here in this paper, the concept of solar power as the input to the inverter instead of capacitors or any other sources are discussed by employing higher level inverters. In this paper, the comparison for five level symmetrical inverter concept is compared to asymmetrical seven and nine level cascaded H-Bridge inverter were discussed. The THD reduces as the number of output levels were increased increasing the system efficiency and performance. This paper explains the simplified method to generate gate pulses for the inverter topologies. With this type of simple logic circuit for generation of pulses, the number of snubber circuits becomes less. The number of gate drives will also become less and the control strategy is very easy to implement. The inverter type Hybrid H-Bridge produces greater voltage levels while using less number of switching devices. Reducing the number of switches also reduces switching losses and THD. Finally the simulation results are validated with hardware results.

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