DUAL VOLTAGE CONTROL OF REDUCED SWITCH HYBRID QUASI Z MULTILEVEL INVERTER FOR ISOLATED ENERGY SYSTEMS

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Abstract: *This paper investigates the performance of new reduced switch hybrid Quasi Z inverter with dual voltage control for isolated energy systems. The proposed hybrid inverter integrates the stepped DC link circuit and the Quasi Z source inverter to yield buck/boosted multilevel AC voltage. It features the advantages of reduced source and switch count, minimized stress and inrush current, use of single impedance network for buck/boost operation thus reducing the passive component requirement and mitigated harmonic profile. Efficient operation of the system is obtained by independent dual feedback control in a way to minimize the high frequency switching variations of the inverter switches. Improved efficiency by 5% is obtained by dual voltage control of proposed inverter thus enhancing system performance. Detailed theoretical analysis of the equivalent model for different operating modes is described and the simulation is performed for a seven level proposed inverter in MATLAB/Simulink. Experimentation of the prototype model of proposed inverter is done in laboratory and the results are validated.*

Key words: *Z source inverter, dual voltage control, harmonics, buck/boost.*

1. Introduction

Z source inverters are gaining importance in application with isolated energy systems due to its prominent advantages of single stage buck/boost conversion, inclusion of shoot through states and higher operational efficiency [1].The voltage quality is always a constraint for Z source inverters. Many topological renovations are being encountered in the field of Z-Source inverter to improvise its performance from its predecessor. Quasi Z source inverters show improved performance by reducing the stress on the devices and contributes high boost factor [2]. Extended Boost Quasi Z-source inverterimplements a topological modification to obtain high boost factor and afford continuous operation of current [3-4], reduction in inrush current is obtained by Improved Z-Source inverter [5]. Trans Z source inverter replaces inductors with coupled devices in the topology. Z source matrix converter combines the advantages of Z source inverter and matrix converter. All the aforesaid inverters produce two level output voltage with high harmonic content and the components are subjected to high stress. To overcome the drawback multilevel Z source inverters were reported in literature but they require more number of switching devices to produce higher levels in output voltage [7]. The structure proposed in [8] used individual LC network in each legs of H bridge inverter of CMLI that increases the passive component count. To overcome the above said drawbacks, the hybrid quasi Z inverter structure is devised that uses reduced source count and single LC network for buck boost operation. The proposed reduced source hybrid Quasi Z multilevel inverter (RSqZMLI) consist of two stage operation, first stage operates at fundamental frequency and produces stepped DC voltage which is boosted and inverted by the second stage operating at high switching frequency.

The variations in inverter voltage resulting due to changes in isolated energy systems are controlled by dual voltage control. Conventional Z source inverters are subjected to single mode control where the switching devices are prone to continuous switching variations [9-12]. In the present work, the RSqZMLI is controlled by independent dual-loop voltage control. Control strategy is set to regulate the DC link voltage at fundamental frequency and the inverter voltage at high switching frequency. This minimizes the switching power loss and contributes for the improvement in efficiency and ensures safe operation.

Detailed analysis of the system is performed in simulation using MATLAB/Simulink. The effect of voltage stress for different duty ratio is studied for different input conditions. Dual-loop control is studied for different operating conditions and the switching variationsare analyzed. A comparative evaluation of the inverter with its counterpart is presented to substantiate the claimed advantages

and the results are presented.

2. Reduced Source Hybrid Quasi Z Multilevel Inverter

The structure of the proposed reduced source hybrid Quasi Z multilevel Inverter producing seven level in the output voltage is shown in Fig .1. The inverter uses two isolated sources and two switches programmed to combine the sources at specified time interval to form stepped DC link voltage (Vsdc).

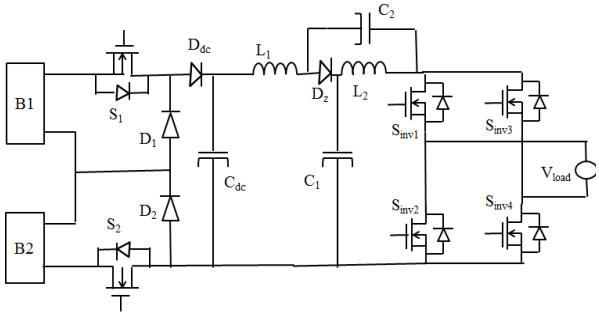


Fig. 1. Structure of Stepped DC link coupled Quasi Z multilevel inverter

Fundamental switching frequency is implemented on the DC side. The stepped input fed to the inverter produces buck/boosted multilevel AC voltage by the simple inclusion of shoot through states in the firing pulse of inverter. Out of different switching strategies formulated for Z source inverters in literatures, maximum constant boost control with third harmonic injection is simple and provides high boost factor and high voltage gain with constant shoot through and hence opted for the proposed inverter[13-16]. The relation between the voltage gain and the Ma is graphically described by Fig. 2. It is observed that for decrease in Ma, the voltage gain increases due to the increase in the shoot through state. The multiple switching levels present in the system exposes the components to low switching voltages as compared to conventional Z source inverters and PWM inverters thus reducing dv/dt and voltage stress problems.

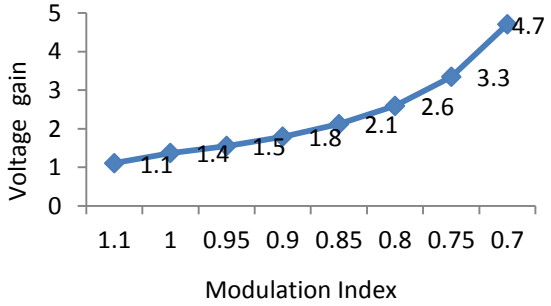


Fig .2. Voltage gain of RSqZMLI for different Ma

2.1 Modes of Operation

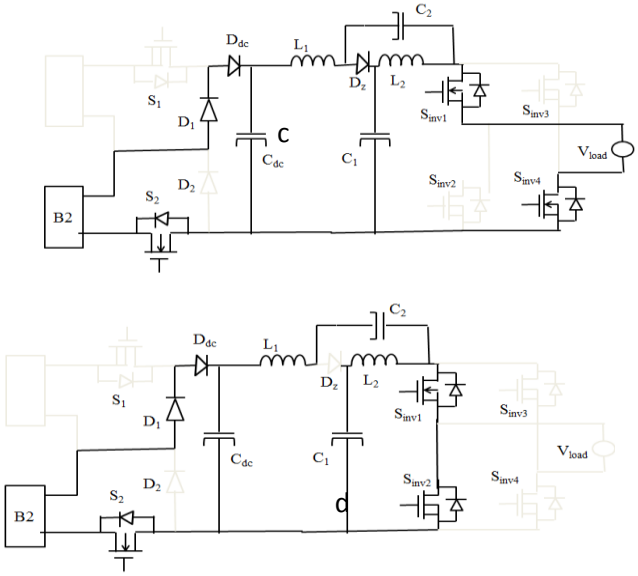
The operation of the inverter is explained with the following modes of operation. The inverter works on asymmetrical voltage levels with the battery voltages B_1 as V_{dc} and B_2 as $V_{dc}/2$. The equivalent circuit of the inverter during various modes is shown in the Fig. 3. The inverter works under shoot through state and active state during the various modes.

a) Mode 1: The switch S_2 conducts and switch S_1 is in off state. The voltage stored in the battery B_2 appears across the inverter through D_2. During the shoot through state, the S_{inv1} and S_{inv3} conducts and the legs of the inverter is shorted. The diode D_Z goes to off state and the energy storage operation happens in the impedance network. During the active state the power flows to the load through S_{inv1} and S_{inv4}. The first level of voltage appears in the output. The equivalent circuit of mode 1 operation is shown in Fig. 3a and 3b.

b) Mode 2: In this mode the switch S_2 is in off state and switch S_1 conducts. During the shoot through state the second input level is boosted and during the active state it appears across the load. The equivalent circuit of mode 2 is shown in Fig. 3c and 3d.

c) Mode 3: Fig. 3e and 3f portrays the equivalent circuit of mode 3. Both the switches S_1 and S_2 are under ON state during this mode. The diodes D_1 and D_2 are in off state. The sum of the both battery voltages are added up and boosted by the impedance network. The boosted voltage appears across the load as the third level. These operations happen for half cycle, during the inversion mode of the inverter the three levels are repeated in negative half cycle.

For zero voltage level in the output, both the switches are turned off and diodes D_1 and D_2 conduct.



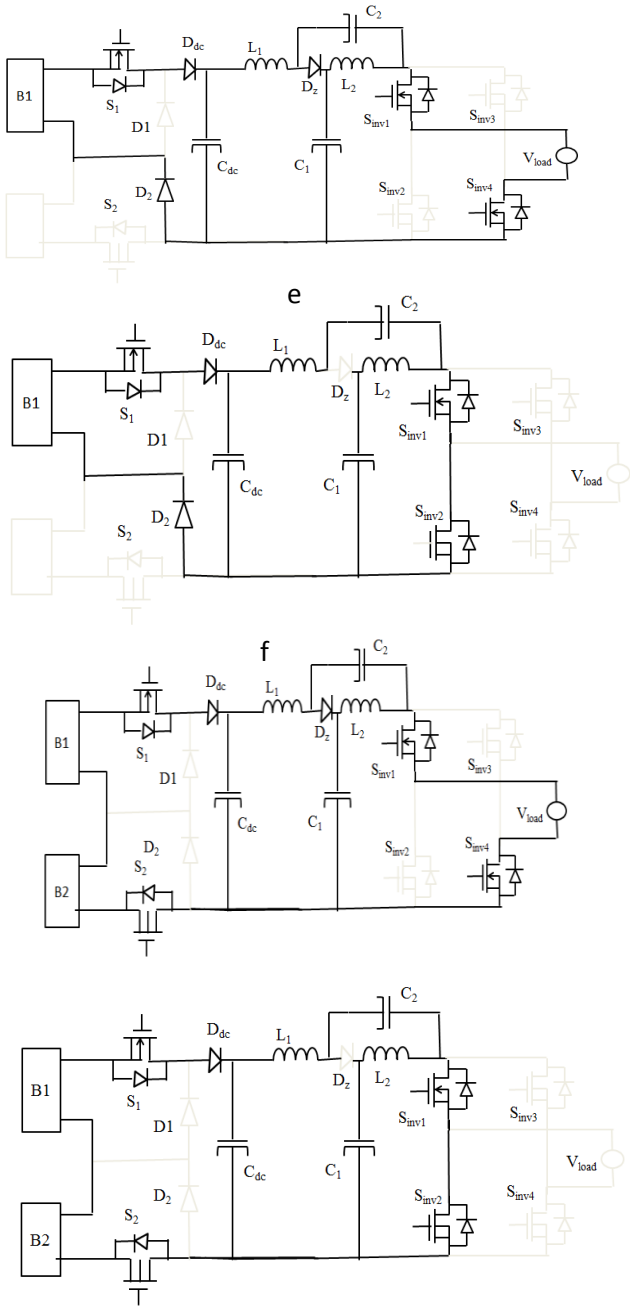


Fig .3. Equivalent circuit of the proposed RSqZMLI during different modes of operation

2.2 Dual voltage control of RSqZMLI

The dual loop voltage control is performed by controlling the DC link voltage (V_{sdc}) and the inverter voltage (V_{ac}). Nominal reference voltage (Vnom) is set for the stepped DC link circuit and the control is performed under two cases.

If Vsdc >Vnom: This case arises during high generated voltage from isolated systems. Vsdc exceeds Vnom and the PI controller controls the firing signal fed to the switches S1 and S2 till Vsdc reduces to Vnom . During this period, the modulation index of the inverter remains unaltered and is switched at constant time period. The circuit diagram of the inverter with control logic is given in Fig. 4.

If Vsdc <Vnom: During unhealthy conditions of drive motor, the speed is reduced and the generated voltage is subjected to decrease, Vsdc becomes less than Vnom. Since stepped DC link circuit can perform only buck operation, its modulation index is set to 1 and no control is performed on DC link side. The input to the inverter is reduced and voltage boost is achieved by controlling the Ma on the inverter side.

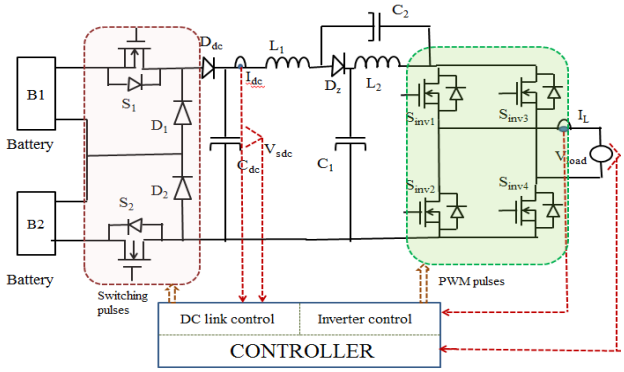


Fig .4. Circuit diagram of proposed RSqZMLI with dual control logic

The block diagram of RSqZMLI with two independent PI controller is shown in Fig. 5. Gc1(s) indicates the transfer function of stepped DC link circuit and Gc2(s) corresponds to the transfer function of QZSI inverter. Saturation limits are set to limit the reference signal beyond the threshold value. The control is shared by DC switches and inverter switches and this reduces the high frequency switching variations of the inverter and leads to loss minimization.

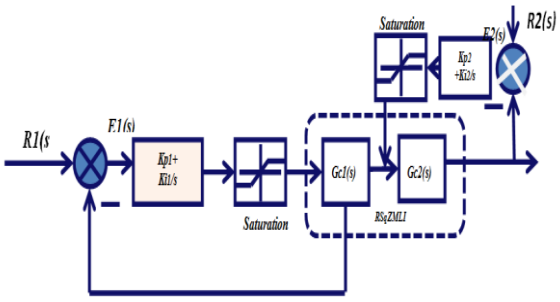


Fig.5. Dual voltage control of RSqZMLI

3. Analysis of RSqZMLI

The analysis of the proposed RSqZMLI is carried for shoot through state and active state. The shoot through state arises when switches of the same leg or of both the legs are shorted and produces a short circuit. This enables the buck boost operation in the inverter. The equations governing the shoot through state is given by (1),

$$V_{sdc} - L_1 \frac{d_{i1}}{dt} + V_{c2} = 0$$

$$-L_2 \frac{d_{i2}}{dt} + V_{c1} = 0 \quad (1)$$

The state equations are framed with the state variables as inductor currents (iL1=x1, iL2=x2) and capacitor voltages (Vc1=x3, Vc2=x4). The shunt resistance across the capacitance is assumed as Rc1 and Rc2. The state space representation for the shoot through state is given by (2)

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1/L_1 \\ 0 & 0 & 1/L_2 & 0 \\ 0 & 1/C_1 & 0 & 0 \\ 1/C_2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{sdc} \quad (2)$$

The circuit equations during the non- shoot through state are given by (3),

$$V_{sdc} - V_{L1} - V_{c1} = 0$$

$$-V_{L2} - V_{ac} + V_{c1} = 0$$

$$V_{c2} + V_{L2} = 0 \quad (3)$$

The state space representation for the non-shoot through state is given by (4),

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 \\ 0 & 0 & 0 & -1/L_2 \\ 1/C_1 & -1/C_1 & 0 & -1/C_1R_{c2} \\ 1/C_2 & 1/C_2 & 1/C_2R_{c1} & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{sdc} \quad (4)$$

The expression for capacitor voltage is arrived by calculating the average voltage in an inductor and equating it to zero. α is taken as the shoot through duty ratio, the capacitor voltages in terms of duty ratio is obtained as (5),

$$V_{c2} = \frac{\alpha}{1-\alpha} V_{c1}$$

$$V_{c1} = \frac{1-\alpha}{1-2\alpha} V_{sdc} \quad (5)$$

The relation between stepped DC link voltage and inverter output voltage is given as (6),

$$-V_{L2} - V_{ac} + V_{c1} = 0$$

$$-V_{c2} = -V_{ac} + V_{c1}$$

$$-\frac{\alpha}{1-\alpha} V_{c1} = -V_{ac} + \frac{1-\alpha}{1-2\alpha} V_{sdc}$$

$$-\frac{\alpha}{1-\alpha}\frac{1-\alpha}{1-2\alpha} V_{sdc} = -V_{ac} + \frac{1-\alpha}{1-2\alpha} V_{sdc}$$

$$\frac{1}{1-2\alpha} V_{sdc} = V_{ac} \quad (6)$$

The capacitor and inductor values are obtained through the design equations given by (7)

$$L_1 = \frac{dt(V_{sdc} - V_{c1})}{di1}, L_2 = \frac{dt(V_{c2})}{di2}, C_1 = \frac{dt(i_{L2})}{dV_{c1}}, C_2 = \frac{dt(i_{L1})}{dV_{c2}} \quad (7)$$

Multi loop control using two independent control has the transfer function given by equations (8-10).

$$\frac{C1(s)}{R1(s)} = \frac{G_{c1}(s)(K_{p1} + K_{i1}/s)}{1 + G_{c1}(s)(K_{p1} + K_{i1}/s)} \quad (8)$$

$$\frac{C_1(s)}{R_1(s)} = \frac{sG_{c1}(s)K_{p1} + G_{c1}(s)K_{i1}}{s(1 + G_{c1}(s)K_{p1}) + K_{i1}} \quad (9)$$

$$\frac{C_2(s)}{R_2(s)} = \frac{G_{c2}(s)(K_{p2}(s) + K_{i2}(s)/s)}{1 + G_{c2}(s)(K_{p2}(s) + K_{i2}(s)/s)} \quad (10)$$

Efficiency of the proposed inverter is determined by framing the power balance equations. The outputpower is obtained as the product of output voltage and current and the equations are given by (11).

$$Pout = V_{ac} I_{ac}, V_{ac} = V_m Sin\omega t, I_{ac} = I_m Sin(\omega t - \phi)$$

$$Pout = V_m Sin\omega t \, I_m Sin(\omega t - \phi)$$

$$Pout = \left(\frac{1}{1-2\alpha}\right) V_{sdc} I_m \left[\frac{\cos(\phi) - \cos(2\omega t - \phi)}{2}\right] \quad (11)$$

The DC input power appears to the inverter during the non- shoot through period and is zero during the shoot period. The DC power equation is given as (12)

$$Pin = (1-\alpha) V_{sdc} I_{dc} + \alpha(0) \quad (12)$$

The efficiency is calculated as the ratio of output power to input power. The efficiency equation is given by (13)

$$\eta = \frac{Pout}{Pin} = \frac{Pout}{Pout + losses} = \frac{Pout}{Pout + Pcaploss + Pindloss + Pswloss + Pconloss} \quad (13)$$

3.1 Power Loss Calculation

The power loss in qZSI includes loss in active state and shoot through state. The total loss comprises of loss in Z impedance network, switching loss and conduction loss.

a. Loss in Impedance network: The power loss in the capacitor and the inductor is accounted for loss in impedance network. The copper loss in inductor and capacitor is given by (14).

$$P_L = 2 I_L^2 R_L \text{ and } P c1, c2 = 2 I_{c1}^2 R_c \quad (14)$$

where R_L and R_C are resistance of inductor and capacitor.

b. Switching loss: The switching loss includes the turn on/off of the MOSFET switches. The switching loss during the shoot through state is given by (15) and during the active state is given by (16) [17].

$$P_{sh} = (V_{sdc} I_{L1} \frac{T_{crt} + T_{vrt}}{2} + V_{sdc} I_{L1} \frac{T_{vrt} + T_{cf\,t}}{2}) fs / 2 \quad (15)$$

$$P_{act} = Q_{rr} V_{sdc} fs + \frac{2}{\pi} \int_0^{\pi} ((V_{sdc} I_n \frac{T_{crt} + T_{vrt}}{2} + V_{sdc} I_n \frac{T_{vrt} + T_{cf\,t}}{2}) \frac{fs}{2} d\omega t \quad (16)$$

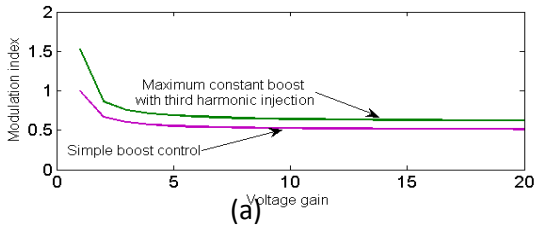
Where Qrr is the reverse recovery charge, IL1 is the current during shoot through and In is the current during active state.

4. Results and discussion

The proposed seven level RSqZMLI is built in MATLAB–Simulink with the following circuit parameters; L_1=L_2=700µH and C_1=C_2=0.6µF, stepped DC circuit is switched at fundamental frequency and inverter is switched at 10 kHz. Maximum boost control with third harmonic injection technique is used to generate firing pulse for the qZMLI.

Fig. 6a.depicts the modulation index for different voltage gain obtained by simple boost control and maximum constant boost control with third harmonic injection. The same voltage gain is obtained with higher modulation index in third harmonic injection and reduces the stress on the devices. Hence third harmonic injection is implemented for the proposed system.

The effect of shoot through duty ratio for different input voltages is given in Fig. 6b. The increase in shoot through duty ratio has a direct impact on the boosted voltage and the component selection is greatly affected by this phenomena. The effect of shoot through duty ratios on capacitor voltages for different input voltage is shown in Fig. 6c. and Fig. 6d. As the boost value increases, an increase in stress is experienced and the capacitor 2 is prone toless stress compared to capacitor 1 in quasi Z network.



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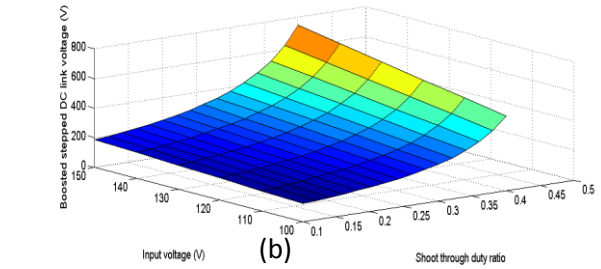

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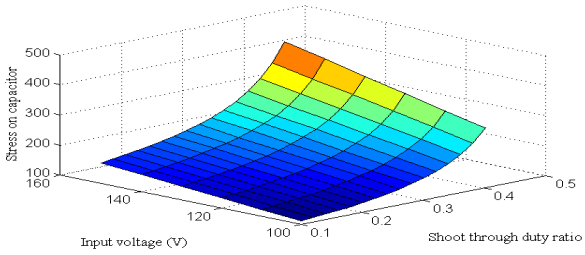

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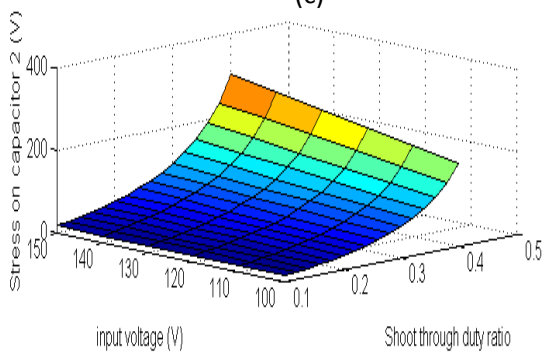


(d)

Fig. 6. Analysis of RSqZMLI for different shootthrough duty ratio

4.1 Analysis of RSqZMLI performance

Two different voltages of B_2=60 V and B_1=120 V are fed to the simulation model of seven level RSqZMLI and its performance is analyzed for 0.82 power factor RL load. Fig. 7.displays the output obtained at various stages of the inverter. The stepped DC voltage of 180V with 7 levels is boosted to 320V and is flipped by the inverter to produce 7 level AC voltage. The load current is a sinusoidal AC of 6.2 A and the voltage across the capacitor is measured to be 240V. The source DC current is 10A with no inrush at the start. The voltage harmonic distortion obtained after LC filter is 3.99% and the filter requirements are minimized compared to conventional two level QZSI. The distortion in current waveform is 9.41%.

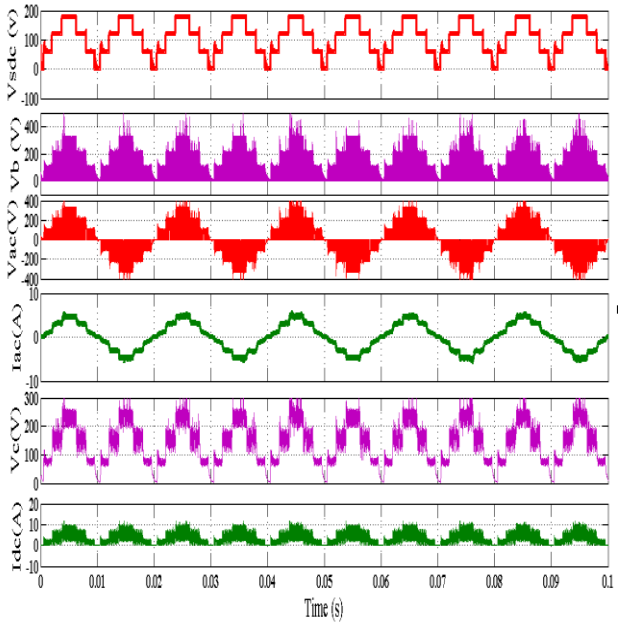


Fig. 7. Simulation results of 7 level proposed RSqZMLI at modulation index of 0.83

A comparative study is performed between QZSI and RSqZMLI to demonstrate the advantages of the proposed structure and is listed in table 1. Both the system outputs rated voltage of 230V (rms) and it is very well seen that the stress produced in RSqZMLI is less compared to QZSI which decreases the rating and the power loss in the impedance network. The stress on the devices is reduced by 77% and the output voltage is improved by 67%. The presence of reduced input during the start minimizes the inrush current in the inverter.

TABLE 1
Comparative evaluation of RSqZMLI and QZSI for Vin =180V(60V each source) and Ma=0.83

Parameter	RSqZMLI	QZSI
Vsdc	Stepped voltage	Constant DC voltage
Boosted Voltage (Vb)	320V (stepped voltage)	410V (chopped DC)
Inverter voltage (Vac)	7 level voltage	Two level voltage
Voltage stress on devices	262V	340V
Inrush current	Nil	150% of input current
Voltage THD without filter	48%	72%
Voltage THD with filter	3.99%	9.15%
Current THD	9.41%	14.15%

The dual closed loop control is performed for different operating conditions of the input voltage.

Case1: Vsdc is greater than Vnom: The DC circuit is operated at Ma=1 for prescribed input voltage. Vnom is set to 140V and the stepped DC link voltage tracks the reference after the rise time of 0.3sec. For a step change in the input voltage of Vdc by 1.45 times the nominal voltage, the PI controller adjusts the Ma to 0.67 to reduce the voltage to nominal value. The error in the stepped DC link voltage is 3V. The step change in input voltage to 67V controls the Ma to 0.83 to get the required operating voltage. Returning to the intial condition, the output voltage tracks the input at Ma=1. Thus for input voltages greater than nominal voltage, the Vsdc is controlled by the DC control circuit. The control operation is visualized in Fig. 8.

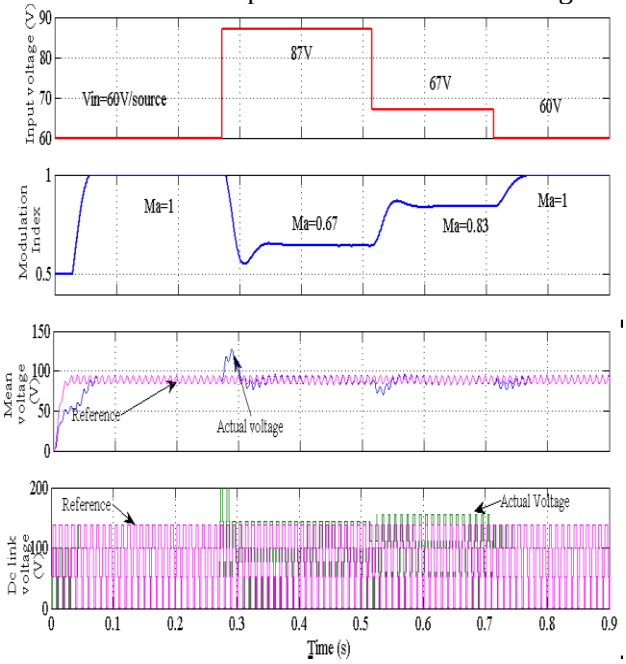
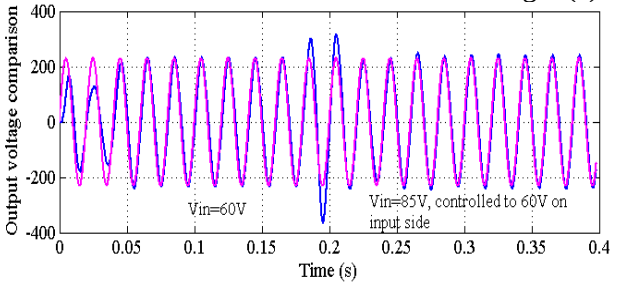


Fig. 8. Simulation results of control action on DC side for Kp=1.78 , Ki=0.72

Case2: Vsdc is less than Vnom: For input voltage less than the nominal voltage, the inverter side control is implemented. Fig. 9.depicts the control approach on the inverter side for different input voltages. For nominal input voltage of 60V from input, the Ma on DC side is 1 and rated output voltage of 230V(peak) is obtained from inverter for Ma of 0.83. The output voltage tracks the reference voltage after a settling time of 0.038sec with a steady state error of 0.014% is obtained. For dynamic increase in input voltage by 41%, the control is executed on the DC circuit and Ma of the inverter remains at 0.83 which is shown in Fig. 9(a).



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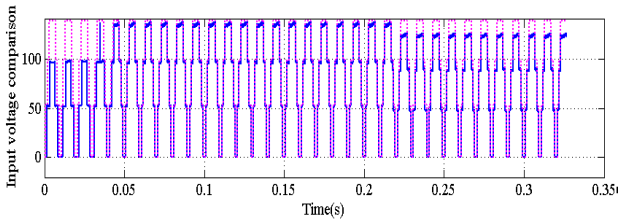

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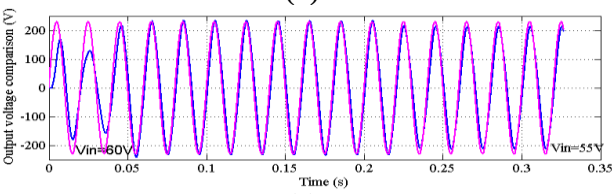


(c)

Fig. 9. Simulation results of control action on inverter side for Kp=1.78 , Ki=0.72

For 8.33% decrease in input voltage, reduced Vsdc appears as input to the inverter shown in Fig 9(b). The buck boost nature of the inverter is utilized to boost the input voltage to the rated operating conditions. The control circuit on the inverter side adjusts the Ma to 0.78 to produce 230V output voltage. The error obtained in the output voltage is 6V. The controlled output voltage is shown in Fig. 9(c).

Chain of simulations were performed to obtain the optimum modulation index for rated voltage on both DC and inverter side. Table 2 consolidates the optimum modulation index for different input conditions.

Table 2
Optimum modulation index for Dual voltage control of RSqZMLI

Input voltage (Sources count = 2)	Dual voltage control to obtain rated operating conditions (Mf= 200)	
	Ma (DC)	Ma (inv)
40	0.57	0.76
35	0.64	0.76
60	1	0.76
15	1	0.68
10	1	0.63
8	1	0.59

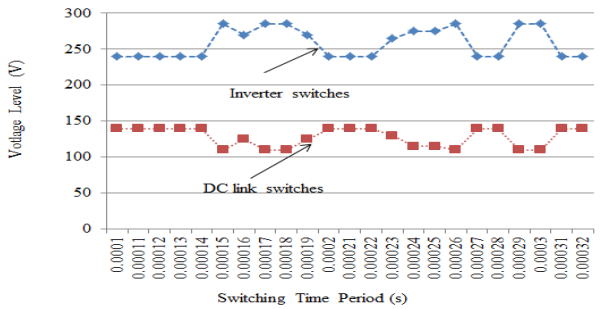
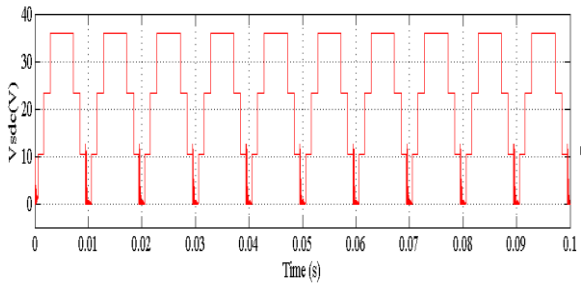
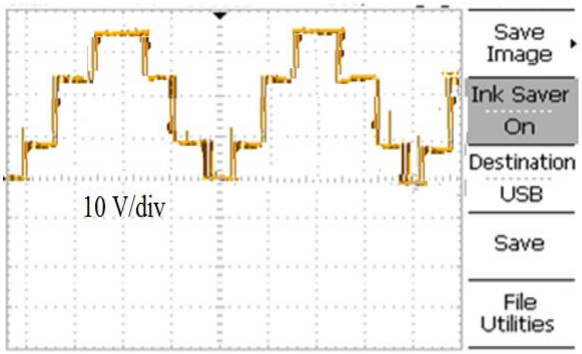


Fig. 10. Voltage level in switching devices for different switching time period

To study the voltage level appearing across the switches for rapid change in input voltages, readings were tabulated and plotted as graph in Fig. 10. For input equal to Vnom, the voltage level on the switches remains unaltered. For Vsdc less than Vnom, the voltage level on DC link switch reduce and consequently boost operation increases the voltage in inverter switches. The DC link switches operate at fundamental frequency and hence the switching loss is less that helps to improve the efficiency. Since the control is shared by both the circuits, the switching variations are minimized that increases the lifetime of the switches.

From the analysis it is evident that the size of battery is reduced and the harmonic profile is improved in RSqZMLI. The stress on devices is reduced by 43% and the RSqZMLI is found to be cost effective with reliable performance. The dual loop control shows an improved performance with reduced losses and switching variations and is comparatively a better choice for isolated energy systems. Fig. 11 depicts the prototype model, simulation and hardware output of open loop RSqZMLI for shoot through duty ratio of 22%.





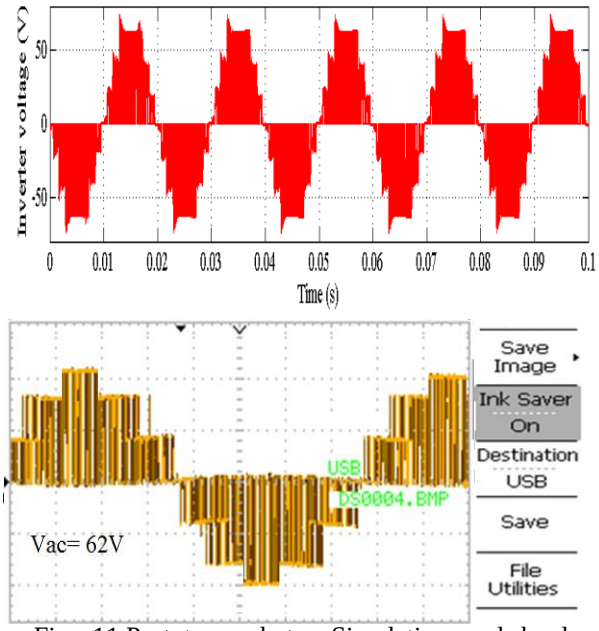


Fig. 11.Prototype photo, Simulation and hardware output of RSqZMLI for input voltage of B_1=24V, B_2=12V. α=22%

5. Conclusions

This paper has presented the dual voltage control of new reduced source hybrid quasi Z multilevel inverter for performance enhancement of isolated energy systems. Theoretical analysis, simulation and experimental validation of a prototype system are performed to illustrate the concept. The RSqZMLI uses reduced source, switch count and uses single impedance network compared to other CMLIs with boost network. The impedance network is subjected to reduced stress of 43% and the output is prone to an improved harmonic mitigation of 24% that reduces the rating of the component used. Use of isolated small size batteries maintains continuous operation of the system and proves to be more reliable for isolated systems. The dual loop control minimizes the switching variations of inverter switches and leads to overall improvement in efficiency by 5% and proves to be cost effective inverter.

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