

REAL-TIME IMPLEMENTATION OF A NOVEL VECTOR-LOCKED LOOP FOR SYNCHRONOUS EXTRACTION OF HARMONICS IN POWER SYSTEMS

Jora M. GONDA

National Institute of Technology Karnataka, Surathkal, India.
Department of Electrical and Electronics Engineering,
Post Srinivasnagar, Mangalore-575025 Karnataka, India.
Email: joragondam@gmail.com

Sumam S. DAVID

National Institute of Technology, Karnataka, Surathkal, India.
Department Electronics and Communication Engineering,
Post Srinivasnagar, Mangalore-575025 Karnataka, India.

Abstract: *The extraction of the harmonics and or the fundamental from a distorted waveform is an important process in the implementation of custom power devices. Several schemes have been proposed in the past towards this. In this paper the principle of operation, performance, and design aspects of a novel scheme of a vector-locked loop (VLL) for synchronous extraction of the harmonics and or the fundamental from a distorted periodic waveform is briefly described and real-time hardware emulation results are presented. Main features of the VLL are: simplicity, excellent insensitivity to harmonics, noise rejection, availability of both fundamental and harmonics without additional processing, and the good speed of operation. Some results from the real-time hardware emulation of the scheme on a dSPACE-Modular system are presented and compared with the results from MATLAB®/Simulink®.*

Key words: *Harmonic extraction, amplitude-locked loop, active filtering.*

1. Introduction

The extraction of the harmonics and or the fundamental components of voltages and or currents is one of the main process in the implementation of custom power devices. The techniques available can be broadly classified into: single-phase or three-phase, direct or indirect, time-domain or frequency-domain based, and also open-loop or closed-loop techniques. The closed-loop techniques have the distinct advantage of being able to stay synchronised (zero-deviation, amplitude and or phase-locked - to be more precise) to the input, which is very important in

all applications connected to the utility grid. Extracting the fundamental and or the harmonics in a single-phase signal in a closed-loop scheme is the main focus of this paper.

Amplitude locking has been in use in the communication area for the purpose of amplitude modulation and or demodulation. A vector-locked loop was presented in a patent by DaSilva [1] which uses peak-detection in the magnitude detection stage of such a scheme. An amplitude-locked loop was presented in another patent by Pettigrew [2]. Both the aforementioned schemes assume the input to be a sinusoid and hence cannot be used for distorted waveforms.

In the area of synchronised filtering the scheme presented in 1995 by Luo, et al., [3] has the desirable feature of staying locked to the phase-locked loop (PLL) reference and is very simple to understand and implement. However its settling time is a function of the integrator gain, but an increase in the gain to improve dynamic performance, results in increased distortion in the filtered output. Moir [4] has presented an analysis of the amplitude servo, proposed by Pettigrew [2] for the purpose of amplitude demodulation. This has features similar to those of the scheme mentioned above. A vector-locked loop, considered here is capable of locking to the phase and amplitude of the fundamental of the input, to which it is tuned. Such a scheme for synchronous extraction of harmonics and or fundamental was presented for the first time in 2002 by

M. Karimi-Ghartemani, et al., [5]. It was improved by H. Karimi et al., [6] in 2003, where a low-pass filter is introduced in cascade with an integrator. This offers a better steady-state response and reduces the settling-time, while allowing for a higher gain.

A sample of application of adaptive filtering technique for extraction of harmonics can be found in [7], and in [8] and [9] are listed other techniques for the same purpose. A comprehensive but detailed information with applications and comparative evaluation may be found in [10]. A novel VLL for extraction of harmonics has been proposed recently by Ritesh et al., [11].

Indirect Methods: The methods of active filter control in which load currents are not directly used for determining the compensating currents or controlling the Voltage Source Converter (VSC) can be listed under this class. In fact in these methods the extraction of desired compensating currents, its injection, and control of the VSC are integrated. The general rule in these techniques is to determine an effective admittance (conductance), as seen from the source into the load side. This is done either by calculating the power or by regulating the DC bus of the VSC. The methods listed from [12-16] fall into this category. In the method proposed by Sincy et al., [12] the admittances at discrete harmonic frequencies are determined to optimize power factor, while meeting the constraints on active-power supplied and current Total Harmonic Distortion (THD). This is also applicable to the operation under non-sinusoidal supply conditions. A series of papers by Smedley et al., [15] based on *unified constant frequency integration control*, is aimed at the elimination of the need for hysteresis control and the problems associated with it, while attempting to draw Fryze's current from supply [12].

Direct Methods: The general principle in these methods is to use the load currents and the supply voltages, to determine the active, reactive, and harmonic components of load current. Using these, appropriate compensating currents or desired source currents are determined, depending on the requirement. These include the correlation based Fourier-series or Discrete Fourier Transform techniques, Notch filtering, Instantaneous active or reactive power theory based techniques, and Synchronous reference frame theory [17-19]. The applications of Active Filtering are discussed in [20]. Application of ANN techniques to Active Power Filters has been reported in several papers [21-24]. A comprehensive

survey of algorithms for active filtering is presented by Asiminoaei, et al., [25].

The technique presented by Ritesh et al., in [11] has the unique feature that it uses a second-order low-pass filter (SOLF) pre-tuned to a centre frequency (ω_n) for extracting the residual fundamental and dc components to drive the integrator to the amplitude of the fundamental. Thus it renders steady-state and transient performances superior to the techniques known so far. In addition to being used for harmonic extraction in single or three-phase utility systems, it can also be used for amplitude and or frequency demodulation in communication systems.

In this paper a real-time hardware emulation of the scheme on the dSPACE-Modular system is presented. The paper is organized as follows: In Section 2, the operation of the scheme is briefly discussed. The approximate transient analysis and linear time invariant (LTI) model development is presented. Section 3 starts with steady-state analysis. The effects of the parameters of the scheme on the steady-state and transient performances are discussed which leads to design considerations. Moreover, design considerations to achieve optimal performance are discussed. Real-time hardware emulation setup is explained in Section 4 and experimental results are presented in Section 5. Conclusions are presented in Section 6.

2. The Structure and operation of VLL

The structure of the VLL is shown in Fig. 1. It has two locked-loops: a phase-locked loop for phase and frequency synchronization and a novel amplitude-locked loop for fundamental amplitude determination. The input,

$$x_I(t) = \sum_{k=1}^{\infty} C_k \sin(k\omega_o t + \phi_k) \quad (1)$$

is a periodic waveform with no dc component. The output of the PLL (pre-tuned to a free-running frequency of ω_o) which is purely sinusoidal, is given a 90° phase shift in order to bring it in phase with the fundamental component of the input. Thus,

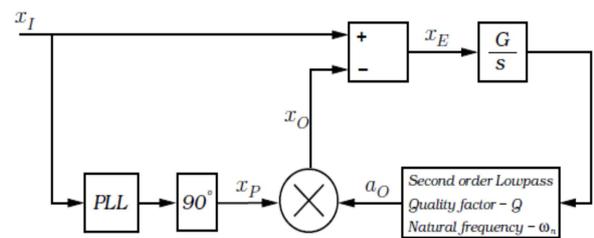


Fig. 1. Block diagram of proposed VLL

$$x_p(t) = B_p \sin(\omega_0 t + \phi_1). \quad (2)$$

The essential idea is to compare the instantaneous values of the input, x_I and the output, x_O (scaled version of x_P) and to adjust the scaling factor (a_O) by feedback in order to minimize the error of the fundamental in x_E . The integrator and the second-order low-pass filter (SOLF) are chosen such that the above operation is performed only on the fundamental component of x_I , thereby desensitizing the loop to all harmonics. Therefore in steady-state, the output x_O exactly locks-on to the fundamental component of x_I (both phase and amplitude) and the signal x_E is the sum of all harmonic components in x_I . In other words, a_O settles to a dc (A_O) such that $A_O B_P$ is the amplitude of the fundamental component of x_I . The integrator gives the additional advantage of zero steady-state error. The SOLF used here has the standard form as given in (3).

$$H(s) = \frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{Q\omega_n} + 1} \quad (3)$$

The characteristics of the SOLF are as shown in Fig. 2, for the purpose of aiding the explanation. It should be noted here that the parameters chosen for the SOLF achieve the following, which are important

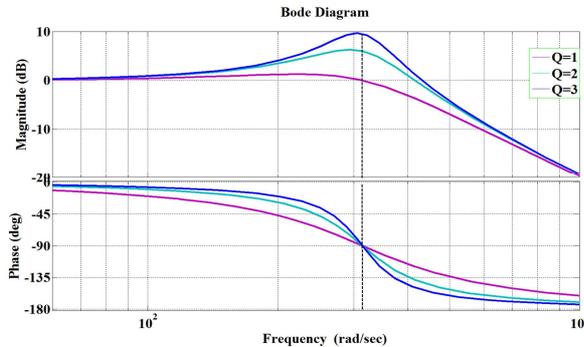


Fig. 2. SOLF Characteristics

and necessary in the operation of the algorithm:

1. SOLF filters out the higher order harmonics at a rate of -40dB/decade.
2. It helps in amplifying the residual fundamental by a gain depending on the choice of Q , which determines the peak of the magnitude plot at ω_n .
3. It also provides 90° phase lag at ω_n which is required for achieving 180° phase-lag for optimum negative feedback.

The features 2 and 3 are very crucial and distinct from a flat frequency response. These will be explained in the following section.

It is shown [11] that the dc component in the error signal x_E is,

$$X_E(t) = -\frac{G_{IP}G}{2\omega_0} [C_1 - A_O(t)] \cos(\phi_0) \quad (4)$$

where $A_O(t)$ is the time varying dc component in $a_O(t)$ and G_{IP} is the gain of the SOLF at ω_0 . Since this signal directly feeds the integrator, it sets the rate at which the integrator output changes and therefore decides how fast $A_O(t)$ reaches C_1 . The difference $[C_1 - A_O(t)]$ must result in a dc error component with the same sign, so as to ensure corrective action through negative feedback. From (4), it follows that $\cos(\phi_0)$ must be negative and as large as possible (in magnitude) to achieve dc negative feedback and minimum settling time respectively. The optimal criterion which meets the above requirements is $\cos(\phi_0) = -1$ or $\phi_0 = \pm 180^\circ$ which leads to,

$$\phi_0^{opt} = \underbrace{\text{SOLF lag}|_{\omega_0=\omega_n}}_{-90^\circ} + \underbrace{\text{integrator lag}}_{-90^\circ}. \quad (5)$$

For values of ω_0 different from ω_n (within certain limits), the loop performs sub-optimally.

2.1 Approximate LTI model

A LTI model is useful for stability analysis and for the purpose of designing for optimal performance. The model must provide some rules for tuning the parameters- G and Q . An approximate but comprehensive and lucid approach is followed in [11]. It is obtained for analysing the effect of variations in the fundamental input amplitude identified by $C_1(t)$. It takes into account only the effect of the dc component produced by the fundamental error signal. The effects of higher frequencies are neglected on the assumption that they are sufficiently attenuated by the SOLF-integrator combination.

At any instant of time, the dc component in x_E is given by (4). When ω_0 is sufficiently close to ω_n , $G_{IP} \approx Q$ and $\phi_0 \approx -180^\circ$. This implies from (4),

$$X_E(t) = \frac{QG}{2\omega_0} [C_1(t) - A_O(t)]. \quad (6)$$

Taking Laplace transform of (6) and with further manipulation and simplification it is shown [11] that,

$$\frac{A_O(s)}{C_1(s)} = \frac{1}{\frac{s^3}{G^2Q\omega_0/2} + \frac{s^2}{G^2Q^2/2} + \frac{s}{G^2Q/2\omega_0} + 1}. \quad (7)$$

Following observations are made here:

- when the input is sinusoidal with constant amplitude, VLL output closely follows that of the fundamental of the input. In other words, the signal a_o will be predominantly a dc quantity.
- when the input amplitude is modulated at sufficiently low frequencies (ω_m), the output amplitude manages to follow closely. The linear time-invariant model *exactly* represents the system for such inputs.
- a feedback architecture for the same presented in [11] is as shown in Fig. 3.
- Fig. 3, can assist designers in the application of LTI control system techniques for optimizing its tracking abilities.

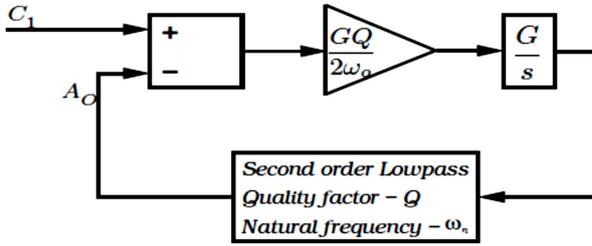


Fig. 3. Equivalent LTI Model

- stability analysis cannot be conducted using the model shown in Fig. 3, because it has not captured the time variant nature of the VLL. Hence experimental approach is followed [11]. The region of stability in the G-Q plane is shown in Fig. 4. The designer can choose G and Q so that the operating point lies only within the stable region.

3. Design consideration

A good PLL is a pre-requisite for the operation of the scheme and hence its design is very important. Its performance can be optimized by well-

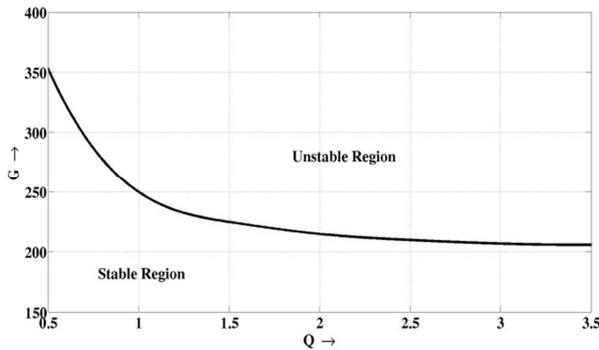


Fig. 4. Equivalent LTI Model

established techniques [26]. Several schemes are presented in the literature concerning the design of PLL with application to power system under distorted and variable frequency conditions [27-32].

In the current discussion a few thumb-rules [11] are presented for designing the VLL. The designer may arrive at a more optimized VLL by fine-tuning the system through computer simulations after following these general rules. Basically, tracking ability (in magnitude and speed or phase) represented by the phase angle θ between $A_o(t)$ and $C_1(t)$ is taken as the key factor in developing the rules. Consider an input modulated by,

$$C_1(t) = C_o + C_m \sin(\omega_m t) \quad (8)$$

where C_o is the dc part of C_1 and C_m is the amplitude of the sinusoidal modulation with modulation frequency ω_m .

3.1 Choice of G

The sensitivity of G w.r.t. θ is shown in [11] to be,

$$\frac{\partial \theta}{\partial G} = -\frac{4\omega_o \omega_m}{Q} \frac{1}{G^3} \quad (9)$$

From (9), it follows that the sensitivity of the phase lag to variations in G is low when G is large. Therefore in practical systems, it is advisable to include a high gain in the loop for quicker response, small phase-lag, and to increase the overall robustness of the system.

3.2 Choice of Q

The sensitivity of θ with respect to variations in Q is given by,

$$\frac{\partial \theta}{\partial Q} = \frac{-2\omega_o \omega_m}{G^2} \frac{1}{Q^2} \quad (10)$$

From (10) one may conclude that sensitivity of phase lag to variations in Q is low when Q is high and that a high value of G already ensures low sensitivity. However, it is not advisable to have a very large Q since the system becomes highly oscillatory and settling-time increases. Also, a higher Q translates to a lower range of ω_o over which $\phi_o \approx -180^\circ$ (criterion for optimal performance). This can be observed from the phase plot in Fig. 2. Therefore the quality factor of the SOLF has a dominant effect on the settling time of the system and also on the dynamic range of input frequency.

4. Real-time Emulation

The algorithm is tested on real-time simulation plat-form. The system description is as follows.

4.1 Description of the system

The dSPACE modular system is shown schematically in Fig. 5. It consists of a processor board (DS1006), DS2002 - a 32 channel A/D board

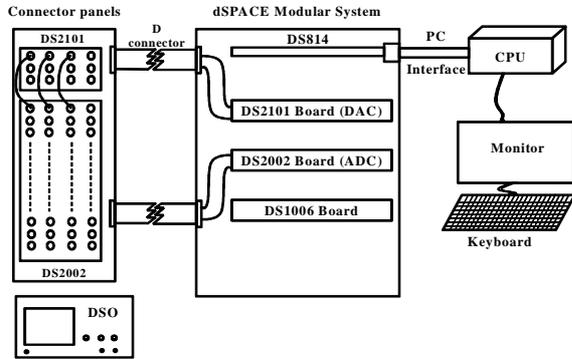


Fig. 5. Schematic of the Hardware setup

and DS2101 - a 5 channel D/A board, and a DS814 - optical communication interface card. All these are mounted on a PHS bus in a modular box. A connector panel kept outside provides for connecting inputs and outputs.

4.2 Emulation setup

The emulation setup is shown in Fig. 6. The system to be emulated in real-time is modelled and simulated in MATLAB[®]/Simulink[®]. Input and

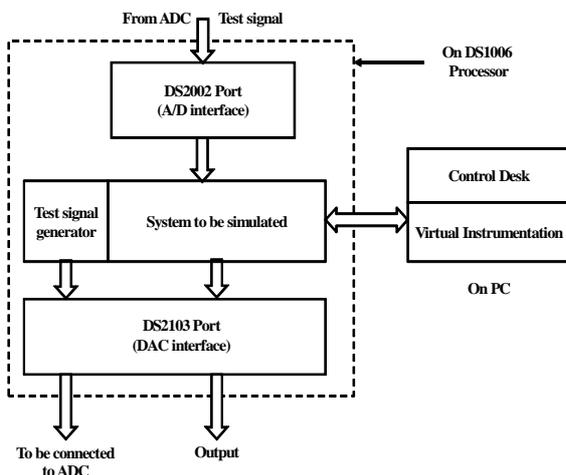


Fig. 6. Real time hardware-emulation setup

output ports are appropriately selected from the Real Time Interface library of the dSPACE-Modular system. The A/D and D/A cards provide the necessary interface to the external system. Matlab generates the code for the system, which can be downloaded into the processor in Modular system.

The system comes with Control Desk- a Graphical User Interface and the Virtual Instrumentation for the system. The simulation setup and signal capturing and or observing can be carried out in Control Desk. In Fig. 7 a snapshot of the hardware setup used for real-time emulation is shown.

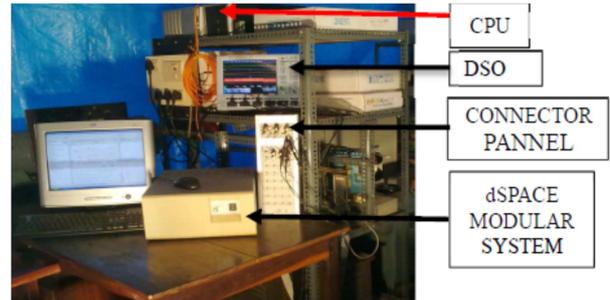


Fig. 7. Hardware Setup

5. Real-time hardware emulation

Extensive simulation studies were conducted on the proposed VLL using MATLAB[®] and Simulink[®]. The system is designed for a specific natural frequency (i.e., 50Hz), and to meet the requirements of, harmonic extraction and tracking amplitude modulation. Hence various features of the system with $\omega_n = 100\pi$ rad/s, $Q = 2$, and $G = 180$ were explored for different inputs. The model of the algorithm is run on the dSPACE- Modular system with fixed step sizes of 20 μ s, 50 μ s, and 100 μ s. With minor tuning in the controller parameters for each case, all cases gave satisfactory results, comparable with the off-line simulation. The results for 50 μ s are presented in Fig. 8 to Fig. 12, which are snapshots obtained from the Control Desk of the dSPACE system.

5.1 Response to Step Input

The real-time hardware emulation result of the VLL and the LTI model for a step change of +0.5 in the fundamental input amplitude at $t = 0.2$ s is shown in Fig. 8. The purpose of this test is to estimate the settling time of the system and to compare it with the response from the LTI model. The input for the proposed VLL is,

$$x_1(t) = 0.5[u(t) + u(t - 0.2)] \sin(100\pi t) \quad (11)$$

Hence the input to the LTI model is $C_1(t)$ which is,

$$C_1(t) = 0.5[u(t) + u(t - 0.2)]. \quad (12)$$

It is observed that the output settles to steady-state within 2% error, in about three cycles of fundamental. As observed in Fig. 8, the settling time for the LTI model is matching with of the

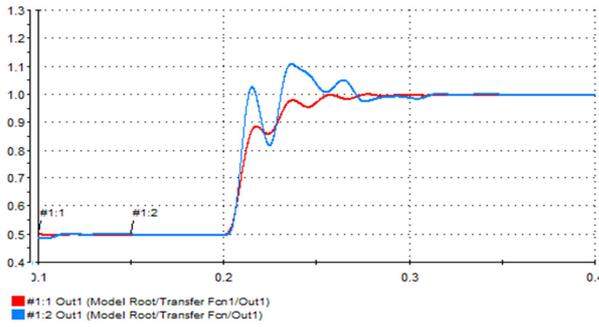


Fig. 8. Step Response to Fundamental amplitude
(x- axis: time in seconds, y-axis: signal value)
Legend: blue- Actual system, red- Equivalent LTI system

original system.

5.2 Response to Input Amplitude modulation

The VLL performance was also investigated for an amplitude modulated sine-wave as given in (8) with $C_O = 1$, $C_m = 0.2$ and $\omega_m = 4\pi$ rad/s. Hence,

$$x_I(t) = [1 + 0.2 \sin(4\pi t)] \sin(100\pi t). \quad (13)$$

Fig. 9 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the

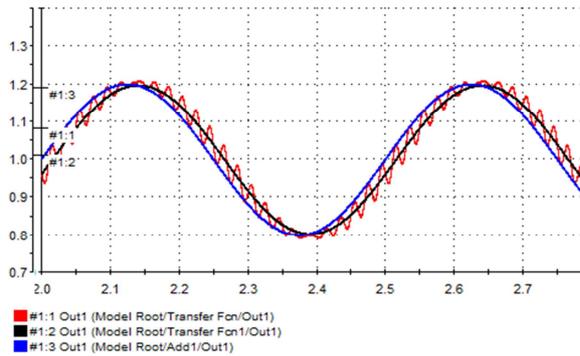


Fig. 9. Comparison of LTI model response and actual.
(x- axis: time in seconds, y-axis: signal value)
Legend: purple- input, black- output from LTI equivalent system, red- out put from actual system

negligible phase-lag in a_O and also the exactness of the LTI model. It is useful to remember that a_O is the instantaneous amplitude of the output, to meaningfully interpret the results. The discrete Fourier series (DFS) of the ripple in a_O revealed the presence of 48Hz and 52 Hz components [11].

5.3 Noise Rejection

Simulation studies on the noise rejection capabilities of the VLL were conducted. Fig. 10 shows the input, which is a sine wave of 100π rad/s with band-limited white noise, and the corresponding output.

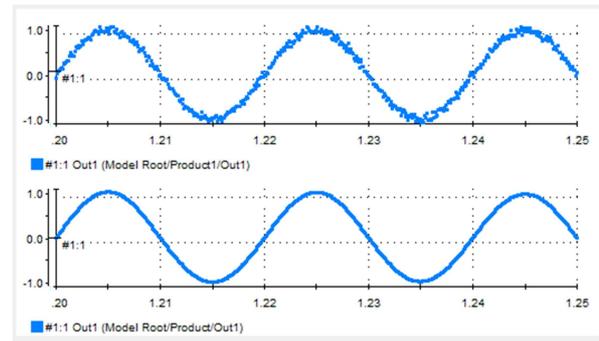


Fig. 10. Response to input with Noise
(x- axis: time in seconds, y-axis: signal values)
Legends: top- input, bottom- output

For an input signal-to-noise-and-distortion ratio (SNDR) of 7 dB, the output SNDR was observed to be 26.3 dB.

5.4 Harmonics Attenuation

Studies on distortion of the output in the presence of harmonics in the input signal are shown in Fig. 11. The applied input is a square-wave of unit amplitude and a frequency of 50 Hz.

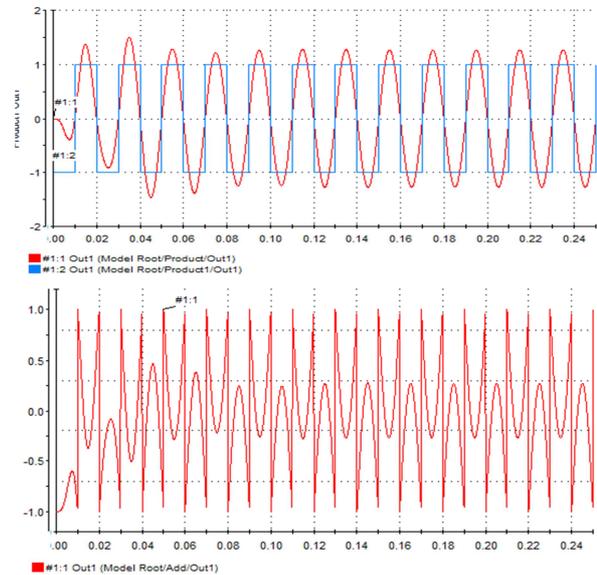


Fig. 11. Filtering for a square wave input
(x- axis: time in seconds, y-axis: signal value)
Legends- Top: blue- input, red- output
Bottom: Filtered harmonics

5.5. Frequency Spectrum

An FFT analysis of an integral number of cycles (which results in the Discrete Fourier Series) of the input and the output is conducted after capturing the data in the Control desk. The results are plotted in

Fig. 12. It can be seen that there is good amount of attenuation of the harmonics in the output. This matches with that of the simulation results.

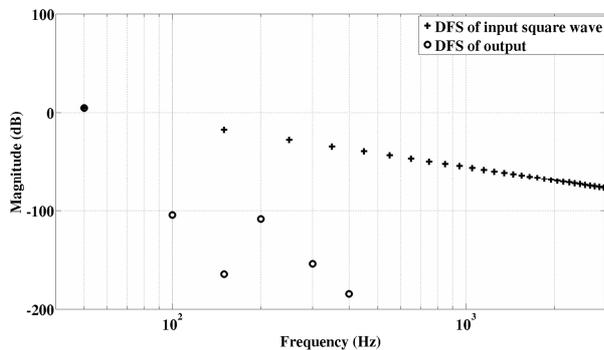


Fig. 12. Frequency spectrum analysis for a square wave input

5.6. Performance under conditions of varying supply frequency

The scheme gives satisfactory performance under conditions of varying supply frequency. It is tested for supply frequency variation in the range of 45 Hz to 55 Hz at a rate of 5 Hz/s. The frequency is maintained constant at 50 Hz until 1s. It is then decreased to 45 Hz over a duration of 1s and then ramped-up to 55 Hz over a duration of 2s. It is observed that the scheme tracks the variation in frequency and produces a clean fundamental of amplitude equal to $4/\pi$ - the value corresponding to the fundamental in a square-wave of unit amplitude. The clippings of the results at different instants of time during the variation of frequency are as shown in Fig. 13.

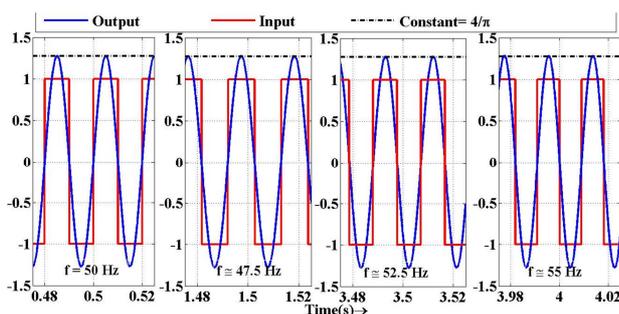


Fig. 13. Performance of the scheme under conditions of varying supply frequency

6. Conclusions

The real-time hardware emulation results of a novel scheme for obtaining synchronized selective-frequency amplitude-locking on distorted signals is presented. A brief explanation for the working of the algorithm is given and the design rules are presented. The results of real-time hardware emulation truly

match with that of the simulation results [11]. It has features similar to a PLL. The scheme has several desirable features like: the transient response is better (about three cycles), has excellent insensitivity to harmonics, and noise rejection. It can find applications in: synchronous separation of the fundamental and the harmonics in a distorted periodic waveform, amplitude and frequency tracking, noise rejection, and amplitude demodulation or peak detection. It also performs satisfactorily under conditions of varying supply frequency.

Its real-time implementation results compare well with the off-line simulation and hence confirm the possibility of its application in Active Power Filtering of harmonics in power systems.

7. References

1. DaSilva, M. K.: *Vector locked loop*. USA Patent No. 5,105,168(1991), USA, 1991.
2. Pettigrew, A. M.: *Amplitude locked loop circuits*, United Kingdom Patent No. 5,341,106(1994), UK, 1994.
3. Shiguo, L., Zhencheng, H.: *An adaptive detecting method for harmonic and reactive currents*. In: IEEE Transactions on Industrial Electronics, Vol. 42(1995), No. 1, February 1995, p. 85-89, USA.
4. Moir, T. J.: *Analysis of an amplitude-locked loop*. In: IET Journals, Electronic Letters, Vol. 31(1995), No. 9, April 1995, p. 694-695, USA.
5. Karimi-Ghartemani, M., Iravani, M. R.: *A nonlinear adaptive filter for online signal analysis in power systems applications*. In: IEEE Transactions on Power Delivery, Vol. 17(2002), No. 2, April 2002, p. 617-622, USA.
6. Karimi, H., Karimi-Ghartemani, M., Iravani, M. R.: *An adaptive filter for synchronous extraction of harmonics and distortions*. In: IEEE Transactions Power Delivery, Vol. 18(2003), No. 4, October 2003, p. 1350-1356, USA.
7. Han, B., Bae, B.: *Novel Phase-locked loop using Adaptive Linear Combiner*. In: IEEE Transactions Power Delivery, Vol. 18(2006), No. 1, January 2006, p. 513-514, USA.
8. Singh, B., Al-Haddad, K., Chandra, A.: *A New Control approach to three-phase Active Filter, for harmonics and Reactive Power Compensation*. In: IEEE Transactions on Power Systems, Vol. 13(1998), No.1, February 1998, p. 133-138, USA.
9. Ghosh, A., Joshi, A.: *A new approach to load balancing and power factor correction in power distribution system*. In: IEEE Transactions on Power Delivery, Vol. 15(2000), No. 1, January 2000, p. 417-422, USA.
10. Akagi, H., Watanabe, E. H., Aredes, M.: *Instantaneous power theory and applications to power con-*

- ditioning. John Wiley & Sons, Inc., Hoboken, New Jersey, 2007.
11. Bhat, R. A, Gonda, J. M., David, S.: *A Novel Vector-Locked Loop Scheme for Synchronized Extraction of Harmonics*. In: Proceedings of 5th International Conference on Information and Automation for Sustainability(ICIAfS-2010), December 17-19, 2010, COLOMBO, SRI LANKA, p. 447-452.
 12. Sincy, G., Vivek, A.: *A Novel, DSP based algorithm for optimizing the harmonics and reactive power under non-sinusoidal supply voltage conditions*. In: IEEE Trans. on Power Delivery, Vol. 20(2005), No. 4, October 2005, pp: 2526-2534, USA.
 13. Kishore, C., Fernandes, B. G., Dubey, G. K.: *An Instantaneous Reactive Volt-Ampere Compensator and Harmonic Suppressor System*. In: IEEE Trans. on Power Electronics, Vol. 19(1999), No. 2, March 1999, pp: 381-392, USA.
 14. Shyh-Jier H., Jinn-Chang, W.: *A Control Algorithm for Three-Phase Three-Wired Active Power Filters under Nonideal mains Voltages*. In: IEEE Trans. on Power Electronics, Vol. 14(1999), No. 4, July 1999, pp: 753-760, USA.
 15. Chongming, Q., Taotao, J., Keyue, M. S.: *One-Cycle Control of Three-Phase Active Power Filter with Vector Operation*. In: IEEE Transactions Industry Applications, Vol. 51(2004), No. 2, April 2004, p. 455-463, USA.
 16. Chattopadhyay, S., Ramanarayanan, V.: *Phase-Angle Balance Control for Harmonic Filtering of a Three-Phase Shunt Active Filter System*. In: IEEE Transactions Industry Applications, Vol. 39(2003), No. 2, March/ April 2003, p. 565-574, USA.
 17. Victor M. Moreno, Alberto Pigazo Lopez, Ramon Ignacio Diego Garcias: *Reference Current Estimation under Distorted Line Voltage for Control of Shunt Active Power Filters*. In: IEEE Trans. on Power Electronics, Vol. 19, No. 4, July 2004, p. 988-994
 18. Paolo Mattavelli: *A Closed-Loop Selective Harmonic Compensation for Active Filters*. In: IEEE Transactions Industry Applications, Vol. 17(2001), No. 1, January/ February 2001, p. 81-89, USA.
 19. Bhattacharya, S., Andrè Veltman, Devan, D. M., Robert D. Lorenz: *Flux-Based Active Filter Controller*. In: IEEE Transactions Industry Applications, Vol. 32(1996), No. 3, May/ June 1996, p. 491-502, USA.
 20. Akagi, H.: *Active Filters and Energy Storage Systems for Power Conditioning in Japan*. In: JEE, Vol. 6(2006), No.3, p. 26-35, Romania.
 21. Allag, A., M.Y. Hammoudi, S.M. Mimoune: *Adaptive Nonlinear Control of Three-phase Shunt Active Power Filter with Uncertainties*. In: JEE, Vol. 7(2007), No.2, p. 26-32, Romania.
 22. Lamchich, M.T., Raoufi, M.: *A Fuzzy Logic Based Controller for Shunt Power Active Filter*. In JEE, Vol. 8(2008), No.2, 2008, p. 70-75, Romania.
 23. Hamoudi, F., A. Chaghi, M. Adli, H. Amimeur, E. Merabet: *Adaptive Fuzzy-Hysteresis Band Current Controller for Four-wire Shunt Active Filter*. In: JEE, Vol. 8(2008), No.3, p. 11-17, Romania.
 24. Suja, S., J. Jerome: *Adaline Based Frequency and Harmonic Estimation*. In: JEE, Vol. 9(2009), No.1, 2009, p. 70-76, Romania.
 25. Asiminoaei, L., Blaabjerg, F., Hansen, S.: *Detection is key - Harmonic detection methods for active power filter applications*. In: IEEE Transactions on Industry Applications Magazine, Vol. 13(2007), No.4, July-Aug. 2007, p. 22 – 33, USA.
 26. Egan, W. F.: *Phase-Lock Basics*. John Wiley & Sons, Inc., Hoboken, New Jersey, 2007.
 27. Vikram, K., Vladimir, B.: *Operation of a Phase Locked Loop System under Distorted Utility Conditions*. In IEEE Transactions on Industry Applications, Vol. 33(1997). No. 1, January/February 1997 p. 1576 – 1584, USA.
 28. Rodriguez, P., Josep, P., Joan, B., Candela, J. I., Ronaldo, P. B., Dushan, B.: *Decoupled Double Synchronous Reference Frame PLL for Power Converters Control*. In: IEEE Transactions on Power Electronics, Vol. 22(2007), No. 2, March 2007, p. 584 – 592, USA.
 29. Karimi-Ghartemani, M., Reza Iravani, M.: *A Method for Synchronisation of Power Electronic Converters in Polluted and Variable-Frequency Environments*. In: IEEE Transactions on Power Systems, Vol. 19(2004), No. 3, August 2004, p. 1263 – 1270, USA.
 30. Rodriguez, P., Luna, A., Coibotaru, M., Teodorescu, R., Blaabjerg, F.: *Advanced Grid Synchronisation System for Power Converters under Unbalanced and Distorted Operating Conditions*. In: Proceedings of IEEE Industrial Electronics Conference (IECON'06), Nov., 6-10, 2006, Paris, p. 5173-5178.
 31. Blaabjerg, F., Teodorescu, R., Marco, L., Adrian, V. T.: *Overview of Control and Grid Synchronisation for Distributed Power Generation Systems*, In: IEEE Transactions on Industrial Electronics, Vol. 53(2006), No. 5, October 2006 p. 1398 – 1409, USA.
 32. Ciobotaru, M., Agelidis, V.G., Teodorescu, R., Blaabjerg, F.: *Accurate and Less-Disturbing Active Antiislanding Method Based on PLL for Grid-Connected Converters*. In: IEEE Transactions on Power Electronics, Vol. 25(2010) , No. 6, June 2010 p. 1576 – 1584, USA.