# SINGLE SWITCH HIGH GAIN ISOLATED DC-DC CONVERTER WITH ACTIVE CLAMP

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***Abstract:*** *— In this paper, an isolated high gain single switch dc-dc converter is proposed. In the proposed converter, high step-up voltage is obtained by single power switching technique that operates appropriate duty cycle with isolated transformer inductors, switched capacitor and power diodes. It alleviates the conventional converters high duty ratio and high voltage stress on power devices. The proposed converter eliminates the switching losses by the method of series resonance soft switching with an active clamp. To achieve high output voltage gain, the isolated transformer primary and secondary terminals are connected in series during switching operation. The proposed scheme experimented with solar cell characteristic. PSIM software has been used for simulation. The operation is verified by simulation and validated by implementing in the hardware model at 40Vdc/400Vdc, 100kHz, 500Watts.*

***Key words:*** *Single Switch, DC-DC Converter, Active Clamp, Reverse-recovery, Solar cell.*

## 1. Introduction.

Photovoltaic (PV) is the direct transformation of solar energy into electricity. Solar energy become one of the main contributors in the future energy crises. The renewable energy has several advantages such as pollution-free power generation, low maintenance cost, low operation cost and supply limitations. PV systems helps further technology improvement and cost reduction along the value chain [2]. PV technology is not only to improve the efficiency of the cells but also of the modules and hence it make it more feasible for various applications [3]. PV electricity is one of the best options for sustainable future energy requirements of the world. The present PV market is growing at the very high market [4]. In recent years, the high step up dc-dc converters have played a vital role in renewable energy applications. The low voltage renewable energy source, in order to connect them to the grid, the voltage level is adjusted according to the electrical network standards in the countries [19]. Earlier the environmental issues have accelerated the use of more efficient and energy saving technologies in renewable energy systems [20]. The boost converters are needed for increasing low dc voltage to high dc voltage. The conventional boost converters are not preferred, because with high voltage duty ratio, it causes severe losses in power devices and high voltage stress across the switching devices, which generate high conduction losses, thus resulting in the increase of complicity. To avoid these problems, the isolated high step-up single switch dc-dc converter with new single switching technique proposed [1] and improved version of this converter are analyzed in this paper. To eliminate the high duty cycle, capacitor switching technology is used [13]. To reduce the stress on the active switch resonant boost converter for photovoltaic application is proposed [5]. Active switch method is adopted to increase the voltage gain and efficiency and a Z-source based topology that can boost the input voltage to desired level with low voltage stress [6]. The input current doubler and output voltage doubler are suitable for better performance in fuel cell power system [7]. The coupled inductors can provide high voltage gain, but their efficiency is degraded by the losses associated with leakage inductors [11].

The conventional boost converters are not able to provide high voltage gain [8]. High voltage gain with high efficiency can be achieved by the intergraded boost flyback converter system [9]. The investigation of high-efficiency clamped voltage dc-dc converter with reduced reverse-recovery current and switch-voltage stress and designed by way of the combination of inductor and transformer to increase the corresponding voltage gain [10]. To reduce high device stress and large transformer size, a high efficient pulse width modulation resonant single switch isolated converter is proposed [18]. To achieve high output voltage gain and soft switching in the flyback converters the active clamp is utilized [15].

The passive lossless clamp circuit is implemented instead of an active clamp circuit to recycle the leakage energy, also simpler and easier to design [12]. The active clamp circuit shows better performance but in passive clamp circuit reduces the circuit complexity when compared to active clamp circuit. A switched capacitor circuit can achieve any voltage ratio, allowing for a boost of the input voltage to high values [13]. Isolated high boost dc-dc converters are suitable for renewable energy source. The photovoltaic panel can be integrated with high efficiency dc-dc converter and single phase inverter in the power conditioning system by using MPPT [14]. High boost isolated dc-dc converter with closed loop control can provide high voltage regulation control suitable for renewable energy source [17]. Further, this work can be proposed

for the efficiency optimization and digital control of the dc-dc converter over wide ranges of operating conditions [16]. The overall performance of the renewable energy system is affected by the efficiency of step-up dc-dc converters, which are the key parts in the system power chain. Earlier the comparison and discussion of different high efficiency dc-dc step-up topologies performed [19]. And comparison of the synchronous-rectified push–pull converter with LLC dc-dc converter was deeply analyzed [21]. High power high efficiency boost dc-dc converters for the use in photovoltaic, fuel cell systems are discussed in view of power losses and efficiency [22].

In this paper, an isolated high step-up single switch dc-dc converter is proposed and implemented. In the proposed, converter high step-up voltage is obtained by single power switching technique operating low duty cycle with isolated transformer inductors and switched capacitors and power diodes. The proposed converter eliminates the switching losses and recycles the leakage energy. The isolated transformer primary and secondary terminals are connected in series during switching operation. The output of the boost converter and isolated switched-capacitor cell are connected in series for high step-up with a low turn-on ratio which has already been discussed [12]. The proposed converter alleviates the conventional converters high duty ratio and high voltage stress on power devices. The proposed converter eliminates the switching losses by the method of series resonance soft switching. PSIM software has been used for simulation. Simulation circuit is analyzed at 40Vdc/400Vdc, 500Watts and this operation is validated by implementing in hardware model at 40Vdc/400Vdc, 500Watts with the switching frequency 100kHz.

## 2. Proposed Circuit and Operation.

The block diagram of the proposed isolated high step-up converter with single power switch is shown in Fig1. The block diagram shows the input PV model, high frequency isolated transformer, power capacitors and power diodes with single power switch. The single power switch is controlled through the controller dSPACE. The output is connected with the resistive load model.

The proposed converters operates in six modes the circuit diagram of these modes is shown in the Fig3 to Fig8. The active lossless clamped circuit is proposed. The clamped capacitor ($C_c$) and clamp diode ($D_c$) connected across IGBT switch to reduce the voltage stress. The $V_c$ is the clamped capacitor voltage. The clamp circuit recycles the energy stored in the leakage inductance. The voltage gain is obtained by significant value by providing a switched capacitor ($C_{sc}$) and secondary inductor $L_s$ and switched diode ($D_s$). The switched capacitor voltage is given by $V_{sc}$. The output diode ($D_o$) current is $I_o$. The topology is modeled with an ideal transformer with corresponding turns ratio (n) equal to $n_2/n_1$. $L_m$ is the magnetizing inductor $L_k$ is the leakage inductance. $I_{LK}$ is the leakage inductance current. $V_d$ is the output diode stress. Hence, here the fast recovery diode used the capacitance effect of the depletion layer of the diodes neglected even reverse-recovery interval. The circuit is operated in six operating modes as explained below. The key operating waveforms are sketched in Fig2. $V_{ce}$ and $I_e$ are switch collector to emitter voltage and current. $I_s$ - is the isolated transformer with secondary current. The clamp diode current is named as $I_{dc}$ and clamp capacitor current named as $I_c$.

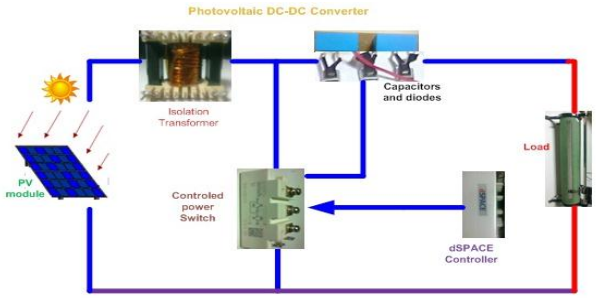


Fig.1. Block diagram of the proposed PV DC-DC Converter

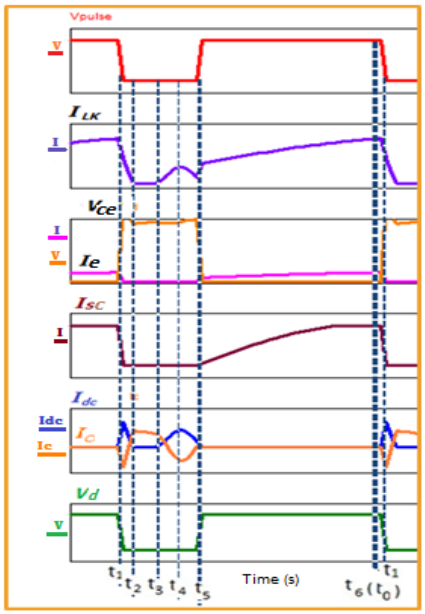


Fig.2. Proposed converter operating waveforms

*Mode I*

The circuit shown in Fig3. is mode-I ($t_o$-$t_1$) operation of the proposed converter. The active switch(S) is turned ON state, the output diode $D_o$ and clamp diode $D_c$ are operating in reverse bias and turn OFF. The magnetizing inductor ($L_m$) is energized by switched capacitor ($C_s$) which energy is already stored in the previous cycle. The source ($V_{in}$) the magnetizing current $i_{lk}$ linearly increases. $L_s$ and $L_p$ inductors are connected via clamp diode $D_c$. The current flow through the secondary winding is controlled by leakage inductor $L_k$ and $i_{lk}$ is given by,

$$\frac{V_{in}(t_1-t_o)}{L_m+L_p} \approx i_c(t_1)-I_c(t_o) \approx i_{Lk}(t) \quad (1)$$

The voltage equation is given by

$$V_{in}=V_{LK}(t_o-t_1)+\frac{V_{CS}}{n} \quad (2)$$

*Mode II*

The circuit shown in Fig4. is mode-II ($t_1$-$t_2$). When switch is turned OFF at $t_1$. The input current as the two path via clamp diode ($I_{dc}$). Switching voltage is clamped to the capacitor voltage. $L_k$ resonate with clamp diode current ($I_c$) and clamped capacitor ($C_c$). So that the current through the leakage inductor $i_{lk}$ linearly decreases through the secondary winding. $L_k$ is discharged by the clamped capacitor voltage $V_c$.

$$\frac{V_C(t_1-t_2)}{L_k}-I_{Lk}(t_1) \approx i_{Lk}(t) \quad (3)$$

*Mode III*

During mode-III ($t_2$-$t_3$) Fig5 the secondary winding current is down to zero, then the switched capacitor $C_s$ employs throughout this period. The voltages of switched capacitor and clamped diode current stay simultaneous, then switched capacitor is resonate with leakage inductor, switched capacitance decreases, but at the same time leakage inductor current $i_{lk}$ decreases. The secondary transformer current ($I_s$) is started raising. $D_o$ and $D_c$ carries the same current.

$$I_{Lk}(t_2)-\frac{V_o-V_c(t_3)}{L_k} \approx i_{Lk}(t) \quad (4)$$

*Mode IV*

Mode-IV ($t_3$-$t_4$) is shown in Fig6. Here, the switch is being turned OFF, the voltage across the switched capacitor is high and then the diode $D_o$ is operated. The magnetizing inductor ($L_m$) releases the stored energy and sends its energy to load, and clamp diode discharge energy when secondary magnetizing energy weakens and the parasitic capacitance of all the diodes is thus neglected as shown in Fig6.

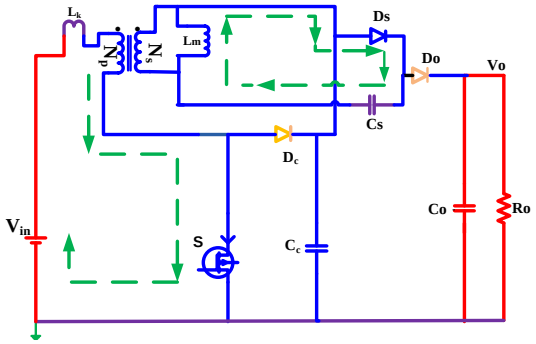


Fig.3. Proposed converter Mode 1 operation circuit

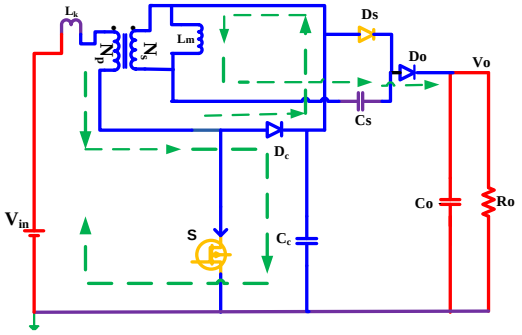


Fig.4. Proposed converter Mode 2 operation circuit

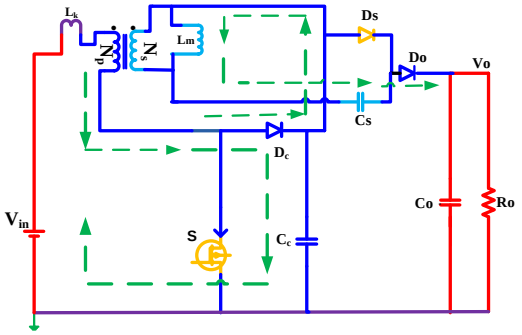


Fig.5. Proposed converter Mode 3 operation circuit.

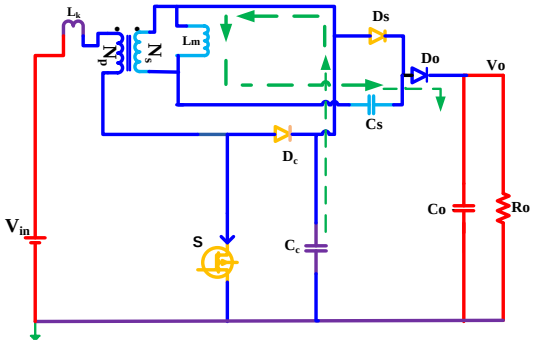


Fig.6. Proposed converter Mode 4 operation circuit

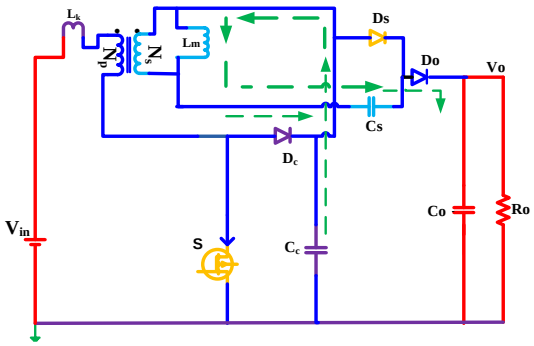


Fig.7. Proposed converter Mode 5 operation circuit.

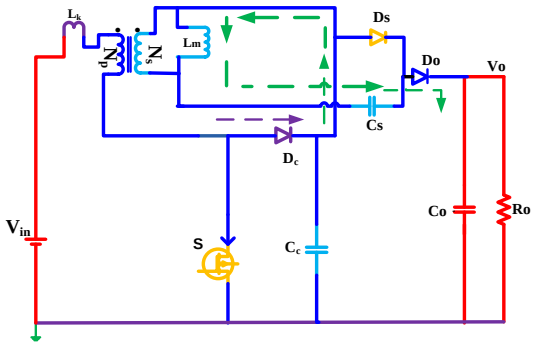


Fig.8. Proposed converter Mode 6 operation circuit.

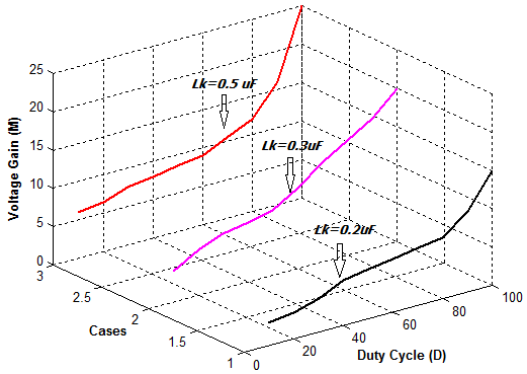


Fig.9. Leakage inductance and voltage gain

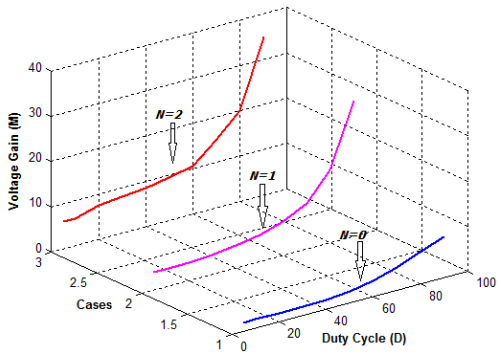


Fig.10. Voltage gain with different turns ratio.

$$\frac{V_o-[V_{Sc}+V_c](t_3-t_4)}{nL_m}+I_{Lm}(t_3)\approx i_{Lm}(t) \tag{5}$$

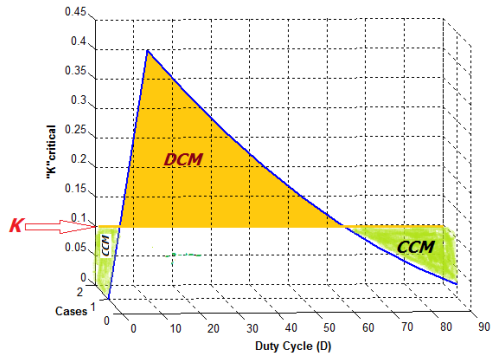


Fig.11. DCM and CCM boundary operation with n=2

Here,

$$n=\frac{n_2}{n_1}=1$$

$$\frac{[L_p+L_m](t_3-t_4)}{nL_p}i_{Lm}(t_3)\approx i_{Lk}(t) \tag{6}$$

The voltage equation from $t_1$ to $t_4$ is given by

$$V_o=(V_c+V_{cs}+n)\times(V_c-V_{Lk(t_1-t_4)}-V_{in}) \tag{7}$$

*Mode V*

In Mode-V ($t_4$-$t_5$) as shown in Fig7 switch leakage inductor ($L_k$) current falls to zero, the magnetizing inductor is discharged linearly. Secondary inductor passes energy to the load through the converter hence $I_s$ decreases. Small charge in magnetizing current is equal to $i_{Lm}$ as given below.

$$\frac{V_o-[V_{sc}+V_c](t_4-t_5)}{nL_m}+I_{Lm}(t_4)\approx i_{Lm}(t) \tag{8}$$

The clamped diode discharges its energy, hence the clamped diode cathode potential is less than the anode and so the diode starts conduct and about resonate the single switch with clamped capacitor.

*Mode VI*

In Fig8, the switch is turned ON ($t_5$-$t_6$), the leakage inductance increases from zero, the switch is turned on by the ZVS condition $V_{ce}$ completely zero, the leakage current is controlled by leakage inductor and the equations are given by

$$\frac{V_{in}+[V_o-V_{sc}(t_5)-V_c(t_5)]}{L_k}(t_5-t_6)\approx i_{Lk}(t) \tag{9}$$

The leakage inductance and the voltage gain relationship are shown in Fig9 with switching frequency 100 kHz and with unity turns ratio. As the leakage inductance increases, the voltage gain of this converter decreases. When leakage inductance increased to a relatively large value, the voltage gain reduces sharply, which increases the switch conduction time and results in large conduction losses.

## 3. Performance analysis

Analysis performed by considering clamped capacitor and switched capacitors are constant and current through the magnetizing inductor ($L_m$) also constant. When the switch is turned on, the $L_m$ is charged by the input voltage is given by,

$$V_{lm}=V_{in} \tag{10}$$

Switched capacitor voltage ($V_{sc}$) can be given by

$$V_{sc} = n \times V_{in} \tag{11}$$

When switch is turned off the $L_m$ is discharged and voltage is expressed by,

$$V_{Lm} = \frac{V_o}{n+1} - V_{in} \tag{12}$$

The voltage gain can be obtained from inductor volt-second balance principle

$$DV_{in} - \frac{V_o}{n+1}(1-D) + V_{in}(1-D) = 0 \tag{13}$$

$$V_{GN} = \frac{V_o}{V_{in}} = \frac{n+1}{1-D} \tag{14}$$

$$V_o = \left(\frac{n+1}{1-D}\right) V_{in} \tag{15}$$

Also the Output voltage can be reanalyzed as follows,

$$DV_{in} - \frac{V_o}{n}(1-D) + \frac{V_c}{n} + \frac{V_{sc}}{n} + \frac{V_d}{n} = 0 \tag{16}$$

$$\frac{nDV_{in}}{(1-D)} + \frac{V_c}{n} + \frac{V_{sc}}{n} + \frac{V_d}{n} = V_o \tag{17}$$

The voltage gain increases greatly when the turns ratio (n) increases. Extreme duty cycle can be designed to optimize the load regulation performance to the proposed isolated high boost dc-dc converter. n=0 is the conventional converter. The voltage gain of the proposed converter is increased greatly by using a proper turns ratio design. The voltage stress of the switch and clamp diode can be written as,

$$V_{stress} = \frac{V_{in}}{1-D} \tag{18}$$

In the circuit design the turn's ratio design plays an important role. By using this, the voltage stress ($V_{stess}$) of the switch is found out and duty ratio is obtained, it is given by

$$n = \left[\frac{(1-D) \times V_o}{V_{in}}\right] - 1 \tag{19}$$

The voltage gain of the converter is gained greatly by using a proper turn's ratio design. Fig10 which shows the relationship between the voltage gains with different turn's ratio at different duty cycle. . From the comparison curve with various turns ratio (n) ranges proposed converter voltage gain higher than that of the conventional boost converter with the same duty cycle.

The output capacitors are used as filter and the aim is to reduce the ripples in the capacitors. The relationship between the output power and voltage ripple is given by

$$C = \frac{P_o}{V_o \times \Delta V_c \times f_s} \tag{20}$$

$$P_o = V_o \times \Delta V_C \times C \times f_s \tag{21}$$

In the above equation, $\Delta V_c$ is voltage ripple on the capacitor $C_c$ or $C_s$. $\Delta V_c$ it assumed as 2%. The proposed dc-dc converter is defined as low loss converter. The efficiency of the converter is the ratio of the output power to the input power. The input power is the sum of the output power and the losses of the individual device.

$$P_{mos} = P_{sw(cond)} + P_{sw(off)} \tag{22}$$

$$P_i = P_o + P_{switch} + P_{diode} + P_{others} \tag{23}$$

Thus the efficiency expression is

$$\eta = \frac{P_o}{P_o + P_{switch} + P_{diode} + P_{others}} \tag{24}$$

Table 1
Simulated values

| *S.No.* | *Parameters* | *Specification* |
|---|---|---|
| 1 | DC voltage input | 38 V – 44 V |
| 2 | DC voltage output | 403 V |
| 3 | Output power (max) | 500 W |
| 4 | Switching Frequency | 100 kHz |
| 5 | Output current | 1.25 A |
| 6 | Output Voltage ripple | 0.3V |
| 7 | Turns ratio (n) | 1:2 |

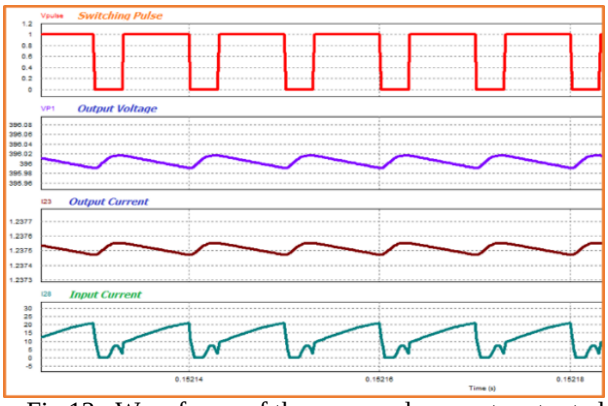

Fig.12. Waveforms of the proposed converter at rated input voltage (40V)

## 4. Boundary operating condition between DCM and CCM

The proposed converter output analysis by applying voltage-second balance to mutual inductance ($L_m$), relationship between the main duty cycle (D) and output diode's conduction time ratio is determined as

$$\boldsymbol{i}_d(t) = \boldsymbol{i}_c(t) + \boldsymbol{I}_o \tag{25}$$

$$\langle i_d(t)\rangle = \frac{1}{T}\int_0^{T_s} \boldsymbol{i}_d(t).dt \tag{27}$$

$$\frac{V_{in}D_1(1-D)T_s}{2L} - \frac{V}{R} = 0 \tag{28}$$

$$\frac{V_o}{R(1-D)} \le \frac{DV_{in}T_s}{2L} \tag{29}$$

Eqn.(17) is substituted in the eqn. (29). Then,

$$R\left[\frac{nDV_{in}}{D'^2} + \frac{V_c + V_{sc} + V_d}{nD'}\right] \le \frac{DT_sV_{in}}{2L} \tag{30}$$

$$\frac{2L}{RT_s} \le \left[\frac{D'^2}{n} + \frac{DD'V_{in}}{V_c + V_{sc} + V_d}\right] \tag{31}$$

Here $V_{in} \approx V_c \approx V_{sc} \approx 3V_d$

Then the eqn.(29) can be rearranged as

$$\frac{2L}{RT_s} \le \left[\frac{nDD'}{2nD + 5D'}\right]$$

$$\frac{2L}{RT_s} = K \tag{32}$$

Dimensionless conduction parameter

$$K_{critical} = \left[\frac{nDD'}{2nD + 5D'}\right] \tag{33}$$

Fig11. shows the DCM and CCM boundary with n=2 at rated full load and the rated input of the photovoltaic isolated dc-dc converter.

When

$$K < K_{critical} \tag{34}$$

The converter falls discontinues conduction mode (DCM). The proposed converter is operated mainly in DCM covers more area as shown Fig11, hence this converter in the DCM at operating full load duty cycle at 70%. It has some salient features like low turn ON loss, soft recovery and low circuit inductance and when

$$K > K_{critical} \tag{35}$$

## 5. DC-DC Converter design considerations

The main equations to design the proposed dc-dc converter are presented.

*Switch Duty-Cycle*

The nominal duty-cycle is defined by (36)

*Switch stress*

The maximum voltage in the single power switch is equal to the

$$V_{stress} = \frac{V_{in}}{1-D} \tag{37}$$

Practically measured stress on the power switch = 130V as shown in the Fig15.

*Switch loss*

The RMS current can be determined approximately by eqn.(38), where the current ripple in the input inductance is not considered. The energy transference form of the capacitance does not change significantly the switch current waveform.

$$I_{switch(rms)} = \frac{P_i}{V_{in}} \times \sqrt{D} \tag{38}$$

The switch conduction loss is calculated by eqn. (40),

The switch turn off loss is reduced in the proposed converter because the turn-on occurs with ZVS. The power loss of the turn-off switching is equal to the area of the switch voltage ($V_{stress}$) and switch current ($I_{switch}$). The transitions at the switching instant are multiplied by the switching frequency. Considering the single switch current equal to 20A at the switching instant and turn-off time ($t_{off}$) equal to 50 ns, the turn-off power loss is calculated by

$$P_{sw(off)} = \left(\frac{1}{2} \times V_{stress} \times I_{switch} \times t_{off}\right) f \tag{39}$$

$$P_{sw(cond)} = I^2_{switch(rms)} \times R_{DSon} \tag{40}$$

*Diodes Conduction loss*

It is assumed that the average current in all diodes is equal to the output current in the proposed structure. The conduction losses of all diodes given are below by considering a conduction-threshold voltage equal to $V_{TD}$=1.2V. Maximum two diodes are active at a time.

$$P_{diode} = 2 \times \frac{P_o}{V_o} \times V_{TD} \tag{41}$$

*Transformer loss*

For high operating frequency suggests that a ferrite

amorphous core be used. A double-E core is chosen for the core shape. From the performance factor curves for ferrite materials at 100 kHz is optimal the ETD44 switched mode transformer used.

$$P_{others} = f_s A_c l_m \int H.dB \tag{42}$$

Where $A_c l_m$ is the column of the core.

*Calculated efficiency*

Calculated efficiency of the expected proposed converter efficiency can be determined by eqn.(24) based on the losses calculated given in eqn.(39) to eqn.(42).

*Voltage stress on output diode*

The voltage stress on output diode can be calculated as eqn.(43) and this practically measured value equal to 130V. $V_{in} \approx 3V_d$

$$V_d = \frac{V_i}{1-D} = \frac{V_o}{n+1} \tag{43}$$

*Voltage stress on clamp diode*

The clamp diode voltage stress is given by

$$V_c = \frac{n \times V_o}{n+1} \tag{44}$$

*Switched capacitor value*

The switched capacitor value approximated by the eqn.(45) the practical value used is 40 µF.

$$C_{sc} = \frac{P_o}{V_o \times \Delta V \times f_s} \tag{45}$$

*Output capacitor value*

Output Capacitor value can be find by the following eqn.(46) and the value used is 330 µF.

$$C_o = \frac{(1-D)V_o}{R \times \Delta V \times f_s} \tag{46}$$

*Leakage Inductance*

Leakage inductance can be designed by following equation

$$\frac{V_{in} + [V_o - V_{sc} - V_c]/n}{i_{Lk}} = L_k \tag{47}$$

Leakage inductance the current increasing rate of the switch is controlled during the switch is turn on with ZVS condition. The leakage inductance of the practical isolated transformer is 0.231µH.

## 6. Results

*Simulation results*

The proposed high boost dc-dc converter is simulated using PSIM software and output voltage and output gain are described before implementing. The switching frequency, input voltage 100kHz, $40V_{dc}$ are respectively used for simulation. Step-up output voltage obtains $403V_{dc}$. The voltage gain ($V_{GN}$) is equal to 10. This is matched with the theoretical value given in eqn.(15) & eqn.(17). Full load rating 500Watts is used in the simulation. At rated input current, the gate pulse (S), output voltage ($V_o$), output current ($I_o$) are shown in the Fig12. The output currents of power diodes $D_o$, $D_r$, and $D_c$ are shown in Fig13 during the switching operation. The Fig14 shows the clamp capacitor wave during the series resonance with transformer inductance and diode forward current as operation given during mode-V. The output voltage is lifted up to 403V. Hence, it is realized with the theoretical output voltage ($V_o$) given in the eqn.(15) & eqn.(17). Table-I provides the simulated parameters and their specifications.

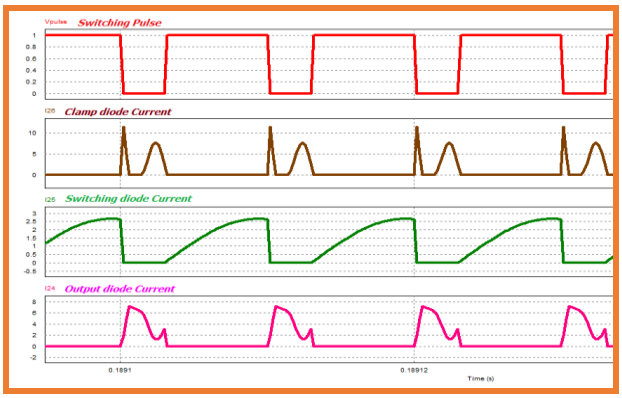


Fig.13 Diode currents during switching operations

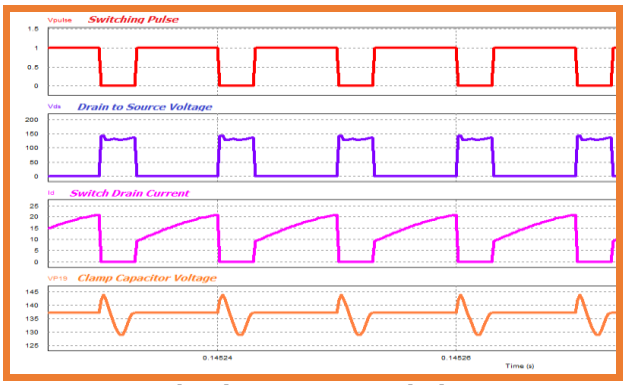


Fig.14. Switch voltage, Current and Clamp capacitor voltage

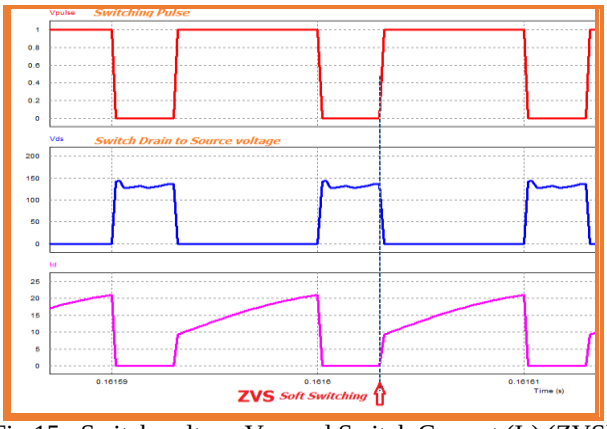


Fig.15. Switch voltage $V_{CE}$ and Switch Current ($I_e$) (ZVS)

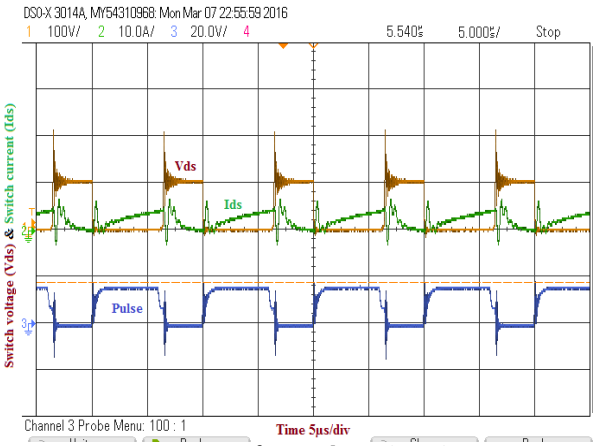


Fig.16. Soft switching (ZVS)

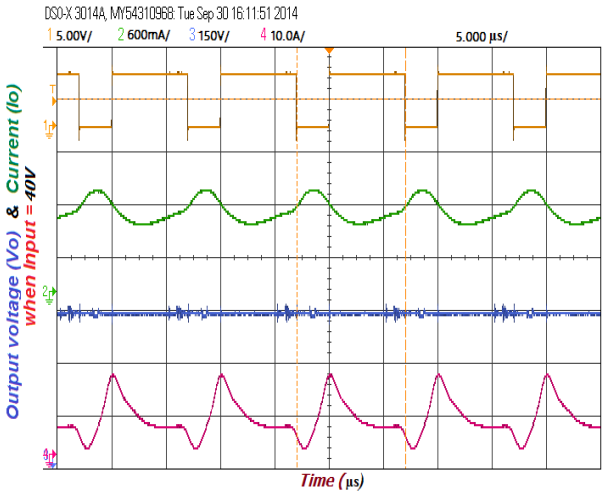


Fig.17. Measured Output Current and Voltage when input = 40V at Full Load (D=70%)

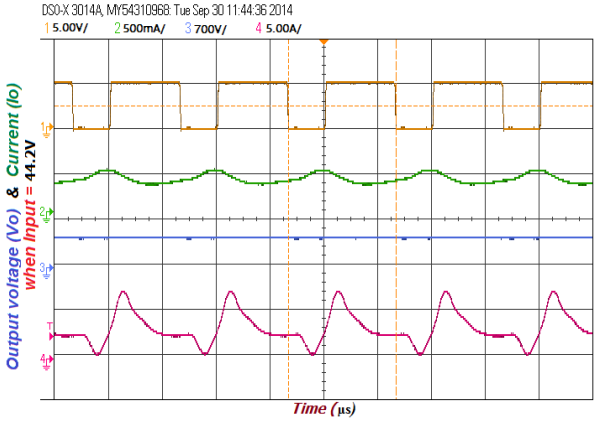


Fig.18. Waveforms of the proposed converter at rated input voltage =42.1V at Half Load (D=68%)

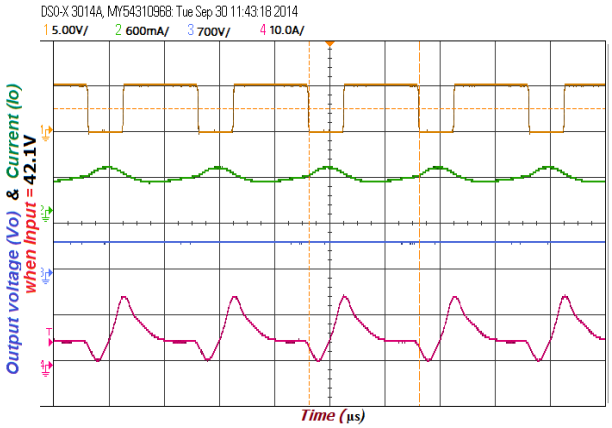


Fig.19. Waveforms of the proposed converter at rated input voltage 44.2V at No Load (D=65%)

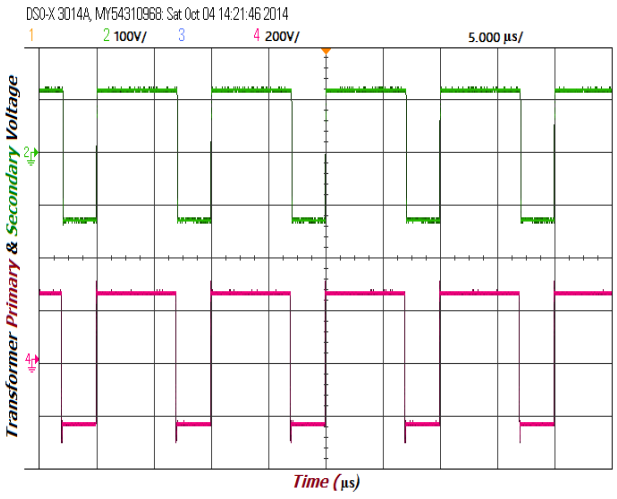


Fig.20. Switching Transformer primary and secondary Voltages

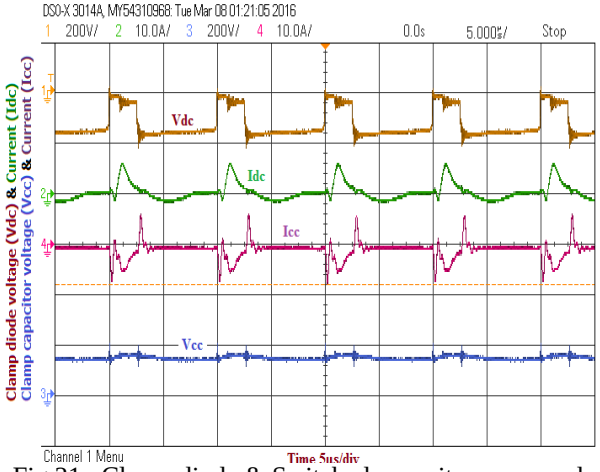


Fig.21. Clamp diode & Switched capacitor measured current

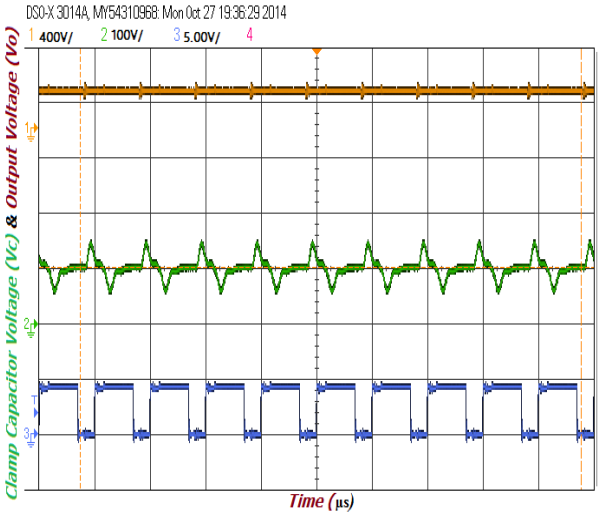


Fig.22. Clamp capacitor voltage & Output voltage

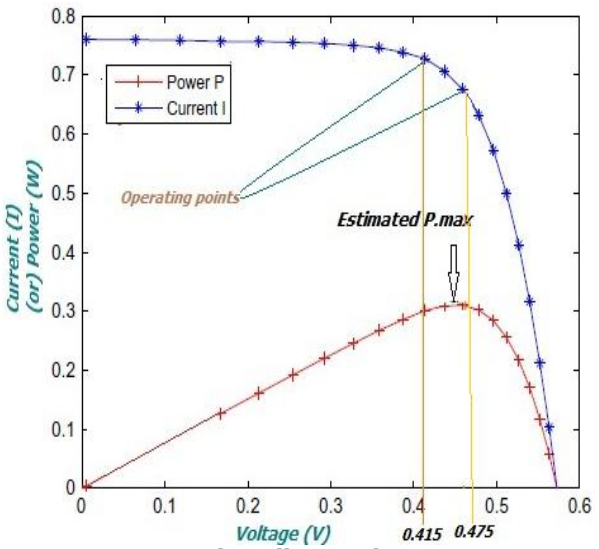


Fig.23. Solar cell I-V and P-V curve

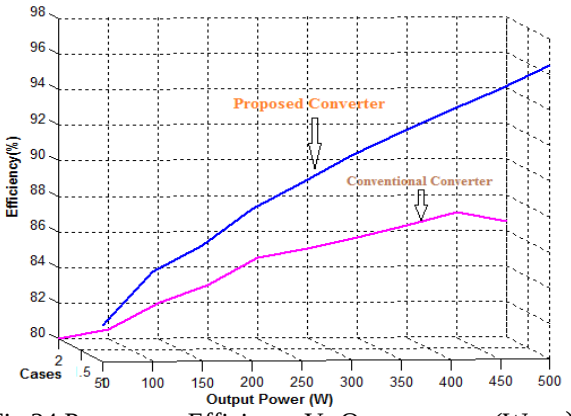


Fig.24 Percentage Efficiency Vs Output power (Watts)

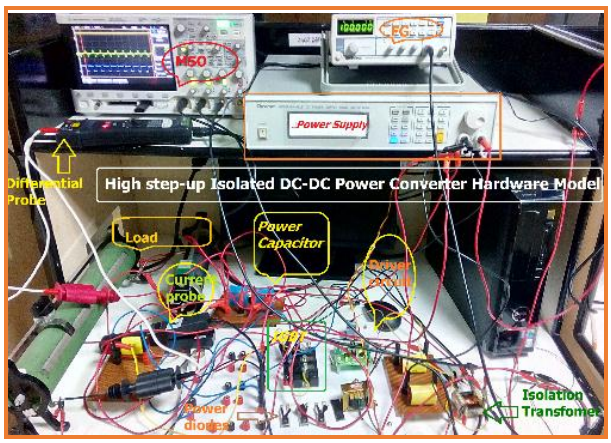


Fig.25 Hard ware model: Proposed isolated DC-DC Converter

*Soft Switching*

In Fig15 shows the voltage between collector to emitter of the IGBT power switch and current through the switch reaches zero before the gate pulse (S) is applied to controlled switch. Then the voltage starts increasing through the switch. This ensures ZVS of the switch. ZVS does not affect the switching loss that arises from the power switch output capacitance and it may not influence the loss induced by diode reverse recovery, hence ZVS is of no help in improving of converter efficiency. The practically measured switch stress ($V_{CE}$) and current ($I_e$) is shown in Fig16. This ensures ZVS of the switch which is depicted in the arrow point in the Fig16. The measured maximum switch voltage is equal 130V. The main switch voltage is clamped to that of the clamp capacitor by the clamp diode, when the switch is turned off at series resonance with isolated transformer inductance. The resonance frequency is greater than the switching frequency. From the waveforms in the Fig16, it can be seen that ZVS turn on condition is achieved for the active switch, which reduces the switching losses.

*Experimental Results*

A 500W prototype of the proposed converter is built to verify the theory. The hardware prototype model is shown in Fig25. The hardware prototype is validated with simulated design. The proposed model is

500Watts with 40Volts at 100kHz switching operation. The measured full load output voltage 400$V_{dc}$ and full load current 1.25A are shown in Fig17. The experimental results of the isolated transformer primary and secondary winding measured voltage are shown in Fig20.

Table 2
Experimental values

| *S.No.* | *Parameters* | *Specification* |
|---|---|---|
| 1 | DC voltage input | 40V |
| 2 | DC voltage output | 400V |
| 3 | Output power (max) | 500 W |
| 4 | Switching Frequency | 100 kHz |
| 5 | Output current | 1.26 A |
| 6 | Output Current ripple | 0.4mA |

The measured clamp diode ($D_c$) and the switched diode ($D_s$) current with switching pulse are illustrated in Fig21. Switched capacitor voltage shown in the Fig22 the measured $V_{rms}$ is 140V. The input to the prototype model is given 40$V_{dc}$ from the available DC power supply source. (Chroma -62012P-80-60) and the controlled single switch is controlled through various controllers like DSP (TMS320F28335) and dSPACE (DS1104) controller. Hence, the proposed converter is used only single pulse signal it also can be controlled by pulse generator.

The fixed DC source validated to renewable source by considering single solar cell measurement. As per the parameter given in the reference [20] the I-V and P-V curves are plotted as shown in the Fig23. For study 57mm diameter silicon solar cell under 1 Sun (1000 W/$m^2$) at 33˚C the voltage and current are measured. From this available experimental data, MPP is roughly estimated.

The solar cell open circuit, short circuit and maximum power point data are $V_{oc}$=0.5727V, $I_{sc}$=0.7605A, $I_{mp}$=0.6755A and $V_{mp}$=0.4590V. MPP is pointed between two steady operating points. These operating points the voltages are 0.415V and 0.475V. These values are per solar cell. For the practical case from the 40V DC source the load operating points are validated with different input voltages. These voltages are based on percentage variation in the single solar cell. The calculated variable voltage ranges are 42.1 40V, and 44.2V at full load, half load and no load respectively. The output waveform is observed by using Mixed Signal Oscilloscope and measured. The measured input and output voltage waveforms in Fig17 to Fig19 are shown at various operating voltages with different load condition. Fig17, Fig18 and Fig19 are output voltage and output current measurements for the different input DC voltages at 40V, 42.1V and 44.2V respectively. The switching pulse duty cycle (D) ranges vary accordingly from 70% to 65% during full load to no load. The experimental results show that the output voltage can be boosted upto the voltage gain 10 when it turns ratio (n) equal to 1:2. Thus, the proposed boost converter is capable to interface to the inverter grid at the user end. The experimental results are tabulated in Table-2.

The efficiency of the hardware model system is calculated at 4 different loads. By using the measured output power, the efficiency of the proposed dc-dc converter curve plotted with conventional converter efficiency are shown in Fig 24. The theoretical efficiency equation is given in eqn.(24). The practical calculated efficiency of the proposed model at full load is 95%.

## 7. Conclusion

This isolated high boost converter with switched capacitor and magnetizing inductor are used to get the high voltage gain. The transformer isolation can be accomplished and it provides better significant influence on efficiency of whole energy condition PV system. An application of fast recovery diodes eliminates the reverse recovery problems. Thus it allows quick diode turn-off without significant power losses. The leakage inductor of the clamp circuit and the series resonance achieve ZVS condition. High boost voltage operation can reduce stress on active switch. The active clamp circuit helps to recover the leakage energy of the diode and clamped capacitor to get high efficiency at high power value. All these features improve the circuit efficiency effectively. Complete analysis of the operations and the performances of the proposed converter are presented in this paper. A prototype of the converter was built and tested for validation of operation and performance of the proposed converter. Hence, the application of this high step-up dc-dc converter in the PV system can improve along with the power system value chain.

**References**


1. Gopi, A., Saravanakumar, R.; *High step-up isolated efficient single switch DC-DC converter for renewable energy source.* Ain Shams Engineering Journal, Article in press, Vol.5, p.1115–1127, (2014)
2. Thilo Grau, Molin Huo, Karsten Neuhoff, ; *Survey of photovoltaic industry and policy in Germany and China*. Energy Policy, Vol.51, p 20-37, (2012)
3. L. El Chaar, L.A. lamont, N. El Zein,; *Review of photovoltaic technologies.* Renewable and Sustainable Energy Reviews, Vol.15, No.5, p.2165-2175, ( 2011)
4. T.M. Razykov, C.S. Ferekides, D. Morel, E. Stefanakos, H.S. Ullal, H.M. Upadhyaya,; *Solar photovoltaic electricity: Current status and future prospects.* Solar Energy, Vol.85, No.8, p.1580-1608, (2011)
5. York, B.; Wensong Yu; Jih-Sheng Lai,; *An Integrated Boost Resonant Converter for Photovoltaic Applications*. Power Electronics, IEEE Transactions on , Vol.28, No.3, p.1199,1207, (2013)
6. Evran, F. Aydemir, M.T.; *Isolated High Step-Up DC–DC Converter With Low Voltage Stress.*

Power Electronics, IEEE Transactions on, Vol.29, No.7, p.3591,3603, (2014)
7. Kwon. J.M., Kwon, B.H.; *High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems.* IEEE Trans. Power Electron., Vol.24. No.1, p.108–115 (2009)
8. Tseng, K.C., Liang, T.J; *Novel high efficiency step-up converter*. IEE Proc Inst. Elect. Eng. Electr. Power Appl., Vol.151. No.2, p.182–190 (2004)
9. Tseng, K.C., Liang,T.J.; *Analysis of intergrated boost-flyback step-up converter*. IEE Proc. Inst. Elect. Eng. Electr. Power Appl., Vol.152. No.2, p.217–2222 (2005)
10. Wai, R.J., Liu, L.W. Duan, R.Y.; *High-efficiency voltage-clamped DC–DC converter with reduced reverse-recovery current and switch voltage stress*. IEEE Trans. Ind. Electron., Vol.53. No.1, p.272–280 (2005)
11. Zhao, Q., Lee, F.C.; *High-efficiency, high step-up dc–dc converters*. IEEE Trans. Power Electron., Vol.18. No.1, p. 65–73 (2003)
12. Zhao, Y., Li, W. Deng, Y., He, X.; *High step-up boost converter with passive lossless clamp circuit for non-isolated high step-up applications.* Power Electronics, IET, Vol.4. No.8, p.851-859 (2011)
13. Abutbul, O., Gherlitz, A., Berkovich, Y., Ioinovici, A., *Step-up switching-mode converter with high voltage gain using a switched capacitor circuit*. IEEE Trans. Circuits Syst. I, Vol.50. No.8, p.1098–1102 (2003)
14. Woo-Young Choi, Change-Goo Lee; *Photovoltaic panel integrated power conditioning system using a high efficiency step-up DC–DC converter*. Renewable Energy, Vol.41, p. 227–234 (2012)
15. Watson, R., Lee, F.C., Hua, G.C.; *Utilization of an active-clamp circuit to achieve soft switching in flyback converters.* IEEE Trans. Power Electron., Vol.11, No.1, p.162–169 (1996)
16. Sang Hee Kang, Maksimovic, D., Cohen, I., *Efficiency Optimization in Digitally Controlled Flyback DC–DC Converters Over Wide Ranges of Operating Conditions*. Power Electronics, IEEE Transactions, Vol.27, No.8, p.3734-3748 (2012)
17. Yihua Hu, Wenping Cao, Finney, S.J., Weidong Xiao, Fengge Zhang, McLoone, S.F.; *New Modular Structure DC–DC Converter Without Electrolytic Capacitors for Renewable Energy Applications*. Sustainable Energy, IEEE Transactions on , Vol.5, No.4, p.1184,1192,(2014)
18. Ki-Bum Park, Chong-Eun Kim, Gun-Woo Moon, Myung-JoongYoun; *PWM Resonant Single-Switch Isolated Converter*. Power Electronics, IEEE Transactions, Vol.24 No.8, p.1876-1886 (2009)
19. Tomaszuk, A., Krupa, A.; *High efficiency high step-up DC/DC converters - A review*. Bulletin of the Polish Academy of Sciences: Technical Sciences, Vol.59, No.4, p.475-483 (2011)
20. Dawidziuk, J.; *Review and comparison of high efficiency high power boost DC/DC converters for photovoltaic applications*. Bulletin of the Polish Academy of Sciences: Technical Sciences, Vol.59, No.4, p.499-506 (2011)
21. Nayak, D. K., Reddy, S.R; *Comparison of the synchronous-rectified push-pull converter with LLC DC to DC converter*. Arabian Journal for Science and Engineering, Vol.38, No.4, p.913-926 (2013)
22. Antonino Laudani., Francesco Riganti Fulginei., Alessandro Salvini.; *High performing extraction procedure for the one-diode model of a photovoltaic panel from experimental I–V curves by using reduced forms*. Solar Energy, Vol.103, p.316–326 (2014)