ACHIEVEMENT OF CASCADED MULTIRATE FIR FILTER STRUCTURES WITH CSE AND CSD

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Abstract: *Decimation and interpolation play vital role in multirate signal processing for sampling rate conversion(SRC). Area optimization is also very important to meet efficient filter structures in multirate signal processing systems. This paper proposes an area efficient multirate FIR filter structure for sampling rate conversion(SRC) from Digital Audio Tape (DAT) to Compact Disc (CD) by cascading three stages of linear phase multirate FIR filters with different sampling rates. The filter structures are implemented using two different approaches, namely, coefficient symmetry and polyphase approach. Area reduction in these structures is achieved by using Common Subexpression Elimination(CSE) technique with CSD (Canonic Signed Digit) and binary representations of filter coefficients. The proposed designs are implemented using MATLAB Simulink model and the Verilog code is generated using HDL coder. The performance of proposed structures is achieved using the Altera Quartus tool and the results are compared with conventional polyphase and coefficient symmetry approaches in terms of area and delay.*

Key words: Coefficient symmetry, CSE and CSD, Multirate FIR filter, Polyphase approach, Sampling rate conversion.

1. Introduction

Multirate digital signal processing play an increasingly important role in modern digital telecommunications theory in which digital transmission systems are required to handle data at several rates[1]. Modern high performance digital signal processing (DSP) systems exploit the benefits of Multirate systems in widespread applications, such as, frequency multiplexing and demultiplexing, digital audio tape, subband coding, conversion from CD to DAT and vice versa [2]. Systems that use different sampling rates at different stages are known as the multirate systems. The multirate techniques are used to convert the given sampling rate to the desired sampling rate, and to provide different sampling rates through the system without destroying the signal components of interest. The upsampler and downsampler are the basic building blocks in sampling rate conversion [3][4][5]. The multirate system consists of adder, multiplier, delay, upsampler and downsampler to obtain the sampling rate conversion shown in Fig.1. A discrete time input signal is upsampled by a factor of L in upsampler or interpolator and the output *p(n)* is passed into a filter with transfer function H(z). This output *q(n)* is downsampled by a factor of M in decimator giving the desired output *y(n)*.

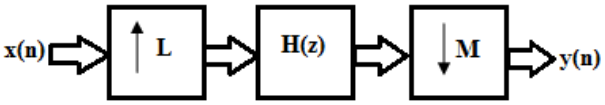

Fig.1. Block diagram of Multirate system

The time domain representation of an upsampling and downsampling is given in equation (1) and (2).

$$y(n)=\begin{cases} x\left(\frac{n}{L}\right) & \text{for } n=0,\pm L,\pm 2L,\pm 3L,\cdots \\ 0 & \text{elsewhere} \end{cases} \quad (1)$$

$$y(n)=\begin{cases} x(nM) & \text{for } n=0,\pm M,\pm 2M,\pm 3M,\cdots \\ 0 & \text{elsewhere} \end{cases} \quad (2)$$

2. Related Work

A lot of work is being done in the field of a Multirate signal processing system that employs different sampling rates. The filter design using contention resolution algorithm for weight-two subexpressions (CRA-2) has been developed for the common subexpression elimination. This approach provides significant reduction in number logic operators[7]. Area efficient hardware implementation of polynomial systems are achieved by applying algebraic techniques to enhance common subexpression elimination[8]. The cascaded integrator-comb (CIC) interpolation filter is included within a digital to analog converter and includes two upsamplers to have reduction in area and power requirements [9]. The method of determining filter coefficients for each filter stage from an associated group of sample points out of the first plurality of sample points is discussed in [10].Interpolator is used to increase the dot density of the digital oscilloscope [11].Efficient polyphase decimation filter design includes an odd/even sample delay line to allow faster

clocking of the FIR filter[12]. Low power and high speed digital filter having reduced number of adders using vertical CSD code words is discussed in [13]. In a digital transceiver, to narrow down a received wideband to a desired channel and to achieve desired sampling rate, interpolation and decimation methods are used[14]. A multirate filter as well as a display system and a mobile phone comprising a multirate filter. Digital filters find widespread use in audio and video processing which includes mobile phones, set top boxes, digital television sets. A discrete time signal resampling circuit is discussed in [15]. Full duplex operation and echo cancellation are utilized for both voice and date to implement multirate wire line modem apparatus. This wire line modem apparatus operable at either of two rates which are transmission or reception modes[16]. The method of Performing 8-point IDCT with common factors are discussed in [17].Area optimization is one of the most important technique in digital circuits design and implementation of DSP computations. Several area optimization techniques have been analyzed in literatures, including multiple constant multiplication (MCM), common subexpression elimination(CSE), canonic signed digit (CSD) representation of filter coefficients. In finite impulse response filter designs with fixed coefficients, constant multiplications are performed with a set of add and shift operations and the optimization is obtained with the help of common subexpression techniques[18]. Low complexity digital filter implementation can also be performed with minimum number of full adders and improved speed as discussed in [19]. High speed finite impulse response (FIR) filters are designed using non recursive signed common subexpression elimination algorithm[20]. The implementation complexity is minimized with coefficient symmetry.[21][22][23].The methods proposed in [24] and [25] eliminate redundant computations in multiplier blocks by employing the most common horizontal subexpressions among the CSD coefficients. As in [26], the transposed direct form CSD filter structures with minimum number of adders can be realized by efficiently combining horizontal and vertical common subexpressions that exist in the filter coefficients. Hence the area efficient structures are obtained by optimizing the filter coefficients of multirate filters. To have a further area reduction, the common subexpression elimination technique applies to the CSD representation of filter coefficients. Arithmetic Complexity reduction is discussed in Farrow filter[27].

In this work, multirate FIR filter structures are implemented using coefficient symmetry and polyphase approach with area reduction by adopting the CSE technique applied to the CSD representation of filter coefficients. The results are analyzed in terms of area and delay constraints. This rest of the paper is organized as follows, Section 2, discusses the survey of existing multirate filter structure implementations and its area optimizations. and in section 3, the problem formulation of the work is defined. In section 4, polyphase filter structures are discussed. Section 5 proposes cascaded Multirate linear phase FIR filter structures with CSE and CSD and its synthesis results are discussed in section 6. Finally, section 7 concludes the work.

3. Problem Formulation

The problem to be solved is described as a flow chart as in Fig.2.For filter coefficients are modified in terms of centosymmetric matrix elements and CSE and CSD is applied to represent multipliers in terms of shift and add operations

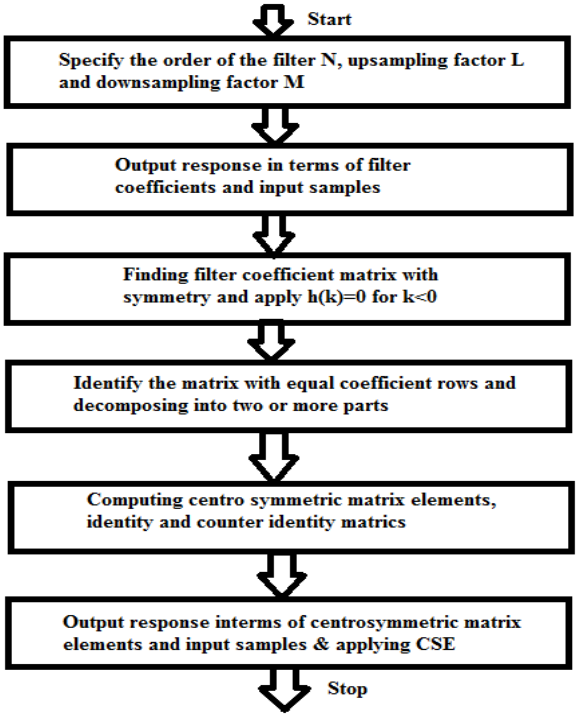

Fig.2. Flow Diagram

The problem to be solved is discussed in this section. This work proposes cascaded multirate filter structures to perform sampling rate conversion(SRC) from DAT to CD. The cascaded structure is achieved using three stages. Each of the structures are implemented using coefficient symmetry with CSE and CSD and they are connected together to get DAT to CD conversion. To perform DAT to CD conversion,the SRC factor 147/160 is needed. Here the upsampling factor (L) 147 is decomposed into three parts 7*7*3 and the downsamplig factor(M) 160 is divided into three components 5*8*4. So the three structures used here are 7/5 SRC,7/8 SRC and 3/4 SRC.Fig.2 shows the general flow diagram of the proposed work.The order for all the three structures are considered here is 33.The sampling rate conversion by a factor of(L/M) with filter order N is discussed here. $y_{n,L}$ is represented as shown below

$$y_{n,L} = H_{L,(p+q+1)}\ x_{m+p,m-q}$$

where $y_{n,L}$ is a vector of L consecutive output samples, and is represented by

$$y_{n,L} = \begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \\ y(n+3) \\ y(n+4) \\ . \\ . \\ y(n+L-1) \end{bmatrix}, x_{m+p,m-q} = \begin{bmatrix} x(m+p) \\ x(m+p-1) \\ x(m+p-2) \\ x(m+p-3) \\ x(m+p-4) \\ . \\ . \\ x(m-q) \end{bmatrix}$$

where *m*, *n* ,*p* and *q* are integers and are given by

$$m = \frac{M}{L}n, \quad n = 0, L, 2L, 3L, 4L, \ldots$$

$$p = \left\lfloor \frac{(L-1)M}{L} \right\rfloor, q = \left\lfloor \frac{N}{L} \right\rfloor$$

$H_{L,p+q+1}$ is a matrix containing the filter coefficients with L rows and $p+q+1$ columns[21].The input signal vector *x* consists of $p+q+1$ signal samples that are arranged in descending order. L and M are interpolation factor decimation factor.

Symmetry property is needed for the filters because the memory requirement for storing coefficients becomes half of the size needed when compared with anti symmetrical filter. The filter coefficients that satisfies the condition $h(k) = 0 \ for \ k < 0; k > N$ are used for applying coefficient symmetry. After applying coefficient symmetry, the rows in the H matrix having equal coefficients are identified and that is decomposed into two or more parts based on L,M and N. The decomposed matrix is then represented in terms of centro symmetric matrix elements c and d in order to reduce the computational complexity. This c and d also varies with L,M and N. For further improvement in the performance is achieved by applying CSE (Common sub expression Elimination) and CSD(Canonic Signed Digit)Technique. In CSE, binary representation is exploited for all the coefficients. Also the coefficients which shares the same inputs are arranged and the patterns are identified. So this approach effectively replaces the multipliers in terms of adders and shifters which further reduces the computational complexity. Similarly, the CSD is a unique representation which is represented by using an iterative procedure given below.

$$u_{-1} = 0, \ w_{-1} = 0$$

$$u_n = u_{n-1}$$

$$for (i = 0 \ to \ n-1)$$

{

$$v_i = u_i \oplus u_{i-1},$$

$$w_i = \overline{w_{i-1}}.\theta_i,$$

$$b_i = (1 - 2u_{i+1}).w_i$$

}

where u_n is the binary representation of a coefficient and b_i is the CSD representation of the coefficients.

The following terms to be used throughout this paper:(1)Coefficient Symmetry: The filter coefficients are selected in such a way that , the symmetry property is satisfied. The matrix representation of output is decomposed in terms of centro symmetric matrix elements which reduces the multiplication complexity considerably. (2)Polyphase: The FIR transfer function is decomposed into M lower-order transfer functions, called the polyphase components, which are afterwards added together to compose the original overall transfer function.(3)CSE: Sub-expression elimination is a numerical transformation of the constant multiplications that can lead to efficient hardware in terms of area, power and speed. Sub-expression can only be performed on constant multiplications that operate on a common variable. It is essentially the process of examining the shift and add implementations of the constant multiplications and finding redundant operations.The number of bit-wise matches (nonzero bits) between all of the constants in the set are determined. By choosing the best match, redundancy is eliminated[6]. (4) CSD: Using a canonic signed digit (CSD) representation, coefficients can be represented using the fewest number of non-zero bits[6]. A number is said to be in CSD representation if no two nonzero digits are consecutive and the number of nonzero digits is minimal, where each bit is in the set (0 ,+1,-1) and the -1 is often denoted by 1.

4. Polyphase FIR Filter

In Polyphase filter, the overall transfer function is decomposed into several sub functions to have efficient realization. In this section, polyphase filter with sampling rate conversion (SRC) by a factor of 7/5, 7/8 SRC and 3/4 SRC have been discussed. In specific, the hamming coefficients of a polyphase filters are represented in terms of binary and canonic signed digit format (CSD). Also the polyphase structure with common subexpression technique has been addressed.

4.1 Polyphase filter with 7/5 SRC

For the filter design, the order is taken as 33.The ouput response *y(n)* of a polyphase filter with upsampling factor 7 and downsampling factor 5 is given in equation (3). The symmetry of the coefficients are exploited for the design of a polyphase filter and is given in equation (4).

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \\ y(n+3) \\ y(n+4) \\ y(n+5) \\ y(n+6) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & h_0 & h_7 & h_{14} & h_{21} & h_{28} \\ 0 & 0 & 0 & 0 & h_5 & h_{12} & h_{19} & h_{26} & h_{33} \\ 0 & 0 & 0 & h_3 & h_{10} & h_{17} & h_{24} & h_{31} & 0 \\ 0 & 0 & h_1 & h_8 & h_{15} & h_{22} & h_{29} & 0 & 0 \\ 0 & 0 & h_6 & h_{13} & h_{20} & h_{27} & 0 & 0 & 0 \\ 0 & h_4 & h_{11} & h_{18} & h_{25} & h_{32} & 0 & 0 & 0 \\ h_2 & h_9 & h_{16} & h_{23} & h_{30} & 0 & 0 & 0 & 0 \end{bmatrix} x_{m+4,m-4} \quad (3)$$

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \\ y(n+3) \\ y(n+4) \\ y(n+5) \\ y(n+6) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & h_0 & h_7 & h_{14} & h_{12} & h_5 \\ 0 & 0 & 0 & 0 & h_5 & h_{12} & h_{14} & h_7 & h_0 \\ 0 & 0 & 0 & h_3 & h_{10} & h_{16} & h_9 & h_2 & 0 \\ 0 & 0 & h_1 & h_8 & h_{15} & h_{11} & h_4 & 0 & 0 \\ 0 & 0 & h_6 & h_{13} & h_{13} & h_6 & 0 & 0 & 0 \\ 0 & h_4 & h_{11} & h_{15} & h_8 & h_1 & 0 & 0 & 0 \\ h_2 & h_9 & h_{16} & h_{10} & h_3 & 0 & 0 & 0 & 0 \end{bmatrix} x_{m+4,m-4} \quad (4)$$

The number of filter coefficients(h_k) of the polyphase filter are seventeen. These seventeen filter coefficients are represents in terms of binary with common subexpression elimination and CSD with common subexpression elimination.

4.2 Polyphase filter with 7/8 SRC

In this section, polyphase filter with upsampling factor 7 and downsampling factor 8 is considered. In addition, the filter coefficients are represented in terms of binary CSE and CSD with CSE. The output response of a symmetric polyphase filter with order 33 is given in equation (5).

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \\ y(n+3) \\ y(n+4) \\ y(n+5) \\ y(n+6) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & h_0 & h_7 & h_{14} & h_{12} & h_5 \\ 0 & 0 & 0 & 0 & 0 & h_1 & h_8 & h_{15} & h_{11} & h_4 & 0 \\ 0 & 0 & 0 & 0 & h_2 & h_9 & h_{16} & h_{10} & h_3 & 0 & 0 \\ 0 & 0 & 0 & h_3 & h_{10} & h_{16} & h_9 & h_2 & 0 & 0 & 0 \\ 0 & 0 & h_4 & h_{11} & h_{15} & h_8 & h_1 & 0 & 0 & 0 & 0 \\ 0 & h_5 & h_{12} & h_{14} & h_7 & h_0 & 0 & 0 & 0 & 0 & 0 \\ h_6 & h_{13} & h_{13} & h_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} x_{m+6,m-4} \quad (5)$$

4.3 Polyphase filter with 3/4 SRC

In this section, polyphase filter with upsampling factor 3 and downsampling factor 4 is considered. In addition, the filter coefficients are represented in terms of binary CSE and CSD with CSE. The output response of a symmetric polyphase filter with order 33 is given in equation (6).

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_0 & h_3 & h_6 & h_9 & h_{12} & h_{15} & h_{15} & h_{12} & h_9 & h_6 & h_3 & h_0 \\ 0 & h_1 & h_4 & h_7 & h_{10} & h_{13} & h_{16} & h_{14} & h_{11} & h_8 & h_5 & h_2 & 0 & 0 \\ h_2 & h_5 & h_8 & h_{11} & h_{14} & h_{16} & h_{13} & h_{10} & h_7 & h_4 & h_1 & 0 & 0 & 0 \end{bmatrix} x_{m+2,m-11} \quad (6)$$

5. Multirate FIR Filter With Coefficient Symmetry

Multirate FIR filter is implemented using adder, multiplier and delay elements. Here the multiplier is the filter coefficients. The filter coefficients are represented in terms of BCSE and CSD CSE. This section deals with the multirate filters which performs sampling rate conversion from DAT to CD. The conversion is done using three stages which are 7/5 SRC, 7/8 SRC and 3/4 SRC. There are four types of linear phase FIR filter. A linear-phase FIR filter of order N is either characterized by a symmetric impulse response as given in (7), or by an asymmetric impulse response of a FIR filter as given in (8). In this work, the type -II linear phase FIR filter is preferred.

$$h(n) = h(N-1-n) \quad (7)$$

$$h(n) = -h(N-1-n) \quad (8)$$

5.1 Coefficient Symmetry

Coefficient symmetry is the technique which helps to reduce the implementation complexity[21][22][23]. For a filter having an order N, the first N/2 coefficients will be the same as the remaining coefficients for even values of N and the coefficient (N+1)/2 will be a loner in the middle of the coefficient array. If N is odd, the first (N+1)/2 coefficients will be the same as the remaining coefficients. The coefficient symmetry technique greatly reduces the multiplication complexity as only (N+1)/2 different filter coefficients are present. Hence the multiplication complexity can be reduced upto half of its original requirement. In this section, the coefficient symmetry approach is applied for all the three multirate filters 7/5 SRC, 7/8 SRC and 3/4 SRC. The filter coefficients are represented in terms of centro symmetric matrix elements. Then for each of the coefficients BCSE and CSD-CSE is applied to have optimum results in terms of area and delay.

5.2 7/5 SRC with Coefficient Symmetry

The sampling rate conversion by a factor of 7/5 with filter order 33 is discussed in this section. The upsampling factor is seven and the downsampling factor is five. Since the upsampling factor is seven, the number of consecutive output samples are also seven. The matrix representation of seven consecutive output samples is given in equation (9).

$$y_{n,7} = H_{7X9} \cdot x_{m+4,m-4} \quad (9)$$

for n = 0, 7, 14, 21, 28, ...and m = 0, 5, 10, 15, 20, ... To realize the efficient structure, the output response expression in matrix form is decomposed into two subparts and each of the subparts are represented using the centrosymmetric matrix elements c and d. The centosymmetric matrix elements c and d are the variables and they depends only on the filter coefficients[21].The filter coefficients are predetermined. The I and J are identity and counter identity matrices. The computed output response in matrix form is given in equation (10).

$$\begin{bmatrix} y(n) \\ y(n+1) \end{bmatrix} = h_{14} x_{m-2} \begin{bmatrix} 1 \\ 1 \end{bmatrix} + \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} c_{00} & c_{01} & 0 & 0 \\ 0 & 0 & d_{01} & d_{00} \end{bmatrix} \begin{bmatrix} I_2 & J_2 \\ J_2 & -I_2 \end{bmatrix} \begin{bmatrix} x_{m,m-1} \\ x_{m-3,m-4} \end{bmatrix}$$

$$\begin{bmatrix} y(n+2) \\ y(n+3) \\ y(n+4) \\ y(n+5) \\ y(n+6) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} c_{10} & c_{11} & c_{12} & c_{13} & 0 & 0 & 0 & 0 \\ 0 & c_{21} & c_{22} & c_{23} & 0 & 0 & 0 & 0 \\ 0 & 0 & h_6 & h_{13} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & d_{23} & d_{22} & d_{21} & 0 \\ 0 & 0 & 0 & 0 & d_{13} & d_{12} & d_{11} & d_{10} \end{bmatrix} \begin{bmatrix} I_4 & J_4 \\ J_4 & -I_4 \end{bmatrix} x_{m+4,m-3} \quad (10)$$

where the centrosymmetric matrix elements to implement the integer sampling rate conversion 7/5 is

given below.

$$c_{00}=\frac{h_0+h_5}{2},\ c_{01}=\frac{h_7+h_{12}}{2},\ d_{00}=\frac{h_0-h_5}{2},\ d_{01}=\frac{h_7-h_{12}}{2}$$

$$c_{10}=\frac{h_2}{2},\ c_{11}=\frac{h_9}{2},\ c_{12}=\frac{h_{16}}{2},\ c_{13}=\frac{h_3+h_{10}}{2}$$

$$d_{10}=\frac{-h_2}{2},\ d_{11}=\frac{-h_9}{2},\ d_{12}=\frac{-h_{16}}{2},\ d_{13}=\frac{h_3-h_{10}}{2}$$

$$c_{21}=\frac{h_4}{2},\ c_{22}=\frac{h_1+h_{11}}{2},\ c_{23}=\frac{h_8+h_{15}}{2}$$

$$d_{21}=\frac{-h_4}{2},\ d_{22}=\frac{h_1-h_{11}}{2},\ d_{23}=\frac{h_8-h_{15}}{2}$$

The complete structure for 7/5 sampling rate conversion of order 33 is shown in Fig.3.

5.2.1 Binary representation with CSE

The filter coefficients are obtained from hamming window. The binary representation is exploited for all the filter coefficients. Also the coefficients which shares the same inputs are arranged and the patterns are identified. For example, the value of centrosymmetric matrix elements c_{11} is 0.0100 1101 0111 1101 and c_{21} is 0.0001 1010 0111 1110 .Here for both coefficients 5^{th},10^{th},11^{th},12^{th},13^{th} and 14^{th} bits are nonzero (ones). So these bits shares the shifters which minimizes considerable amount of shifters. The two coefficients c_{11} and c_{21} are multiplied with the signal which is the delayed and downsampled version of the input signal. The resultant two outputs are given as the input for the delay and upsampler block .Similarly all the constants or coefficients are represented in terms of shift and add operation instead of multiplication. So the number of multipliers have been reduced to zero but at the expense of shifters and adders. Similarly the value of centrosymmetric matrix elements c_{12} and c_{22} are 0.0111 1111 1011 1110 and 0.0110 1101 1110 0000. These coefficients are represented in terms of adders and shifters and is given in Fig.4 and Fig.5.

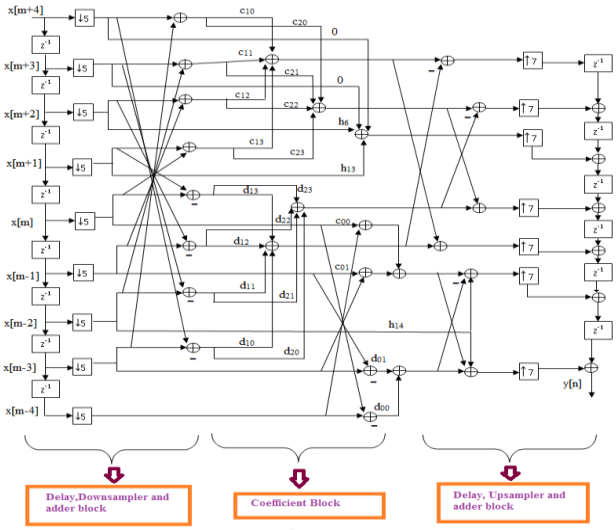

Fig.3. SRC by a Factor 7/5 with N=33

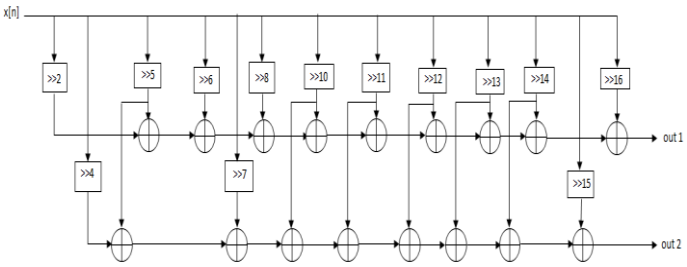

Fig.4. Representation of c_{11} and c_{21}

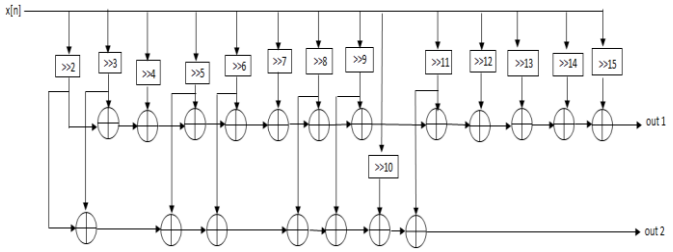

Fig.5. Representation of c_{12} and c_{22}

The 7/5 SRC structure without CSE shown in figure 3 , the coefficients are modified in terms of centrosymmetric matrix elements which gives a considerable reduction in multiplication complexity when compared to the polyphase 7/5 SRC structure without CSE. In 7/5 SRC without CSE,the required number of multiplication and addition complexity to produce seven output samples is 24.997 and 36.96. So the multiplication and addition complexity to produce one output sample is 3.571 and 5.28 . Whereas in binary with CSE requires zero multiplication but at the expense of adders and shifters.

5.2.2. CSD with CSE

In this section, the filter coefficients are represented in canonic signed digit format. The patterns are identified between the centro symmetric matrix elements which shares the same input sequence to have efficient design. Because finding the pattern reduces considerable number of shifts. The coefficients and their CSD form[6] is given below and if there is a pattern exists , this is indicated with the bold letter of 1's. The CSD value of the coefficient c_{21} is 0.0010 1010 1000 0001 and c_{11} is 0.0101 0010 1000 0010. These two coefficients is multiplied with the same signal and is given in Fig.6.Similarly the value of c_{22} and c_{12} are 0.1001 0010 0010 0000 , 0.1000 0000 0100 0010 respectively which are given in Fig.7 7.

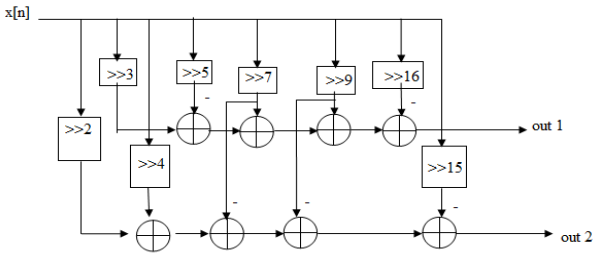

Fig.6. CSD Representation of c_{21} and c_{11}

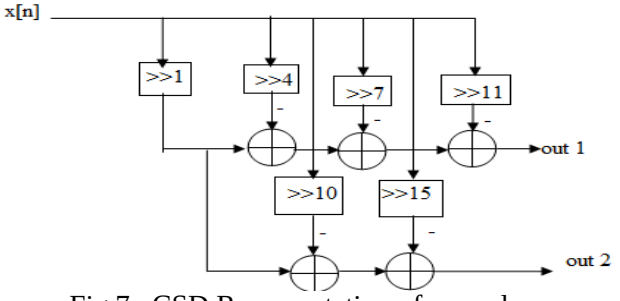

Fig.7. CSD Representation of c_{22} and c_{12}

The binary and CSD representations of the above mentioned filter coefficients are listed in Table I. In binary representation, consecutive ones are possible, whereas CSD representation does not have consecutive ones. CSD representation is a unique representation[6].

Table 1

Filter Coefficient Representation

Coeff	Binary Representation	CSD Representation
c_{11}	0.0100 1101 0111 1101	0.0101 00$\underline{1}$0 $\underline{1}$000 00$\underline{1}$0
c_{21}	0.0001 1010 0111 1110	0.00$\underline{1}$0 $\underline{1}$010 1000 000$\underline{1}$
c_{12}	0.0111 1111 1011 1110	0.1000 0000 0$\underline{1}$00 00$\underline{1}$0
c_{22}	0.0110 1101 1110 0000	0.$\underline{1}$00$\underline{1}$ 00$\underline{1}$0 00$\underline{1}$0 0000

5.3 7/8 SRC with Coefficient Symmetry

In this section, the sampling rate conversion by a factor of 7/8 with filter order 33 is explained. The seven consecutive output samples can be expressed as a function of input samples and is given in the matrix equation (11)

$$y_{n,7} = H_{7\times11} \cdot x_{m+6,m-4} \qquad (11)$$

For n = 0, 7, 14, 21, 28, ... and m= 0, 8, 16, 24, 32,..... For the six consecutive output samples , 5x5 identity and counter identity matrix [21][22] is used. The computed matrix is given in equation (12).

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \\ y(n+3) \\ y(n+4) \\ y(n+5) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} c_{00} & c_{01} & c_{02} & c_{03} & c_{04} & 0 & 0 & 0 & 0 & 0 \\ 0 & c_{11} & c_{12} & c_{13} & c_{14} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & c_{22} & c_{23} & c_{24} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{24} & d_{23} & d_{22} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{14} & d_{13} & d_{12} & d_{11} & 0 \\ 0 & 0 & 0 & 0 & 0 & d_{04} & d_{03} & d_{02} & d_{01} & d_{00} \end{bmatrix} \begin{bmatrix} I_5 & J_5 \\ J_5 & -I_5 \end{bmatrix} x_{m+5,m-4}$$

$$[y(n+6)] = [h_6 \quad h_{13} \quad h_{13} \quad h_6]\, x_{m+6,m+3} \qquad (12)$$

The calculated twenty four centrosymmetric matrix elements c and d are given below

$$c_{00} = \frac{h_5}{2},\ c_{01} = \frac{h_{12}}{2},\ c_{02} = \frac{h_{14}}{2},\ c_{03} = \frac{h_7}{2},\ c_{04} = \frac{h_0}{2}$$

$$d_{00} = \frac{-h_5}{2},\ d_{01} = \frac{-h_{12}}{2},\ d_{02} = \frac{-h_{14}}{2},\ d_{03} = \frac{-h_7}{2},\ d_{04} = \frac{-h_0}{2}$$

$$c_{11} = \frac{h_4}{2},\ c_{12} = \frac{h_{11}}{2},\ c_{13} = \frac{h_{15}}{2},\ c_{14} = \frac{h_1 + h_8}{2}$$

$$d_{11} = \frac{-h_4}{2},\ d_{12} = \frac{-h_{11}}{2},\ d_{13} = \frac{-h_{15}}{2},\ d_{14} = \frac{h_1 - h_8}{2}$$

$$c_{22} = \frac{h_3}{2},\ c_{23} = \frac{h_2 + h_{10}}{2},\ c_{24} = \frac{h_9 + h_{16}}{2}$$

$$d_{22} = \frac{-h_3}{2},\ d_{23} = \frac{h_2 - h_{10}}{2},\ d_{24} = \frac{h_9 - h_{16}}{2}$$

The implemented Linear phase FIR filter structure with 7/8 sampling rate conversion and order 33 is shown in Fig.8. The six consecutive output samples represented in terms of centro symmetric matrix elements. These matrix elements are given in terms of filter coefficients h_k. The seventh output sample is obtained by using the filter coefficients h_6 and h_{13}. The common subexpression elimination technique is applied in binary and CSD format[6] of filter coefficients. The patterns are identified and are represented in bold letters. This bold letter **1** indicates that the required shifting is taken from the previous coefficient value. This way of finding pattern, minimizes the number of shift operations required to implement a multirate filter structure. So the multipliers or the filter coefficients are identically replaced by shift and add operations to get area efficient structure.

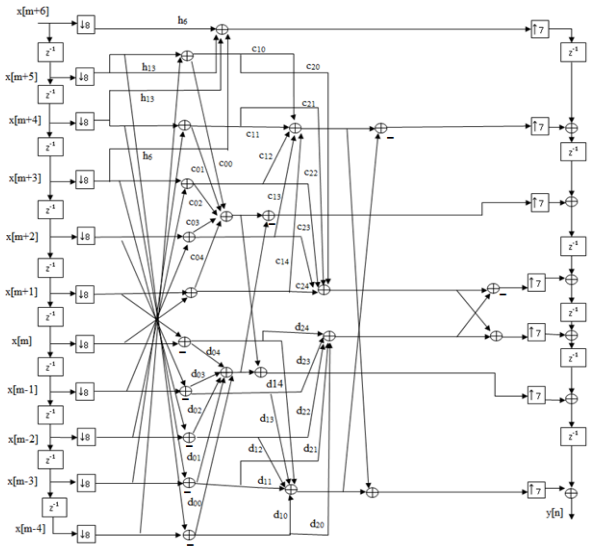

Fig.8. Sampling Rate Conversion by a Factor 7/8 with N=33

5.4 3/4 SRC with Coefficient Symmetry

The sampling rate conversion by a factor of 3/4 with filter order 33 is considered in this part. Here the sampling frequency is increased by a factor of 3 and decreased by a factor of 4. The three consecutive output samples are represented interms of input samples [21][22].

$$y_{n,3} = H_{3\times14} \cdot x_{m+2,m-11}$$

For n = 0, 3, 6, 9,... and m = 0, 4, 8, 12, 16,.... The computation is similar to that of integer sampling rate conversion 7/5 and 7/8. The first part is the computation of one output sample and the second part is the computation of remaining two output samples and is given in equation (13).

$$[y(n)] = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} c_{00} & c_{01} & c_{02} & c_{03} & c_{04} & c_{05} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & d_{05} & d_{04} & d_{03} & d_{02} & d_{01} & d_{00} \end{bmatrix} \begin{bmatrix} I_6 & J_6 \\ J_6 & -I_6 \end{bmatrix} x_{m,m-11}$$

$$\begin{bmatrix} y(n+1) \\ y(n+2) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} c_{10} & c_{11} & c_{12} & c_{13} & c_{14} & c_{15} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & d_{15} & d_{14} & d_{13} & d_{12} & d_{11} & d_{10} \end{bmatrix} \begin{bmatrix} I_6 & J_6 \\ J_6 & -I_6 \end{bmatrix} x_{m+2,m-9} \quad (13)$$

The calculated twenty four centrosymmetric matrix elements are listed below.

$$c_{00} = \frac{h_0}{2}, c_{01} = \frac{h_3}{2}, c_{02} = \frac{h_6}{2}, c_{03} = \frac{h_9}{2}, c_{04} = \frac{h_{12}}{2}, c_{05} = \frac{h_{15}}{2}$$

$$d_{00} = \frac{-h_0}{2}, d_{01} = \frac{-h_3}{2}, d_{02} = \frac{-h_6}{2}, d_{03} = \frac{-h_9}{2}, d_{04} = \frac{-h_{12}}{2}, d_{05} = \frac{-h_{15}}{2}$$

$$c_{10} = \frac{h_2}{2}, c_{11} = \frac{h_1 + h_5}{2}, c_{12} = \frac{h_4 + h_8}{2}, c_{13} = \frac{h_7 + h_{11}}{2}, c_{14} = \frac{h_{10} + h_{14}}{2}, c_{15} = \frac{h_{13} + h_{16}}{2}$$

$$d_{10} = \frac{-h_2}{2}, d_{11} = \frac{h_1 - h_5}{2}, d_{12} = \frac{h_4 - h_8}{2}, d_{13} = \frac{h_7 - h_{11}}{2}, d_{14} = \frac{h_{10} - h_{14}}{2}, d_{15} = \frac{h_{13} - h_{16}}{2}$$

The implemented filter structure with 3/4 sampling rate conversion and order 33 is shown in Fig.9.The output response of this multirate filter structure is represented in terms of twenty four centrosymmetric matrix elements. From the binary and CSD representation of the filter coefficients of 3/4 SRC structure, it is observed that the patterns are not obtained since the input to the filter coefficients are different.

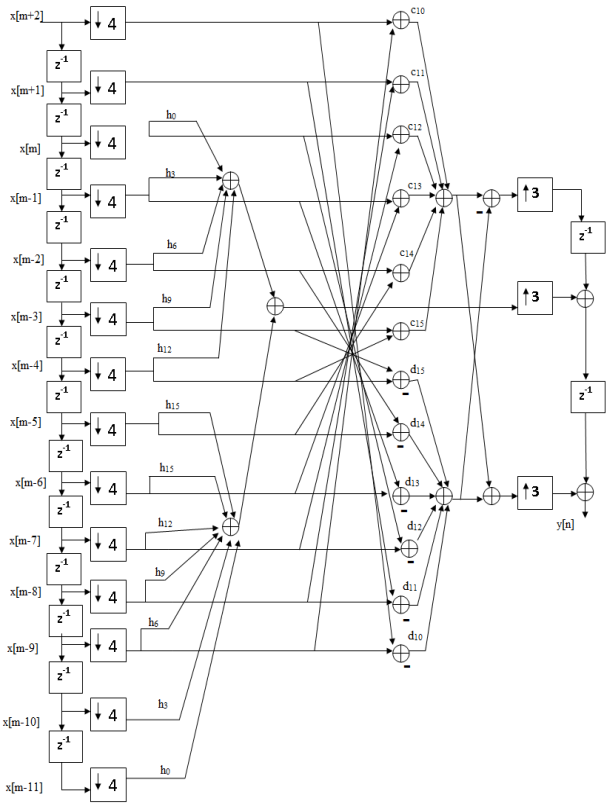

Fig.9. SRC by a Factor 3/4 with N=33

6.Simulation Results and Discussions

The Matlab version 2012a is used to create the simulink model for the individual multirate filter. In addition, the Simulink model for all the three stages of cascaded structure have also been developed and the Verilog codes are generated using HDL coder. These codes are verified using Modelsim Altera 6.5e. The area, power and delay are determined using Altera Quartus-II software and the compilation summary is given in Table II,III and IV . The synthesis results are analyzed with Cyclone II family FPGA device EP2C70F672C6. The Simulink model of 7/5 SRC with CSE in Binary representation is given in Fig.10.A coefficient used in this structure is given in Fig.11.

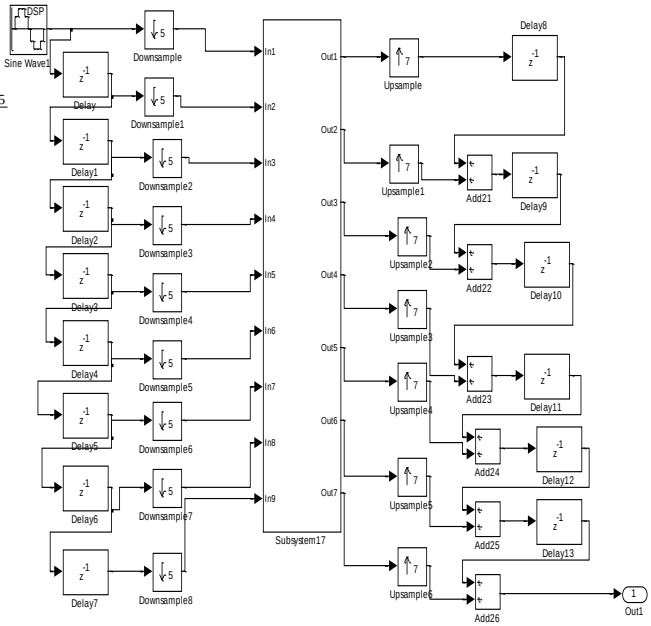

Fig.10. SRC by a Factor 7/5 with CSE in Binary

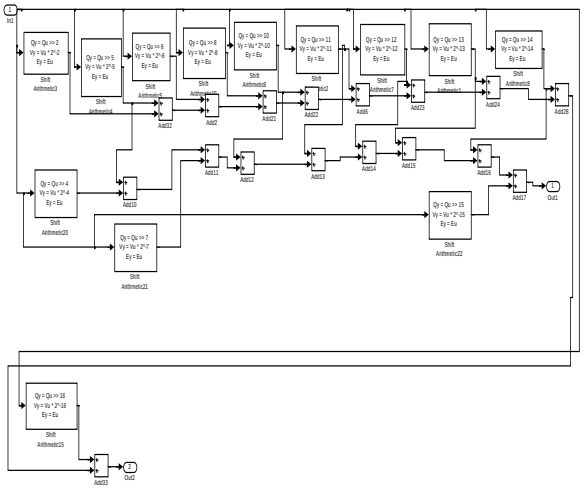

Fig.11 Coefficients used in 7/5 SRC with CSE in Binary

Table 2(a) shows the total number of adders and multipliers needed for the existing and the proposed CSE,CSD scheme.The number of one's needed to represent a binary number is higher than the CSD representation for both polyphase and coefficient symmetry approach. The 7/5 SRC structure having 34 filter coefficients h_0 to h_{33}.The filter coefficient h2 requires 8 adders, h9 and h4 requires 9 adders,h16,h11,h6,h1 shares the common input which requires 31 adders. Similarly the coefficients h10,h15,h13,h8,h3 requires 37 adders. Similarly the next set of coefficients which shares the common input requires 49,49,30,26 and 12 adders respectively.

So the total number of adders require for the binary with CSE in polyphase approach is 251 which is larger than CSD Representation. Since CSD is a unique representation, less number of bits are used for the filter coefficients in all the three structures. Comparing to the polyphase approach, coefficient symmetry approach requires less number of adders. Without CSE approach requires multipliers, whereas with CSE, the multipliers have been replaced in terms of adders and shifters. Table 2(b) shows the computational complexity per output sample of the cascaded stages. In the proposed scheme, each of the multipliers are replaced with adders and shifters. So the multiplication complexity is eliminated with increase in adders and shifters. In terms of number of complex multiplication, the proposed scheme is better when compared with polyphase and coefficient symmetry approach.

The arithmetic complexity in terms of number of complex multiplications are shown in Table 2(c).Multipliers are costly when compared to adders. So, in the proposed scheme the multipliers are modified interms of shifters and adders. Compared to the approaches specified in coefficient symmetry [21] and Farrow based [27], the proposed scheme has less complexity. For the Farrow based approach, the number of subfilters are considered to be 3 and the length and order of each filters taken as 12 and 11 respectively..The complexity of Farrow approach is closer to polyphase approach but it varies based on the number of subfilters.

Table 3 shows the synthesis summary of polyphase filter in which the area(logic elements) and delay has been analyzed. Three SRC structures (7/5, 7/8 and 3/4) are implemented using a polyphase filter. In addition, all the structures are implemented with and without CSE. Here CSE technique is applied in both binary and CSD representation of filter coefficients. The filter coefficients or the multipliers are equivalently represented by shift and add operations in order to reduce the area. For these structures, the binary representation of filter coefficients are having more number of one's than CSD representation. Hence the area in binary representation is minimized when compared to the without CSE structure but it is increased when compared to CSD representation. However, the individual stages of polyphase filter with CSE having lesser area (logic elements) when compared to the without CSE structure. Area has been greatly reduced by applying CSE technique in CSD representation. The delay has also been reduced in binary and CSD representation when compared to the without CSE structures.

Table 4 shows the compilation summary of each of the multirate filter using coefficient symmetry approach. The delay is reduced in both polyphase and coefficient symmetry approach by applying CSE technique in CSD format. The number of logic elements in the coefficient symmetry approach without CSE is greater than the Binary and CSD Representation. Since in binary and CSD, only the non zero bits are considered for the design which minimizes adders and multipliers. However the logic elements with CSE in individual stages using coefficient symmetry approach is larger than the individual stages of polyphase approach. This is because , in polyphase, the number of coefficients which shares the same delayed input is higher than that of coefficient symmetry approach. So, more number of common bit patterns are obtained which reduces the number of adders required for the implementation with polyphase approach. Since in coefficient symmetry approach with CSE, the number of centrosymmetric matrix elements which is common to the input is minimal thereby less number of patterns are obtained which involves more number of adders than polyphase with CSE. Also the number of logic elements in polyphase approach without CSE is larger than coefficient symmetry approach without CSE. Because in polyphase structure with 7/5 SRC, the number of multiplications and additions required to produce seven consecutive output samples are 34 and 27. So the multiplication and addition complexity per output sample is 4.8571 and 3.8571. In coefficient symmetry approach with 7/5 SRC, the coefficients modified in terms of centrosymmetric matrix elements show a considerable reduction in multiplication complexity. The number of multiplication and addition complexity to produce seven output samples is 24.997 and 36.96. So the multiplication and addition complexity to produce one output sample is 3.571 and 5.28, which shows that the multiplication complexity is reduced for the proposed filter structure when compared to the conventional polyphase filter structure with a slight increase in addition complexity. Similarly, the multiplication complexity of the second and third stage having the conversion factor of 7/8 and 3/4 SRC are lesser when compared to the polyphase structure without CSE. The results of cascaded stages using polyphase and coefficient symmetry approach is given in Table 5. Cascaded SRC using coefficient symmetry without CSE requires lesser logic elements when compared to the polyphase approach without CSE. Similarly the binary with cascaded coefficient symmetry requires

lesser logic elements when compared to the cascaded polyphase approach with binary. Since in binary , the number of ones are represented by the relevant shift and add operations and zeros does not requires shift and add operations which saves considerable amount of logic elements. Similarly cascaded coefficient symmetry with CSD requires lesser logic elements than cascaded polyphase with CSD.

The speed improvement of the proposed scheme over the polyphase and coefficient symmetry approach [Ref 21] is given in table 6. The speed improvement of the proposed scheme is significant when compared to the polyphase and coefficient symmetry approach.The speed (operating frequency) improvement in the proposed scheme over the polyphase and coefficient symmetry approach is justified in Table 6, by implementing the design on EP2C70F672C6 device using Altera ,Cyclone-II tool. From Table 6 it is clear the operating frequency of the proposed coefficient symmetry scheme with CSE is 24.53MHz and 23.58MHz and for the proposed polyphase scheme with CSE is 19.63MHz and 18.56MHz, whereas for the coefficient symmetry polyphase and scheme [21] it is 19.59MHz and 16.16MHz. This results in the speed improvement in the proposed coefficient symmetry scheme with CSE by 20.12% and 16.9% over existing scheme. Similarly the speed improvement in the proposed polyphase scheme with CSE is achieved about 17.64% and 12.93 % over without CSE scheme.

Based on the comparisons made with other earlier designs, such as polyphase and coefficient symmetry based [21] shown in Table 3 to Table 6, it can be justified that the proposed design provides frequency as well as area optimization.

Table 2(a)
Number of Adders and Multipliers

Add/Mul	SRC 7/5			SRC 7/8			SRC 3/4		
	Ref [21]	Proposed CSE (B)	Proposed CSE (CSD)	Ref [21]	Proposed CSE (B)	Proposed CSE (CSD)	Ref [21]	Proposed CSE (B)	Proposed CSE (CSD)
P_{Mul}	34	-	-	34	-	-	34	-	-
P_{Add}	27	251	166	27	243	162	31	237	154
C_{Mul}	24.9	-	-	31.9	-	-	18	-	-
C_{Add}	36.9	170	94	43	200	115	35	133	89

Table 2(b)
Computational Complexity per output sample of cascaded stages(N=33)

S.No	SRC	Ref[21]		Proposed CSE(B)		Proposed CSE (CSD)		Relative Comparison			
		Cm	Ca	Cm1	Ca1	Cm2	Ca2	Cm1/Cm	Ca1/Ca	Cm2/Cm	Ca2/Ca
1	Polyphase	21	18	-	150	-	98	-	8.333	-	5.444
2	Co.sym	14	23	-	97	-	59	-	4.217	-	2.535

Table 2(c)
Multiplication Complexity of cascaded stages

Parameter	Using Ref[27]	Using Ref[21]		Proposed			
	Farrow	Polyphase	Coefficient Symmetry	Coefficient symmetry with CSE (Binary)	Coefficient symmetry with CSE (CSD)	Polyphase with CSE (Binary)	Polyphase with CSE (CSD)
Number of complex multiplications	108	102	75	-	-	-	-

Table 3
Compilation Summary of Polyphase FIR Filter for Individual Stages

Device		Polyphase [SRC 7/5]			Polyphase [SRC 7/8]			Polyphase [SRC 3/4]		
		(using Ref [21])	Proposed With CSE(Binary)	Proposed With CSE(CSD)	(using Ref [21])	Proposed With CSE(Binary)	Proposed With CSE(CSD)	(using Ref [21])	Proposed With CSE(Binary)	Proposed With CSE(CSD)
Altera Cyclone-II EP2C70F672C6	Logic Elements	3620/ 68416	346/ 68416	295/ 68416	4223/ 68416	339/ 68416	290/ 68416	3961/ 68416	439/ 68416	331/ 68416
	Power (mW)	201.46	201.38	201.43	201.52	201.40	201.44	201.37	201.35	201.36
	t_{pd} (ns)	30.737	21.233	19.036	32.835	19.895	18.967	37.364	31.524	30.088

Table 4
Compilation Summary of Multirate FIR Filter Using Coefficient Symmetry for Individual Stages

Device		Coefficient Symmetry [SRC 7/5]			Coefficient Symmetry [SRC 7/8]			Coefficient Symmetry [SRC 3/4]		
		(using Ref [21])	Proposed With CSE (Binary)	Proposed With CSE (CSD)	(using Ref [21])	Proposed With CSE (Binary)	Proposed With CSE (CSD)	(using Ref [21])	Proposed With CSE (Binary)	Proposed With CSE (CSD)
Altera Cyclone-II EP2C70F672C6	Logic Elements	1769/ 68416	886/ 68416	784/ 68416	3488/ 68416	966/ 68416	723/ 68416	2875/ 68416	906/ 68416	868/ 68416
	t_{pd} (ns)	28.33	22.193	21.847	31.763	22.234	21.847	32.542	22.135	21.081

Table 5
Compilation Summary of Cascaded Stages

Device		Cascaded stages (Coefficient Symmetry)			Cascaded stages (Polyphase)		
		(using Ref [21])	Proposed With CSE (Binary)	Proposed With CSE (CSD)	(using Ref [21])	Proposed With CSE (Binary)	Proposed With CSE (CSD)
Altera Cyclone-II EP2C70F672C6	Logic Elements	31289/ 68416	32578/ 68416	25483/ 68416	51355/ 68416	37282/ 68416	29901/ 68416
	t_{pd} (ns)	51.040	40.769	42.412	61.866	50.955	53.866

Table 6
Speed Improvement of Cascaded Stages

Parameters	Using Ref[21]		Proposed		Proposed	
	Polyphase	Coefficient Symmetry	Coefficient symmetry with CSE (Binary)	Coefficient symmetry with CSE (CSD)	Polyphase with CSE (Binary)	Polyphase with CSE (CSD)
Delay (ns)	61.866	51.04	40.769	42.412	50.955	53.866
Freq. (MHz)	16.16	19.59	24.53	23.58	19.63	18.56
Speed Improvement (%)	-	-	20.12%	16.9%	17.64%	12.93%

The propagation delay of coefficient symmetry approach with CSE and polyphase approach with CSE are lesser when compared to the without CSE which increases the speed of operation. The logic element utilization for the individual SRC stages and cascaded stages are given in Fig.12 and Fig.13.

The cascaded SRC structures are simulated using MATLAB. The simulation results for DAT to CD conversion is given in Fig.14(a) and Fig.14(b). The number of samples in the input signal is 201, 281 in the 7/5 SRC, 246 samples in the 7/8 SRC and 184 samples in the 3 /4 SRC which provides the required conversion factor. Thus the multirate filter with coefficient symmetry is exploited for all the structures. The Fig.15(a)and Fig.15(b) shows the simulation waveforms achieved using MATLB. Here for the input signal with number of samples 101, the output of 7/5 SRC contains 141 samples. Likewise the output of 7/8 SRC and 3/4 SRC contains 88 and 76 samples respectively. The output of cascaded stage contains 92 samples.Here the application is validated and the programs and schemes are inserted in the webpage https://github.com/Mariammalkms/multirate-filters.

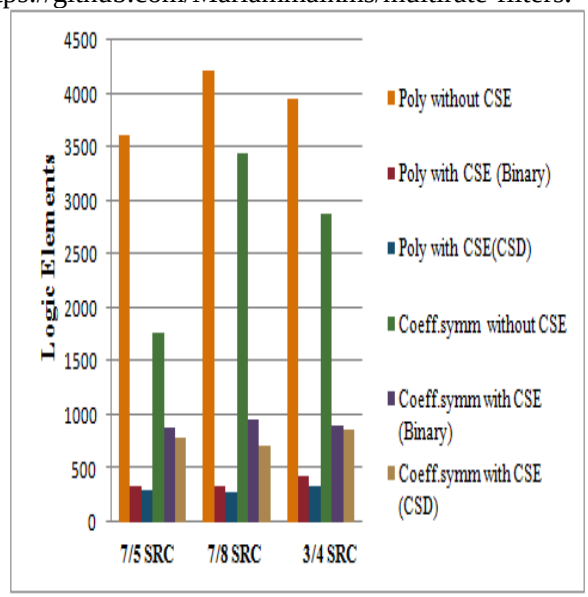

Fig.12. Logic Elements (Area) achievement for each stage

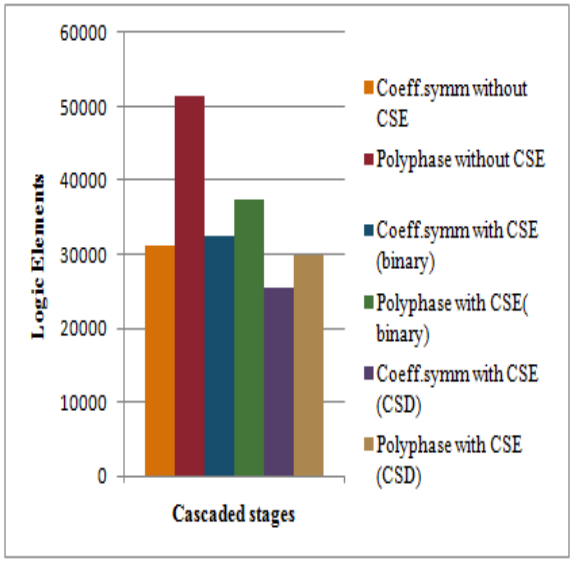

Fig.13. Logic Elements (Area) achievement for cascaded stages

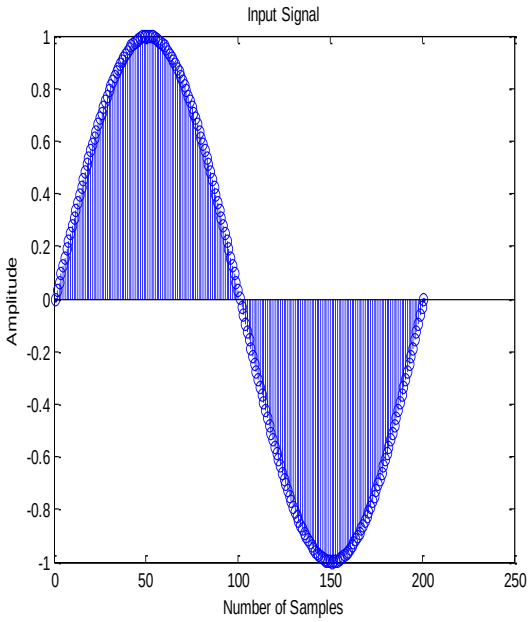

Fig.14(a) Input signal

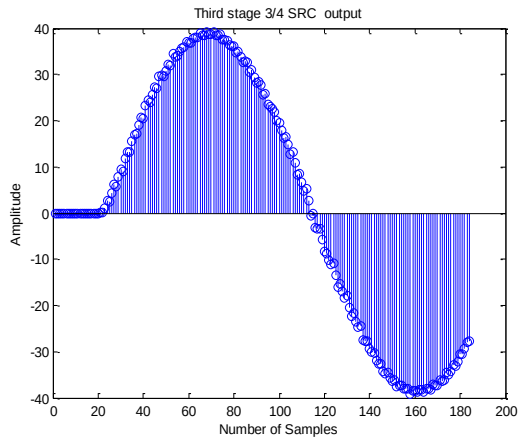

Fig.14(b) Output signal

Fig.15. Cascaded SRC (DAT to CD) with input having 201 number of samples

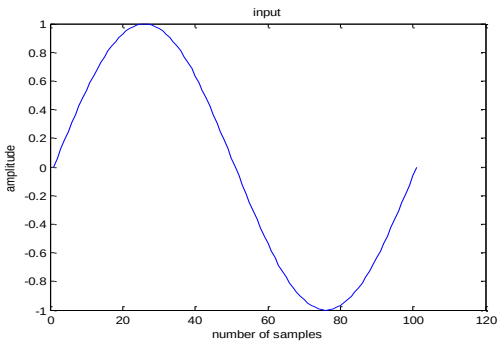

Fig.15(a) Input signal

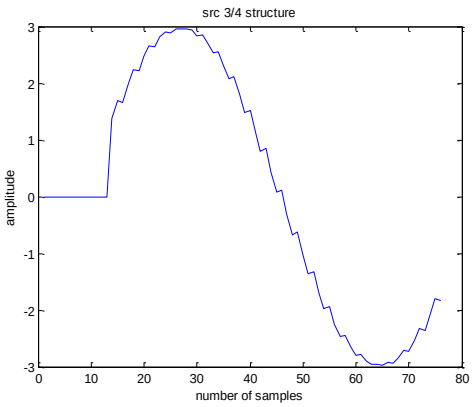

Fig.15(b) 3/4 SRC output

Fig.15. SRC with input having 101 number of samples

7. Conclusion

This paper proposes various Multirate Linear Phase FIR filter structures utilizing the coefficient symmetry and polyphase with CSE and CSD to perform DAT to CD conversion. The DAT to CD conversion is performed using cascaded approach and the DAT to CD conversion factor is 147/160. Here the up sampling and down sampling factors are decomposed into three stages, which are 7/5 SRC, 7/8 SRC and 3/4 SRC. The filter structures are implemented using coefficient symmetry approach and polyphase approaches. The multiplication complexity of the proposed achievement is significantly reduced when compared to the polyphase, coefficient symmetry and Farrow based SRC structures.To have speed improvement and area reduction CSE technique is applied in binary and CSD representation of filter coefficients and the results are reported. Simulink model have been developed to obtain HDL codes for the implemented structures. The resources utilized for the individual SRC stages and the cascaded stages are analyzed using the Altera, cyclone II family with EP2C70F672C6 device and the results are also compared in terms of area, delay and power dissipation. The results shows that the coefficient symmetry approach without CSE requires lesser logic elements and minimum delay when compared to the conventional polyphase approach without applying CSE. Also area is reduced for both approaches by applying CSE technique in CSD representation when compared to the filter structure without CSE technique.

References

[1] Robert J.Schilling, Sandra L.Harris , *Fundamentals of Digital Signal Processing using MATLAB* ,Thomson 2007 pp:331-516.

[2] Ljiljana Milic, *Multirate Filtering for Digital Signal Processing:MATLAB Applications*, Information Science Reference, 2009, pp:23-198.

[3] John G.Proakis, Dimitris G.Manolakis, *Digital signal processing principles algorithms and applications*, Fourth edition Prentice Hall of India, 2006, pp:650-700& 750-800.

[4] P.P.Vaidyanathan, *Multirate systems and filter bank*, ISBN 978-81-7758-942-9, Pearson Fifth Impression, 2011, pp:100-150.

[5] Ronald E.Crochiere Lawrence R.Rabiner, *Multirate Digital Signal Processing*, Prentice Hall, 1983,pp:13-88 & 127-180.

[6] Keshab.K. Parhi, *VLSI Digital Signal Processing Systems Design and Implementation*, John Wiley 2008 ,pp:559-583.

[7] Fei Xu, Chip-Hong Chang and Ching-Chuen Jong, *Contention Resolution Algorithm for Common Subexpression Elimination in Digital Filter Design*, IEEE Transaction on Circuits and Systems-II:Express Briefs, Vol.52 , No.10, October 2005, pp:695-700.

[8] Sivaram Gopalakrishnan and Priyank Kalla, *Algebraic Techniques to Enhance Common Sub-Expression Elimination for Polynomial System Synthesis*, EDAA 2009, pp:1452-1457.

[9] Michael R.May, Carlos A.Greaves ,*Cascaded Integrator-Comb Interpolation Filter*, United States Patent US005880687A,Mar.9, 1999, No.5880687.

[10] David S.McGrath, *Digital Multirate Filtering*, United States Patent US7321913 B2, Jan.22, 2008.

[11] Thomas P.Dagostino, Bruce ELMiller, Luis J.Navarro, *Display Interpolator Employing a Transversal Filter for a Digital Oscilloscope*, United States Patent 4263593, Apr.21,1981.

[12] Mohammad Shafiul Mobin, Marta Rambaud , *Efficient Polyphase Decimation Filter*, United States Patent US6532273 B1,Mar.11, 2003.

[13] Jang, Young-Beom, Yang, Se-Jung, *Low power CSD linear phase FIR filter architecture using vertical common subexpression and filter design method therefor*, European Patent Application EP 1 311 064 A2 ,May.14, 2003.

[14] Adnan Al-Adnani, *Multirate Digital Transceiver*, United States Patent US7616720B2 ,Nov.10, 2009.

[15] Bruekers, Alphons, Kalker, Antonius, *Multirate Filter and a Display System and a Mobile Telephone Comprising said Multirate Filter*, European Patent Specification EP 1 570 574 B1, May.30 ,2012.

[16] Peter Cummiskey, Marvin Epstein, Paul A.Gilmour, Richard Kim, *Multirate Wire Line Modem Apparatus*, United States Patent, 50005168, Apr.2,1991.

[17] Yuriy Reznik, *Transforms with Common Factors*, United States Patent US8595281B2,Nov.26 2013.

[18] R.Pasko, P.Schaumont, V.Derudder, S.Vernalde, D.Durackova, *A New Algorithm for Elimination of Common Subexpressions* ,IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.18 ,No.1, January 1999, pp:58-65.

[19] A.P.Vinod and Edmund M.-K.Lai, *An Efficient Coefficient-Partitioning Algorithm for Realizing Low-Complexity Digital Filters*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.24, No.12, December 2005,pp:1936-1946.

[20] Marcos Martinez-Peiro, Eduardo I.Boemo and Lars Wanhammar, *Design of High-Speed Multiplierless Filters using a Nonrecursive Signed Common Subexpression Algorithm*, IEEE Transactions on Circuits and Systems -II:Analog and Digital Signal Processing, Vol.49, No.3, March 2002, pp:196-203.

[21] Robert Bregovic, Ya Jun Yu, Tapio Saramki, Yong Ching Lim, *Implementation of Linear-Phase FIR Filters for a Rational Sampling-Rate Conversion Utilizing the Coefficient Symmetry* , IEEE Transactions on Circuits and Systems-I:Regular Papers, Vol.58, No.3, March 2011, pp:548-561.

[22] Zhi-Jian (Alex) Mou, *Symmetric Exploitation in Digital Interpolators/Decimators*, IEEE Transaction on Signal Processing, Vol.44, No.10,October 1996,pp:2611-2615.

[23] Robert Bregovic, Tapio Saramki, Ya Jun Yu, Yong Ching Lim, *An Efficient Implementation of Linear-Phase FIR Filters for a Rational Sampling Rate Conversion*, IEEE 2006, ISCAS 2006, pp:5395-5398.

[24] Hartley, R.I., *Subexpression sharing in filters using canonic signed digit multipliers*, IEEE Trans. Circuits Syst. IL Analog. Digit. Signal Process,1996 43 (lo), pp. 677-688.

[25] Yagyu, M**.,** Nishihara, A., and Fuji, N, *Fast FIR digital filter structures using minimal number of adders and its application to filter design*, ICICE Trans. Fundam. Electron. Commun. Comput. Sei.1996 E19-A (8), pp. 1120-1 129.

[26] A.P. Vinod, E.M-K. Lai, A.B. Premkumar and C.T. Lau, *FIR filter implementation by efficient sharing of horizontal and vertical common subexpressions*, Electronics Letters ,Vol.39, No.2, 23rd January 2003, pp:251-253.

[27] Amir Eghbali and Hakan Johansson, *Complexity Reduction in Low-Delay Farrow Structure Based Variable Fractional Delay FIR Filters Utilizing Linear Phase Subfilters*, IEEE 2011.pp.21-24.