

# Advanced Control Techniques for Three Phase Cascaded Multilevel Inverter

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**Abstract**— In this paper, various novel pulse width modulation techniques are proposed, which can minimize the total harmonic distortion and enhances the output voltages from five level inverter to multilevel topologies. Multilevel inverters are important for power electronics applications such as flexible ac transmission systems, renewable energy sources, uninterruptible power supplies and active power filters. Three methodologies adopting the constant switching frequency, variable switching frequency multicarrier, phase shifted carrier pulse width modulation concepts are proposed in this paper. The above methodologies divided in to two techniques. The subharmonic pulse width modulation cascaded multilevel inverter strategy, minimized total harmonic distortion and switching frequency optimal pulse width modulation cascaded multilevel inverters strategy, enhances the output voltages. Field programmable gate array has been chosen to implement the pulse width modulation due its fast proto typing, simple hardware and software design. Simulation and Experimental results are provided.

**Keywords**— Constant switching frequency, variable switching frequency, multicarrier pulse width modulation, phase shifted carrier pulse width modulation, subharmonic, switching frequency optimal, cascaded multilevel inverter

## I. INTRODUCTION

Recently, for increasing use in practice and fast developing of high power devices and related control techniques, multilevel inverters have become more attractive to researches and industrial companies. Multilevel inverters have achieved an increasing contribution in high performance applications. The different multilevel inverter structures are cascaded H-bridge, diode clamped and flying capacitors multilevel inverters [1]-[4]. Increasing the number of levels in the inverter without requiring high ratings on individual devices can increase the power rating [5]. In this paper, constant switching frequency, variable switching frequency multicarrier and phase shifted carrier pulse width modulation methods are used for proposed inverter control methods, since, they are all based on the carrier concept. The control objective is to compare reference with multicarrier and phase shifted carrier wave using three phase five level cascaded inverter. The multilevel inverter advantages are improved output voltage, reduced output total harmonic distortion, reduced voltage stress on semiconductor switches and decrease of EMI problems [6]-[10]. In this paper, three novel carrier pulse width modulation schemes are presented which take advantage of special properties available in multilevel

inverter to minimize total harmonic distortion and increases output voltage [11]-[15]. The total harmonic distortion value is high for multicarrier subharmonic pulse width modulation and multicarrier switched frequency optimal pulse width modulation and output voltage level is below actual value [16]. Illustrative examples are given to demonstrate the feasibility of the proposed methods.

## II. THREE PHASE CASCADED MULTILEVEL INVERTER

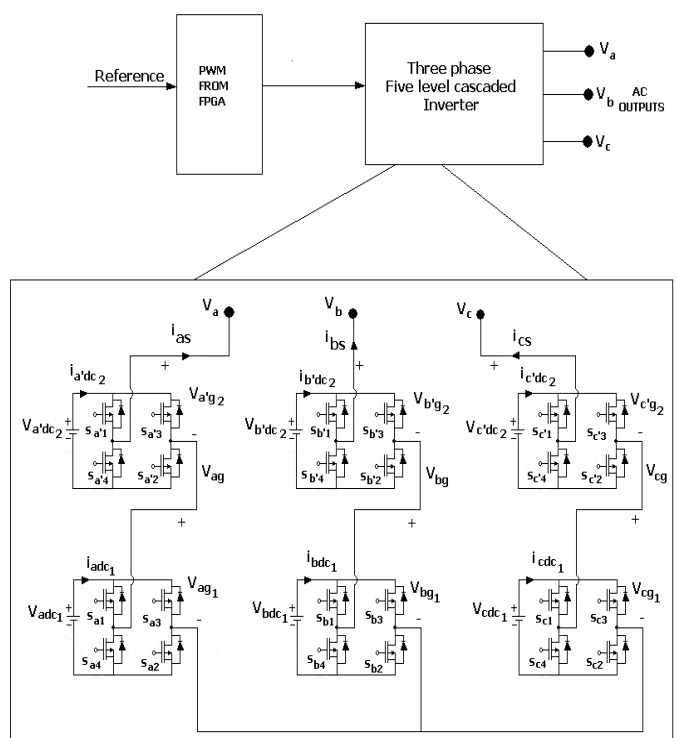


Fig. 1: FPGA based three phase cascaded five level inverter

A Field programmable gate array based three phase cascaded five level inverter is illustrated in fig.1. Each dc source is connected to an inverter. Each inverter level can generate three different voltage outputs,  $+V_{dc}$ ,  $0$ , and  $-V_{dc}$  using various combinations of the four switches. The ac outputs of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of

output phase voltage levels  $m$  in a cascaded inverter is defined by  $m=2s+1$ , where  $s$  is the number of separate dc sources.

### III. CONSTANT SWITCHING FREQUENCY MULTICARRIER PULSE WIDTH MODULATION

#### A. Constant switching frequency multicarrier subharmonic pulse width modulation (CSFMC-SH PWM)

Fig.2a shows an  $m$ -level inverter,  $m-1$  carriers with the same frequency  $f_c$  and the same amplitude  $A_c$  are disposed such that the bands they occupy are contiguous. The reference waveform has peak to peak amplitude  $A_m$ , the frequency  $f_m$ , and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than  $s$  carrier signal, then they active device corresponding to that carrier is switched off.

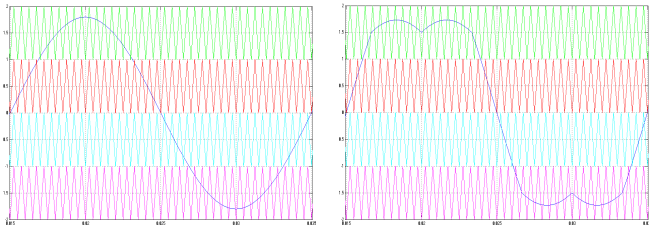


Fig 2: Constant switching frequency multicarrier pulse width modulation a) CSFMC-SH PWM and b) CSFMC-SFO PWM

In multilevel inverters, the amplitude modulation index  $M_a$  and the frequency ratio  $M_f$  are defined as

$$M_a = A_m / (m-1)A_c \quad (1)$$

$$M_f = f_c / f_m \quad (2)$$

#### B. Constant switching frequency multicarrier switching frequency optimal pulse width modulation(CSMC-SFO PWM)

Fig.2b shows the CSFMC-SFO PWM in which triplen harmonic voltage is added to each of the carrier waveforms. The method takes the instantaneous average of the maximum and minimum of the three reference voltages ( $V_a, V_b, V_c$ ) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms.

$$V_{\text{offset}} = \{ \max(V_a, V_b, V_c) + \min(V_a, V_b, V_c) \} / 2 \quad (3)$$

$$V_{a\text{SFO}} = V_a - V_{\text{offset}} \quad (4)$$

$$V_{b\text{SFO}} = V_b - V_{\text{offset}} \quad (5)$$

$$V_{c\text{SFO}} = V_c - V_{\text{offset}} \quad (6)$$

The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system,

however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

In this Paper to increase output voltage, MC-SFO PWM technique is used and by Third harmonic injection, the output voltage  $V_{ac}$  can be achieved to 10V with THD value 21.40%.

### IV. VARIABLE SWITCHING FREQUENCY MULTICARRIER SUBHARMONIC PULSE WIDTH MODULATION

#### A. Variable switching frequency multicarrier subharmonic pulse width Modulation (VSFMC-SH PWM)

For a multi level inverter, if the level are  $m$  there will be  $m-1$  carrier set with variable switching frequency multi carrier Pulse width modulation when compared with sinusoidal reference. The carriers are in phase across for all the bands. In this technique, significant harmonic energy is concentrated at the carrier frequency. But since it is a co-phasal component, it doesn't appear line to line voltage. In this paper, we proposed a five level inverter whose levels are  $0, \pm V/2$  and  $\pm V$ , its carrier set are assigned to have variable switching frequency of 2000 Hz and 4000Hz as shown in the fig.3a

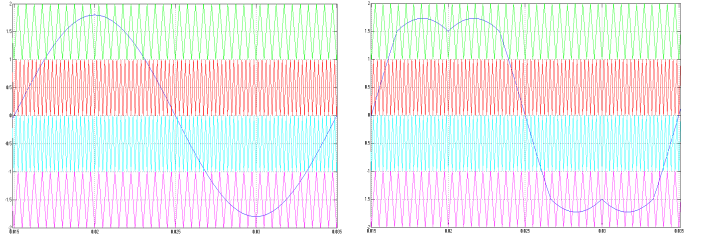


Fig 3: Variable switching frequency multicarrier subharmonic pulse width modulation a) VSFMC-SH PWM and b) VSFMC-SFO PWM

#### B. Variable switching frequency multicarrier switching frequency optimal pulse width modulation (VSFMC-SFO PWM)

For a multilevel inverter, if the level is  $m$  there will be  $m-1$  carrier set with variable switching frequency multi carrier Pulse width modulation when compared with third harmonic injection reference. For third harmonic injection given as

$$Y = 1.15 \sin\theta + 1.15 / 6 \sin 3\theta. \quad (7)$$

The resulting flat topped waveform allows over modulation while maintaining excellent AC term and DC term spectra. This is an alternative to improve the output voltage without entering the over modulation range. So any carriers employed for this reference will enhance the output voltage by 15% without increasing the harmonics.

In this paper, there are five level inverter is proposed whose levels are  $0, \pm V/2$  and  $\pm V$ , its carrier set are assigned to have variable switching frequency of 2000 Hz and 4000Hz as shown in the fig. 3b.

## V. PHASE SHIFTED CARRIER PULSE WIDTH MODULATION

### A. Phase shifted carrier subharmonic pulse width modulation (PSC-SH PWM)

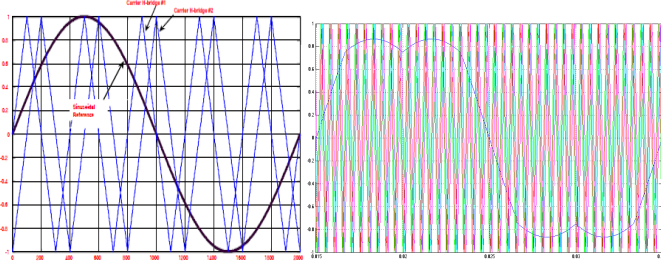


Fig.4: Phase shifted carrier pulse width modulation  
a) PSC-SH PWM and b) PSC-SFO PWM

Fig.4a shows the Phase shifted carrier subharmonic pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, which provides an even power distribution among the cells. A carrier phase shift of  $180^\circ/m$  for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

The modulating signal generator for the PSC PWM optimum harmonic cancellation is achieved in PSC PWM. Phase shifting for carrier is given by,

$$(K-1)\Pi/n \quad (8)$$

Where,  $k$  is the  $k$ th inverter.

$n$  is the number of series connected single phase inverter.

$$N = (L-1)/2 \quad (9)$$

Where,  $L$  is the number of switched DC levels that can be achieved in each phase Leg.

The average output voltage for a phase shifted carrier pulse width modulation to a particular power cell  $i$  is given by,

$$V_{oi} = 1/T_{cr} \cdot \int V_{oi}(t)dt \quad (10)$$

$$V_{oi} = T_{on}/T_{cr} \cdot V_{dc} \quad (11)$$

$$V_{oi} = V \quad (12)$$

Where,  $V_{oi}$  is the output voltage of cell  $i$ , and  $T_{on}$  is the time interval, determined by the comparison between the reference and the carrier signals.

### B. Phase shifted carrier switching frequency optimal pulse width modulation (PSC-SFO PWM)

The method takes the instantaneous average of the maximum and minimum of the three reference voltages ( $V_a, V_b, V_c$ ) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms, which is shown in fig.4b.

From the above criteria we obtain the following equation

$$V_{carrier} = \{ \max (V_a, V_b, V_c) + \min (V_a, V_b, V_c) \} / 2 \quad (13)$$

$$V_{aSFO} = V_a - V_{carrier} \quad (14)$$

$$V_{bSFO} = V_b - V_{carrier} \quad (15)$$

$$V_{cSFO} = V_c - V_{carrier} \quad (16)$$

The carrier voltage is the average of maximum and minimum value of  $V_a, V_b, V_c$ . The phase voltage using SFO is the difference between reference voltages to carrier voltage. The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

## VI. RESULTS

The total harmonic distortion (THD), which is a measure of closeness shape between a waveform and its fundamental component, is defined as

$$THD = 1/V_{01} \left( \sum_{n=2,3}^{\infty} V_{on}^2 \right) \quad (17)$$

Where,

$V_{01}$  is the fundamental rms output voltage.

$V_{on}$  is the rms value of  $n$ th harmonic component.

The table.1 shows the THD value and  $V_{ac}$  value using CSMC-SH PWM, CSMC-SFO PWM, VSMC-SH PWM and VSMC-SFO PWM. Using PSC-SH PWM and PSC-SFO PWM the THD and  $V_{ac}$  values are reduced respectively.

The table.2 shows the THD and output voltage value for PSC-SH PWM and PSC-SFO PWM. The THD value for PSC-SFO PWM was seen to be high. In spite of this high value the output voltage was improved. So, PSC-SFO PWM technique can be used where high output voltage is needed.

TABLE 1  
VARIOUS MODULATION INDEX OUTPUT VOLTAGE  
AND THD FOR MC-SH PWM AND MC-SFO PWM

Modulation Index	CSMC-SH PWM		CSMC-SFO PWM		VSMC-SH PWM		VSMC-SFO PWM	
	THD%	Vac	THD%	Vac	THD%	Vac	THD%	Vac
1.0	7.21	9.35	21.7	10.2	10.62	9.32	22.82	10.2
0.9	6.69	8.99	21.3	10.0	10.12	9.001	22.47	10.0
0.8	7.45	8.32	20.9	09.8	10.35	8.26	22.18	09.82
0.7	8.54	7.9	21.5	09.5	11.35	7.8	22.71	09.75

TABLE 2  
VARIOUS MODULATION INDEX OUTPUT VOLTAGE AND THD  
FOR PSC-SH PWM AND PSC-SFO PWM

Modulation Index	PSC PWM		PSC-SFO PWM	
	THD %	Vac	THD %	Vac
1.0	0.75	10.15	20.92	11.43
0.9	0.35	10.01	20.65	11.01
0.8	1.05	09.36	20.51	10.04
0.7	2.45	08.58	20.72	09.32

#### A. Simulation Results

To verify the proposed schemes, a simulation model for a three phase five level cascaded H-Bridge inverter is implemented. The simulation parameters for constant switching frequency multicarrier pulse width modulation are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, switching frequency 2KHz. Phase leg voltages have been calculated and drawn for CSFMC-SH PWM method in Fig.5a. Phase leg voltages have been calculated and drawn for CSFMC-SFO PWM method in Fig.5b.

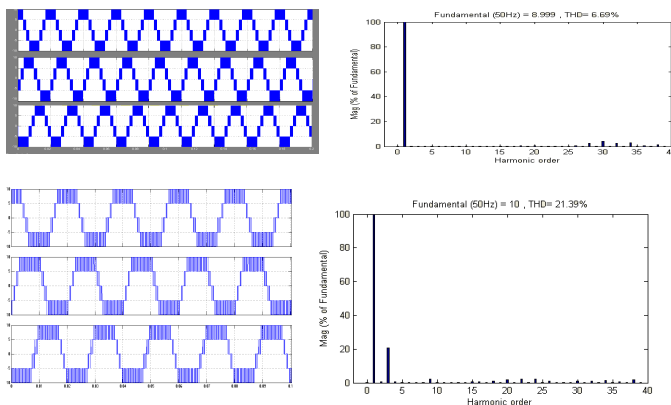


Fig. 5. Constant switching frequency multicarrier pulse width modulation output voltage and harmonic spectrum a) CSFMC-SH PWM and b) CSFMC-SFO PWM

The simulation parameters for variable switching frequency multicarrier pulse width modulation are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, switching frequency 2KHz and 4KHz. Phase leg voltages have been calculated and drawn for VSFMC-SH PWM method in Fig.6a. Phase leg voltages have been calculated and drawn for VSFMC-SFO PWM method in Fig.6b.

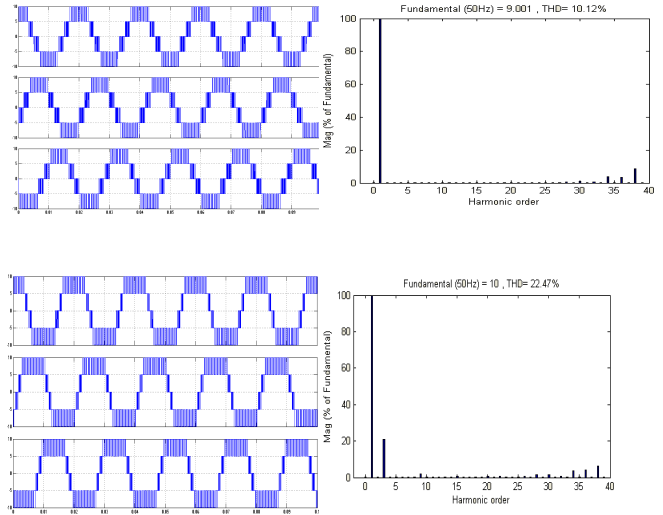


Fig 6: Variable switching frequency multicarrier pulse width modulation output voltage and harmonic spectrum a) VSFMC-SH PWM and b) VSFMC-SFO PWM

The simulation parameters for phase shifted carrier pulse width modulation are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, switching frequency 5KHz. Phase leg voltages have been calculated and drawn for PSC-SH PWM Method in Fig.7a. Phase leg voltages have been calculated and drawn for PSC-SFO PWM Method in Fig.7b.

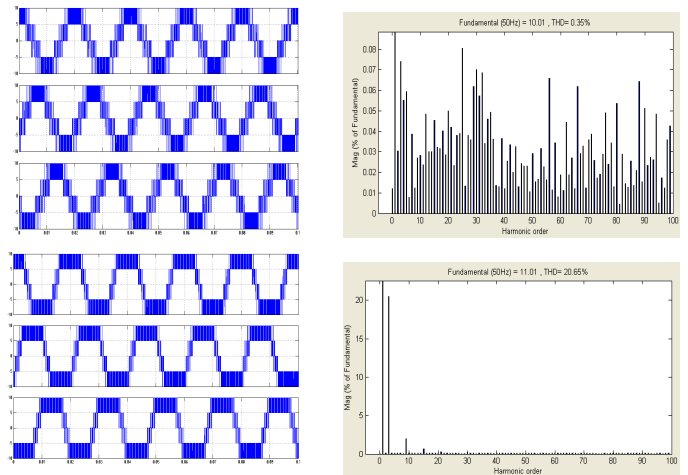


Fig. 7: Phase shifted carrier pulse width modulation output voltage and harmonic spectrum a) PSC-SH PWM and b) PSC-SFO PWM

## B. Hardware Results

A hardware setup of three phase five level cascaded inverter has been built to validate the theoretical analysis. The hardware parameters for CSFMC PWM are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, fundamental frequency 50HZ, switching frequency 2KHZ and Xilinx Spartan – DSP controller (FPGA). The three phase output voltage waveform for CSFMC-SH PWM method shown in fig.8a and CSFMC-SFO PWM method shown in fig.8b.

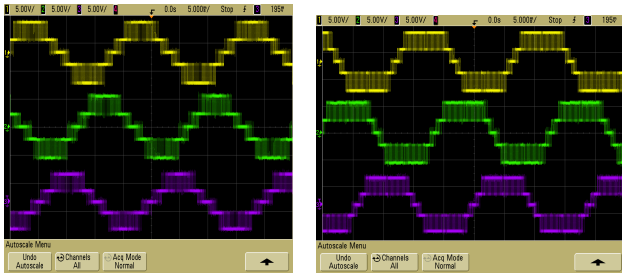


Fig 8: Constant switching frequency multicarrier pulse width modulation a) CSFMC-SH PWM output voltage and b) CSFMC-SFO PWM output voltage

The hardware parameters for VSFMC PWM are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, fundamental frequency 50HZ, switching frequency 2KHZ, 4Khz and Xilinx Spartan – DSP controller (FPGA). The three phase output voltage waveform for VSFMC-SH PWM method shown in fig.9a and VSFMC-SFO PWM method shown in fig.9b.

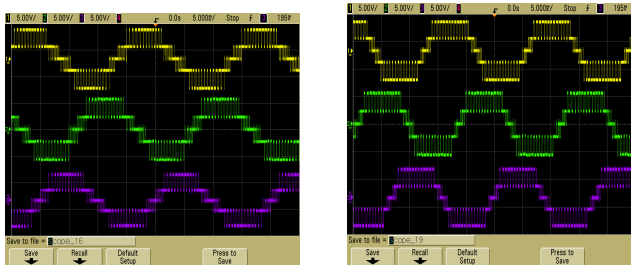


Fig 9: Variable switching frequency multicarrier pulse width modulation a) VSFMC-SH PWM output voltage and b) VSFMC-SFO PWM output voltage

The hardware parameters for PSC PWM are as following, 5KW rating, three phase load  $R = 100$  ohms,  $L = 20$ mH, each source  $V_{dc} = 5$ V, fundamental frequency 50HZ, switching frequency 2KHZ and Xilinx Spartan – DSP controller (FPGA). The three phase output voltage waveform for PSC-SH PWM method shown in fig.10a and PSC-SFO PWM method shown in fig.10b.

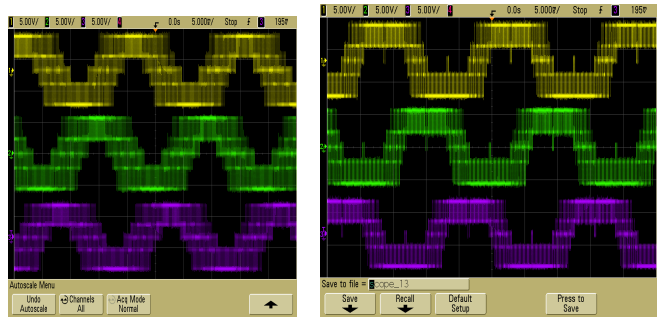


Fig.10: Phase shifted carrier pulse width modulation a) PSC-SH PWM output voltage and b) PSC-SFO PWM output voltage



Fig.11: Hardware setup of three phase cascaded multilevel inverter

## V. CONCLUSION

In this paper, three new schemes adopting the constant switching frequency multicarrier, variable switching frequency multicarrier and phase shifted carrier pulse width modulation concepts are proposed. The subharmonic pulse width modulation strategy reduces the THD and switching frequency optimal pulse width modulation strategies enhances the fundamental output voltage. The multilevel inverter improves output voltage, reduces output total harmonic distortion and voltage stress on semiconductor switches. These schemes are confirmed by simulation results and experimental results.

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