

New Topology of a Three Phase Dynamic Voltage Restorer (DVR) for Voltage Swells Mitigation in Electrical Distribution System

R.Omar N.A Rahim

Department of Industrial Power, Faculty of Electrical
University Teknikal Malaysia Melaka, Malaysia
tel/fax: +6065552224

e-mail: (author, .rosloamar@utem.edu.my)

Centre of Research for Power Electronics, Drives, Automation and Control
University of Malaya, 50603 Kuala Lumpur, Malaysia

Abstract: This paper proposed three topologies of a three phase dynamic voltage restorer (DVR), these new topologies comprises of filtering schemes, dc-link capacitor and three phase four wire of a three phase transformer connection. The new Topology of the DVR based on direct- quadrature –zero (d-q-0) transformation technique controller is presented. The proposed topologies of a DVR can compensate three phase voltage swells outages. MATLAB/SIMULINK power system toolbox is used to simulate the proposed system. To validate the effectiveness of the control proposed a three phase DVR prototype with a power rating of 5KVA has been successfully developed. Simulation and experimental results verify the capabilities of the proposed topologies in mitigating voltage swells in the distribution network. **Keywords:** filtering scheme, prototype, dynamic voltage restorer, voltage swells, three phase voltage swells in the distribution network.

Key words: filtering scheme, prototype, dynamic voltage restorer, voltage swells, three phase voltage

1. Introduction

The voltages disturbances such as voltage sags, swells, harmonics, transients and unbalance are considered are the most common power quality problems in electrical distribution systems[1]. These types of disturbances can cause fails in the equipments, raising the possibility of an energy interruption. Voltage swells can be defined as a short duration increase in rms of main source with an increase in voltage ranging from 1.1 p.u up to 1.8 p.u. of nominal voltage source. There are various solutions to these problems. One of the most effective solutions is the installation of a Dynamic Voltage Restorer (DVR), [2-5]. Traditional DVR,[6] functions by injecting three single phase AC

voltages in series with three-phase incoming voltage during disturbances, compensating for the difference between faulty and nominal voltages. Figure1. where the DVR consists of essentially a series connected injection transformer, a voltage source inverter (VSI), inverter output filter and an energy storage device connected to the dc-link. The power system upstream to DVR is represented by an equivalent voltage source and source impedance. The disturbances correction capability of the restorer depends on the maximum voltage injection capability of the device. In [7], an analysis of the energy requirement of the DVR is presented and a control scheme is proposed.

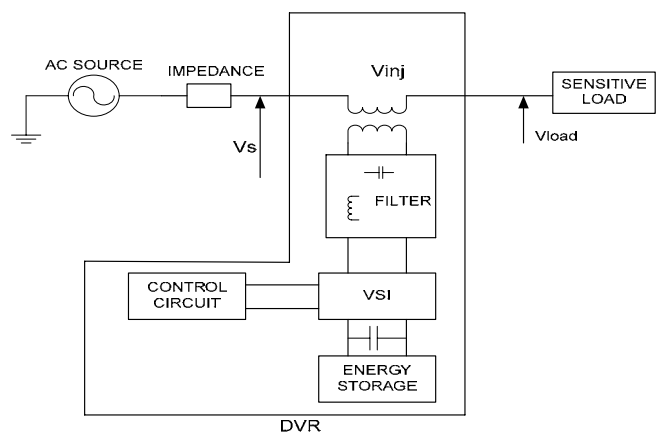


Figure 1 Conventional DVR Circuit Topology [7]

Voltage sag is a momentary decrease in the rms ac voltage from 10% up to 90% of the nominal voltage of duration from 0.5 cycles to a few seconds[8]. Voltage sags are normally caused by single and three phase fault in the distribution system and by the startup of induction motors of large rating[9-12]. Voltage

sags/swells can occurs more frequently than other power quality phenomenon. These sags/swells are the most important power quality problems in the power distribution system. IEEE 519-1992 and IEEE 1159-1995 describe the voltage sags/swells as shown in Figure 2. IEEE Standards Board (1995),

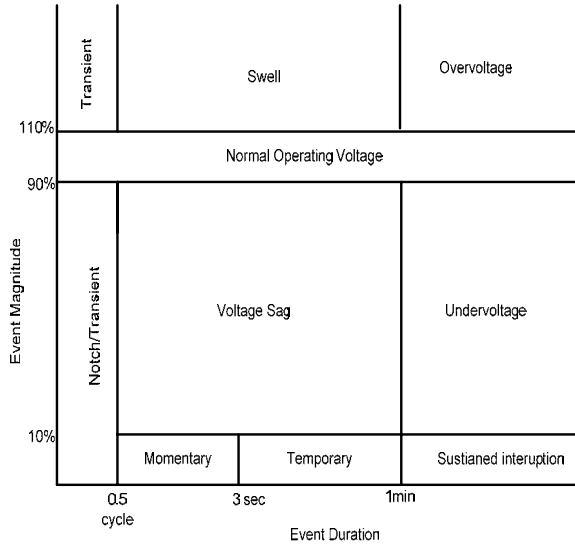


Figure 2 Voltage Reduction Standard of IEEE Std 1159-1995

2. DVR Concept in Distribution System

Figure. 1 shows a DVR is connected in series between sensitive loads in order to mitigate unbalanced loads or faults in feeder. The possibility of compensation of voltage disturbances can be limited by a number of factors including finite DVR, power rating, different load conditions, background power quality problems and different types of disturbances in the distribution system. There are several types of energy storage been used in the DVR such as battery, superconducting coil, and flywheels. These types of energy storages are very important in order to supply active and reactive power to DVR. The controller is an important part of the DVR for switching purposes. The switching inverter is responsible to do conversion process from DC to AC. The inverter ensures that only the swells or sags voltage is injected to the injection transformer[13].

In this paper, a new topology of the DVR is proposed by using a three phase four wire, three phase inverter

with six Insulated Gate Bipolar Transistor (IGBTs), DVR with split capacitors (C_{dc1} and C_{dc2}) and new installation of the capacitors filtering scheme. With these new topologies the proposed DVR offers the following advantages over the traditional DVRs:

- A Three phase four wire DVR is used, the beneficial of this configuration is that to control the zero sequence voltage during the unbalanced faults period.
- A three phase DVR with three single phase full bridge inverter has been proposed in the previous DVR. Typically, only one capacitor is used at the dc side of the inverter. In these configuration three control systems and many IGBTs switches are needed, so it's very costly.
- The placement of the capacitors filter at the high voltage side causes the harmonics for the voltage at the connected load is reduced.
- The DVR with split capacitors (C_{dc1} and C_{dc2}) causes zero sequence current to circulate through the DC –link; therefore unbalanced voltage sags with zero sequence can be compensated effectively.

3. The Circuit of The Proposed Topology

Four different system topologies for DVRs has been analyzed and tested in[7] Nielsen etl, (2005). Figure 3 illustrates a new configuration model of the proposed DVR system, and the system consists of a DC voltage source (V_{dc}), three single phase injection transformer, a three phase voltage source PWM inverter, L-C output filter and sensitive loads. In this proposed designed of DVR, special attention must be paid on three types of configuration as follows;

- Filtering schemes configuration
- Isolation or distribution transformer and
- Injection transformer winding.

Filtering configuration for DVR is very important as it related with the system dynamic response. The filtering system of the DVR can be placed either on the high voltage or the low-voltage side of the injection transformer and are referred to as line side filter and inverter-side filter respectively[14-16]. In the

proposed filtering system as shown in Figure 3, the filtering scheme is installed for both on the low and high voltages. The filter inductor, capacitor and resistor (L_{fa}, L_{fb}, L_{fc} , C_{fa}, C_{fb}, C_{fc} and R_a, R_b, R_c) are installed on low voltage side between the series inverter and the transformer and the high voltage side (C_1, C_2 and C_3), when it is placed in low voltage side, high order harmonics from the three phase voltage source PWM inverter is by pass by the filtering scheme and its impact on the injection current rating can be ignored. The type of this filtering configuration can also eliminate switching ripples produced by the inverter.

In Figure.3 also highlighted that the three phase isolation or distribution transformer has a Delta connected primary winding and a Wye connected secondary winding. The input and output rated line to line voltage of $415 V_{rms}$. The values of the load resistors R_a , R_b and R_c are chosen to be 47 ohm, therefore the current through each load resistor are as follows;

$$I_{Load \ resistor} = \frac{|V_{phase}|}{Load \ Resistor} = \frac{240V_{rms}}{47\Omega} = 5.10A_{rms}$$

The minimum apparent power with an additional 25 % safety factor can be calculated as follow;

$$\begin{aligned} S_{transformer, 1\phi} \text{ (min)} &= 1.25 \left[\sqrt{3} (V_{L-L}) (I_L) \right] \\ &= 1.25 \left[\sqrt{3} (415) (5.1) \right] \\ &= 4.6 \text{ KVA} \end{aligned}$$

Based on the value of $S_{transformer}$, the minimum ratings of a 5KVA isolation transformer was chosen. In this research a Delta-Wye step-down transformer with the neutral grounded is used. The advantages of its configuration, zero sequence current will not propagate through the transformer when unbalanced faults occur on the high voltage level. Also third harmonic voltages are eliminated by the circulation of the harmonic current trapped in the primary Delta winding. However, a Wye-Wye step down distribution transformer with the neutral grounded will not solve these problems in unbalanced fault situation.

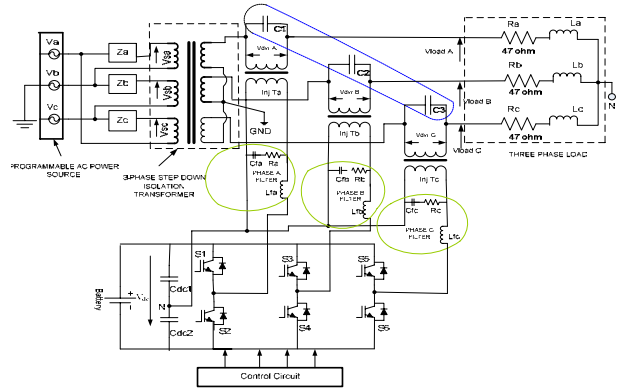


Figure 3 : New configuration of the proposed DVR [7]

A three phase DVR with three single phase full bridge inverter has been proposed in [18]. Typically, only one capacitor is used at the dc side of the inverter. In these configuration three control systems and many IGBTs switches are needed, so it's very costly. In this research a three phase four wire DVR with three phase inverter is proposed to control the zero sequence voltage during unbalanced faults.

The new types of DVR systems employ the d-q-0 transformation or Park's transformation for balanced and unbalance voltage detection. The proposed d-q-0 operated DVR system is implemented using DSP board. The main aspects of the control system are shown in Figure 4 and include the following blocks: Block 1 is used to convert the three phase load voltages (V_{La} , V_{Lb} , V_{Lc}) into the α - β -0 coordinates as in equation (1)

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \\ V_o \end{bmatrix} = Q \begin{bmatrix} V_{La} \\ V_{Lb} \\ V_{Lc} \end{bmatrix} \quad (1)$$

$$\text{Where } Q = \frac{2}{3} \begin{bmatrix} 1 & -1 & -1 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

Block 1 is also used to convert the three phase load voltages (V_{La} , V_{Lb} , V_{Lc}) into the α - β -0 coordinates as in equation (1), the three phase load voltages reference components $V_{\alpha-ref}$, $V_{\beta-ref}$ and V_o-ref can be converted to V_{d-ref} and V_{q-ref} as shown in equation (2).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (2)$$

Transformation to dqo to abc

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -0.5 & \frac{\sqrt{3}}{2} & 1 \\ -0.5 & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_o \end{bmatrix} \quad (4)$$

Block 2 is considered as a source voltages (V_{sa} , V_{sb} , V_{sc}). The amplitude of AC voltage at the sources (V_{source}) can be calculated as shown in equation (5);

$$V_{source} = \frac{2}{3} \left(\sqrt{(V_{sa})^2 + (V_{sb})^2 + (V_{sc})^2} \right) \quad (5)$$

Block 3 is a three phase PLL (Phase-locked loop). PLL comprises a Phase Detection (PD) scheme, a Loop Filter (LF), and a Voltage Controlled Oscillator (VCO). The phase difference between the input and the output signals is measured using a phase detection scheme and passed through a loop filter to generate an error signal driving a voltage-controlled oscillator (VCO) which generates the output signal. The PLL block is implemented in d-q-0 synchronous reference frame as shown in Figure 5. The PLL block allows to detect the amplitude and phase (V_s and θ) of fundamental positive sequence components of the source voltages. A PI regulator is used to control this variable and the output of this regulator is the source frequency, the source voltage angle can be obtained through the integration of the source frequency.

Block 4 is the detection scheme for the voltage Unbalanced compensator. From Figure 5 shows that, the synchronous frame variables, V_d and V_q are used as inputs for low pass filters to generate voltage references in the synchronous frame. Block 5 receive

the components of the load voltage vectors $V_{d \text{ ref}}$ and $V_{q \text{ ref}}$ and transforms them to three phase coordinates using equation (3) and (4) the generation voltages are used as the voltage reference. The DC link error in Figure 4 is used to get optimized controller output signal because the energy on the DC link will be changed during the unbalance voltage. Block 6 is the PWM block, this block provides the firing for the Inverter switches (PWM1 to PWM6). The injection voltage is generated according to the difference between the reference load voltage and the supply voltage and is applied to the voltage source Inverter (VSI).

In this research a Delta-Wye isolation or distribution transformer with the neutral grounded is used. The advantages of its configuration, zero sequence current will not propagate through the transformer when unbalanced faults occur on the high voltage level. The DVR with split capacitors (C_{dc1} and C_{dc2}) causes zero sequence current to circulate through the DC-link; therefore unbalanced voltage sags with zero sequence can be compensated effectively. A Three phase four wire DVR is used, the beneficial of this configuration is that to control the zero sequence voltage during the unbalanced faults period the placement of the capacitors filter at the high voltage side causes the harmonics for the voltage at the connected load is reduced. The used PLL algorithm is based on a fictitious electrical power (three phase dq PLL), the selected structure has a simple digital implementation and therefore low computational burden. An improvement of the proposed controller uses the d-q-0 rotating reference frame as its accuracy is high as compared to stationary frame-based techniques. The proposed controller is able to detect the voltage disturbances and control the inverter to inject appropriate voltages in order to restore the load voltage. This control strategy uses the d-q-0 rotating reference frame because it offers higher accuracy than stationary frame-based techniques.

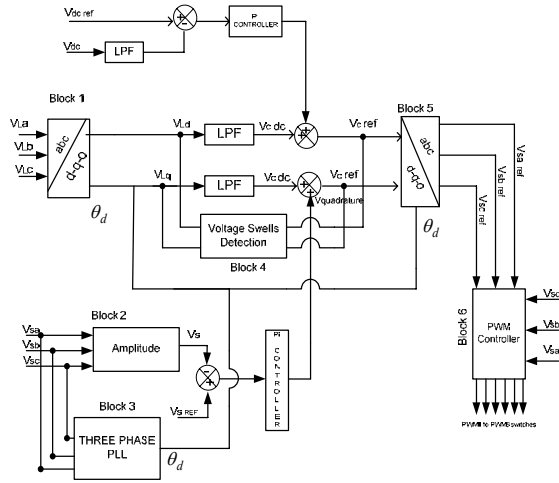


Figure.4: Block Diagram Control of the proposed Scheme of DVR for Voltage Swells Detection

4. Results and Discussion

The system modeled in Figure 3 has been simulated using Matlab/Simulink. The performance of the system has been considered with the load is represented by a series equivalent rated at $415V_{rms}$, 5KVA at 0.95 load power factor. Simulation and experimental parameters are given in Table 1. The performance of the DVR for different supply disturbances is tested under various operating conditions. Several simulation of the DVR with proposed controller scheme and new configuration of it have been made.

As for the filtering scheme is placed in the high voltage side in this case, high order harmonic currents will penetrate through the injection transformer and it will carry the harmonic voltages. Fast Fourier Transform (FFT) analyses for the output voltage at the connected load has been done without or with capacitors filter (C_1 , C_2 and C_3) at the high voltage level side of the transformer as shown in Figure 6. Figure.6 (a) shows that FFT analysis when the transformer at the high voltage level is not installed with the capacitors filter. The Total Harmonics Distortion (THD) for the voltage is about 8.8%. When the capacitors filter are placed at the high level side, THD value decreases to 0.38% as shown in Figure. 6(b). Thus the harmonics are reduced from 8.8 % to 0.32%. The THD value of 0.32 % when capacitors filter are placed at the high voltage transformer side is satisfying the IEEE-519 standard harmonic voltage limit.

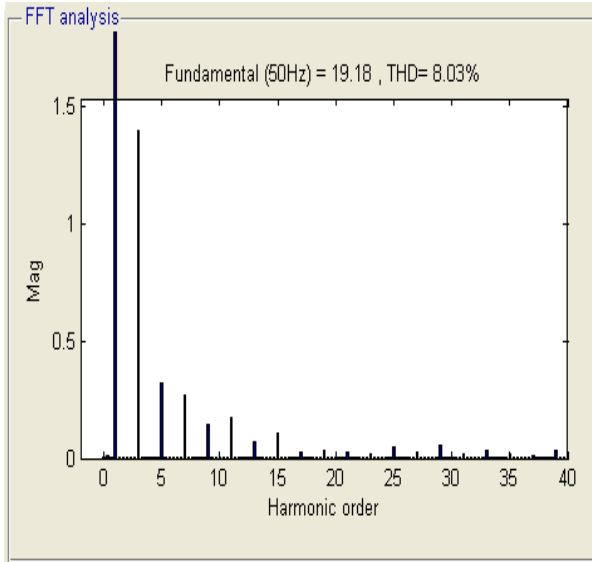
Table 1: Simulated And Experimental System Parameters

Main Supply Voltage per phase	$415 V_{rms}$
Line Impedance $L_s = 0.5mH$ $R_s = 0.1 \Omega$	
Series transformer turns ratio	1:1
DC Bus Voltage	100V
Filter Inductance	2mH
Filter capacitance	1uF
Load resistance	47 Ω
Load inductance	60mH
Line Frequency	50Hz
Switching Frequency	5kHz

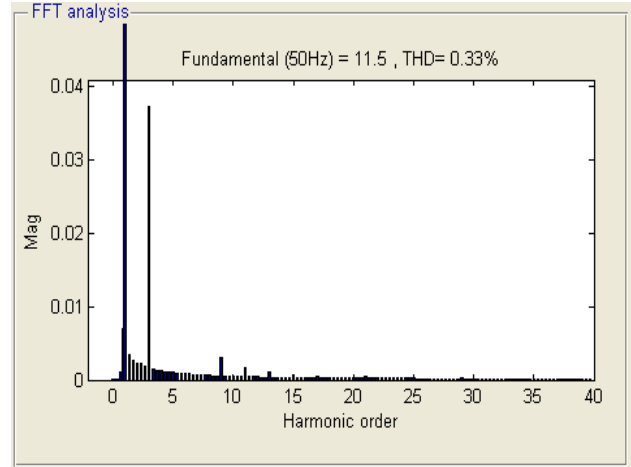
Investigation on the DVR performance can be observed through testing under various disturbances condition on the source voltage. The proposed control algorithm was tested for balanced and unbalanced voltages swells in the low voltage distribution system. In case of balance voltage swell, the source voltage has increased about 20-25% of its nominal value. The simulation results of the balance voltage swells as shown in Figure 7(a). The swells voltages occur at the time duration of 0.06s and after 0.12 s the voltage will restore back to its normal value. The function of the DVR will injects the missing voltage in order to regulate the load voltage from any disturbance due to immediate distort of source voltage. The restore voltage at the load side can be seen in Figure 7(b). The Figure shows the effectiveness of the controller response to detect voltage swells quickly and inject an appropriate voltage. In case of unbalance voltage swells, this phenomenon caused due to single phase to ground fault. One of the phases of voltage swells have increased around 20-25% with duration time of swells is 0.06 s. The swells voltage will stop after 0.12 s. At this stage the DVR will injects the missing voltage in order to compensate it and the voltage at the load will be protected from voltage swells problem. The third simulation study is to show the performance of proposed configuration DVR for one single phase to ground fault. As shown in Figure 7(a) the proposed topology injects the desired voltage to the grid in order to mitigate voltage swells in the distribution system. From the results, the swells load terminal voltage is restored and help to maintain a balanced and constant to its nominal voltage.

In order to assess the operation of the proposed system a small scale prototype of DVR was built and tested.

The prototype developed based on schematic in Fig.3, all the system parameters for the hardware designed as shown in Table 1. The prototype is rated to protect 5KVA load 40% voltage sags mitigation and in case of unbalance voltage at the Point of Common Coupling (PCC) is set at 10%-20% and the three phase load comprising of $47\ \Omega$ and 60mH inductor. The proposed control strategy is implemented digitally in DSP TMS320F2812. The DSP was selected as it has a 32-b CPU operating at 150MHz. The voltage and current sources were sent to the analog digital converter of the DSP. The sampling times are governed by the DSP timer called a CpuTimer0 which generates periodic interrupt at each sampling times T_s . The Interrupt Service Routine (ISR) will read the sampling value of the voltage and current source from the analog digital converter (ADC) The DSP controller offers a display function, which monitor the disturbances in the real time. The control algorithm which is proposed in section II is tested with a control using DSP TMS 320F 2812. The controller has its own ADC converters and PWM pulse outputs. The inputs of a 3-leg Voltage Source Inverter (VSI) are the PWM pulses which are generated by the digital controller.

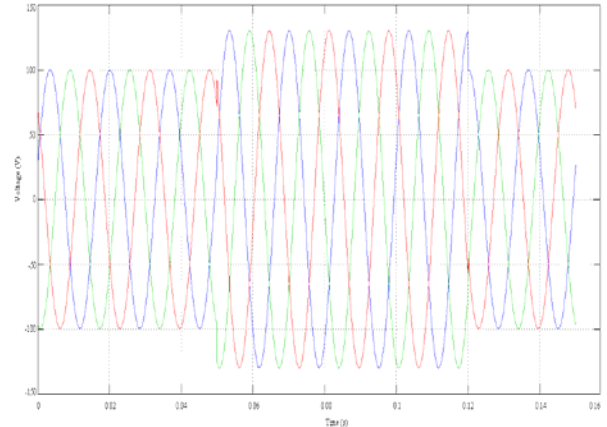


(a)

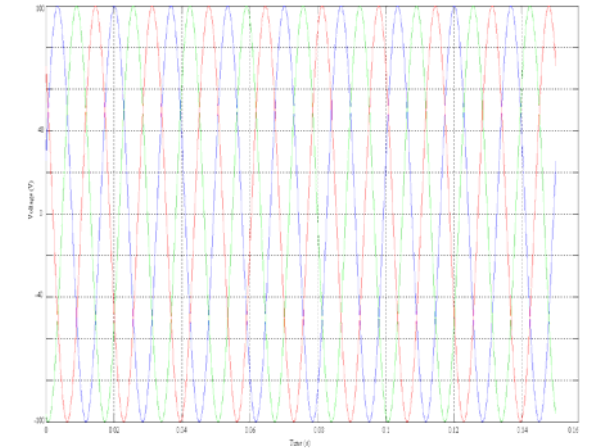


(b)

Figure 6(a) and (b). FFT Analysis for Voltage without or with Capacitors Filter

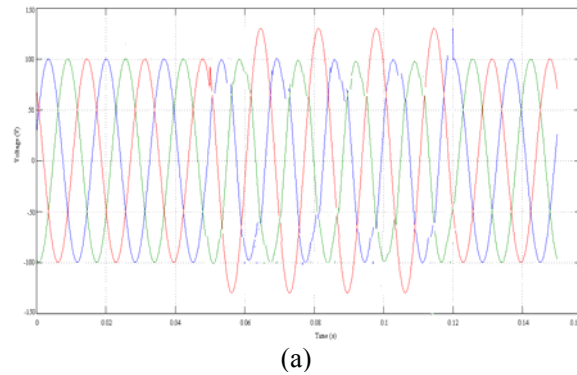


(a)



(b)

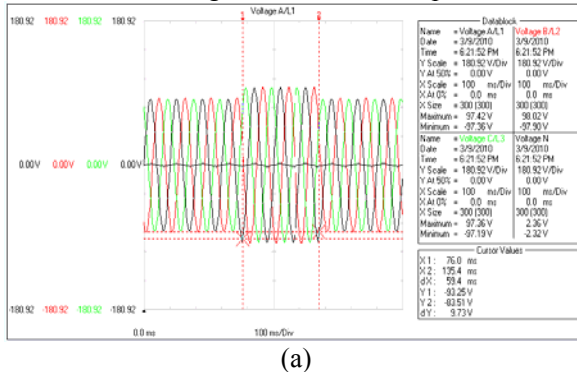
Figure 7 (a) and (b). Balanced Voltages Swells and Load Voltages Compensation



(a)

(b)

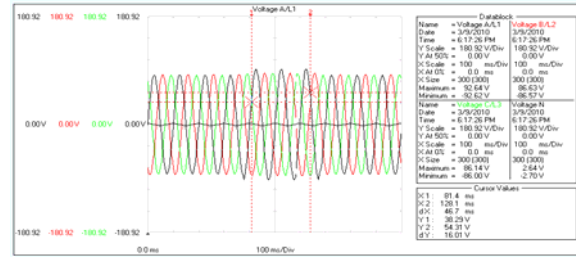
Figure 8(a) and (b). One Phase Voltage Swells and Voltage Swells after Compensation



(a)

(b)

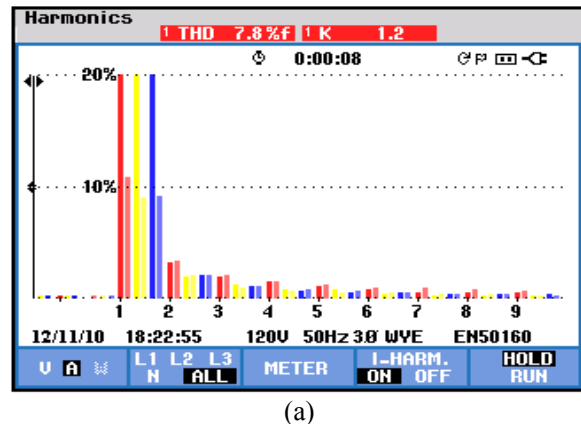
Figure 9(a) and (b). Balanced Voltages Swells and Compensation of balanced Voltages Swells



(a)

(b)

Figure 10(a) and (b). One Phase Voltage Swell and Compensation of Voltages swells



(a)

(b)

Figure .11: (a) Total Harmonic Distortion Current (THD_i) under unstable dc-link (b) Total Harmonic Distortion Current (THD_i) under stable dc-link.

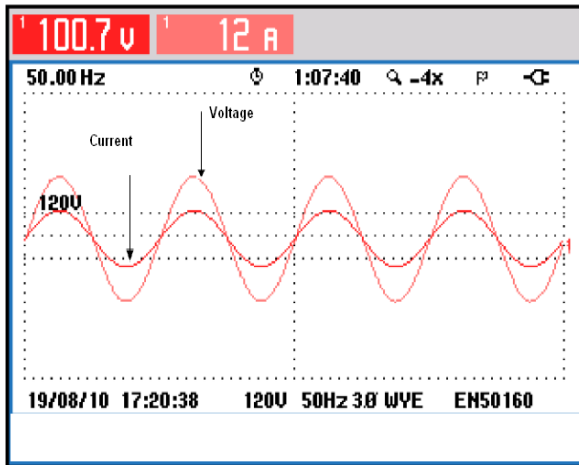


Figure.12. Phase voltage and current at the connected load

The switching frequency of the inverter is 5 kHz. To start up the test, the loads are first powered by the utility, the low voltage prototype DVR was fed with a programmable AC power source 6560/6590. The prototype is rated to protect 5KVA load with 25% voltage swells from their nominal voltage. All the components part of the DVR has been integrated according to the parameters in the Table 1. A DSP TMS320F2812 board was used for the control scheme. The sampling frequency is set at 10 kHz. The source voltages V_{sa} , V_{sb} , V_{sc} are measured by the voltage sensor, and then its signals are entered into the DSP board. The output currents of the inverter is measured by using current sensor and then sensed by the DSP board to boost up the voltage response of the DVR.

In the experiment, a 25% three phase and single phase swells are generated from their nominal voltage. The experimental results obtained for both conditions are shown in Figures 9 and 10 respectively. Figure 9(a) shows the waveform of utility voltage when the tested system suffered a disturbance of 25% voltage swells. Balanced voltage swells are created immediately after a fault. The DVR injects fundamental voltage in series with the supply voltage. Figure 9(b) shows the load terminal voltages which are restored through the compensation by DVR. The capabilities of the DVR in mitigating one single phase to ground fault is also investigated. Figure 10 (a) shows the series of voltages components for unbalanced conditions for one phase to ground fault. The DVR load voltages are shown in Figure 10 (b). As can be seen the swells load terminal voltage is compensated and help to maintain a balanced and constant load voltage and the control method that can generate the required voltages from

significantly disturbance source voltages. As shown in Figure 3 there are two DC-link capacitors were used, it acts as an energy storage element of the DVR. The rating of the IGBT is totally depending on the DC link of the DVR prototype. Harmonic current is depending on the DC link voltage. The function of the DC link is to absorb the ripple, therefore the values of the DC side capacitors (C_{dc1} and C_{dc2}) should be large enough without the distorting the dc bus voltage much. If there is distortion in the dc voltage the inverter output will get distorted with third harmonic content. With the stability of the DC bus and the Total Harmonic Distortion for current (THD_I) for third harmonics current is reduced 7.8 % to 2.8% as shown in Figure. 11(a) and 11(b). Phase voltage and current at the load are the sinusoidal waveform without any distortion due to design of the good capacitor filter and use of the suggested controller, this can be seen in Figure 12.

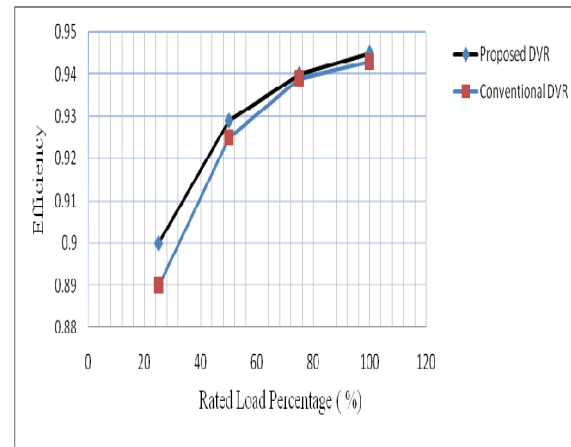


Figure 13. Efficiency for Proposed and Conventional DVRs

The efficiencies between the proposed DVR with capacitors filter scheme as shown in Figure 3 and the conventional DVR without capacitors filter have been compared and it is observed that the proposed DVR is more efficient than the conventional one as shown in Figure 13.

5. Conclusions

A new configuration of a DVR is proposed in this research. The proposed method can protect customer's equipment from potential voltage swells. The capabilities of the proposed topologies and an improvement of d-q-o controller can be seen from

Simulation and experimental results in mitigating of voltage swells in the distribution system. The experimental results show that the performance of the DSP controller is satisfactory in mitigating disturbances in the network such as voltage swells. These results validate the proposed strategy for the detection and control of the DVR, from voltage swells problems.

References

- [1] Elnady and M.M. A. Salama, "Mitigation of Voltage disturbances using adaptive perception – based control algorithm," IEEE Trans. Power Delivery., vol. 20,no.1,pp,309-318, Jan.2005.
- [2] M.F. Alves, T.N. Ribeiro, "Voltage Sag an Overview of IEC and IEEE Standards and Application Criteria, Proceedings of IEEE Conference on Transmission and Distribution, 1999,Vol 2. pp. 585-589.
- [3] P. Boonchiam, and N. Mithulananthan, Dynamic Control Strategy in Medium Voltage DVR for Mitigating Voltage Sags/Swells International Conference on Power System Technology, 2006, pp. 1-5.
- [4] Ezoji, A. Sheikholeslami, M.Tabasi and M.M. Saeednia, Simulation Of Dynamic Voltage Restorer Using Hysteresis Voltage Control, European Journal of Scientific Research (EJSR), 27(1) (2009), pp. 152-166.
- [5] M.R. Banaei, S.H. Hosseini, S.Khanmohamadi and G.B.Gharehpetian, Verification of a New Energy Control Strategy for Dynamic Voltage Restorer by simulation, ELSEVIER Simulation Modeling Practice and Theory, 14(2006),pp. 113-125.
- [6] M. Vilathgamuwa, A. A. D. Ranjith Percra and S. S. Choi, "Performance Improvement of The Dynamic Voltage Restorer with Closed-Loop Load Voltage and Current-Mode Control", IEEE Transactions on Power Electronics, vol. 17, no. 5, Sept.2002,pp.824-834.
- [7] J.G. Nielsen and F. Blaabjerg, "A Detailed Comparison of system J Topologies for Dynamic Voltage Restorer", IEEE Transaction on Industrial Applications, vol.41, no.5, Sept/Oct.2005, pp.1272-1280.
- [8] IEEE Standards Board (1995), "IEEE Std. 1159-1995", IEEE Recommended Practice for Monitoring Electric Power Quality". IEEE Inc. New York.
- [9] C.S.Lam, M.C.Wong, and Y.D.Han, "Voltage swell and over-voltage compensation with unidirectional power flow controlled dynamic voltage restorer, " IEEE Trans. Power Delivery.,vol.23, no.4, pp. 2513-2521, Oct. 2008.
- [10] B.Wang, G.Venkataramanan, and M.IIindala, "Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converter, "IEEE Trans.Power Electron.,vol.21, no.4, pp. 1053-1061 Jul. 2006.
- [11] P.R. Sanchez, E.Acha, J.E.O. Calderon, V.Feliu, and A.G. Cerada, "A versatile control scheme for a dynamic voltage restorer for a dynamic voltage restorer for power quality improvement, "IEEE Trans. Power Delivery.,vol. 24, no.1, pp. 277-284 Jan. 2009.
- [12] M.H.J. Bollen, Understanding power quality problems: voltage sags and interruptions, New York, IEEE Press,1999.
- [13] D. Sabin, "An assessment of distribution system power quality," Elect.Power Res. Inst., Palo Alto, CA,EPRI Final Rep. TR-106294-V2, vol. 2, Statistical Summary Report, May 1996.
- [14] H Kim, J H Kim and S K Sul , "A Design Consideration of Output Filters for dynamic Voltage Restorer " 35th Annual IEEE Power Electronic Specialist Conference 2004.
- [15] S.Sasitharan, Mahesh K. Mishra, B. Kalyan Kumar, V. Jayashankar "Rating and design issues of DVR injection transformer" International Journal of Power Electronics 2010 - Vol. 2, No.2 pp. 143 – 163.
- [16] G. Zhou, X Shi, C. Fu and Y. Wang, "Operation of a Three phase Soft Phase Locked Loop Under Distorted Voltage Conditions Using Intelligent PI Controller," in Proc. 2006 IEEE Region 10 Conf. (TENCON 2006), pp 315-320.
- [17] Rosli Omar and N.A Rahim "Design Requirement for a Dynamic Voltage Restorer for Voltage Sags Mitigation in Low Voltage Distribution System" Journal of Electrical Engineering 2010- Volume 10.
- [18] Yop Chung, Sang-Young Park et al. "The Control and Analysis of Zero Sequence Components in DVR System "Power Engineering Society Winter Meeting, 2001, IEEE, Vol 3, pp.1021-1026, 2001.