Balanced and Unbalanced Voltage Sag/Swell Compensation Using DVR Based on Energy storage device

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Abstract**—***To mitigate voltage disturbances in low voltage distribution system dynamic voltage restorer (DVR) with energy storage device is used in this paper. DVR is installed between supply and load which will inject voltage and active power to the distribution system during balanced/unbalanced voltage sag and swell disturbances. The super capacitor is used as an energy storage device in this paper. The performance of the DVR depends on control strategy used. In this work SRF Theory with Proportional Integral (PI) controller is used as an control technique. The performance of DVR for various disturbances is compared with and without energy storage device. The simulations are carried out using MATLAB/SIMULINK software.*

Key words: *DVR, SRF theory (synchronous reference theory), PI Controller, un balanced voltage sag/swell, balanced voltage sag/swell*

1. Introduction

In power distribution systems the advent of a large numbers of sophisticated electrical and electronic equipment, such as computers, programmable logic controllers and variable speed drives causes various power quality problems like voltage sag, voltage swell and harmonics. These are the major concern of the industrial and commercial electrical consumers due to enormous loss in terms of time and money, in which voltage sag and swell are major power quality problems [1].

The voltage sag is defined as reduction of the RMS value of AC Voltage for a short duration of time. Voltage sags are mainly associated with short circuit incidences. The increase in RMS value AC Voltage in short duration of time is called voltage swell in distribution system. The voltage sag and swell is divided into balanced and unbalanced voltage sag and swell. In balanced voltage sag &swell, voltage decreases and increase in all three phases simultaneously respectively. In unbalanced voltage sag &swell voltage decrease and increases in only one phase at a time [2,4]. This unbalanced/ balanced voltage sag and swell can be compensated by using DVR.

DVR is the one of the best FACTS device compared to all other FACTS control devices. DVR is well suited to protect sensitive loads from balanced/unbalanced voltage sag and swell. DVR is basically a controlled voltage source installed between the supply and a sensitive load. The DVR injects voltage to the system in order to compensate any disturbance occur due to supply [3].

The performance of DVR depends up on control strategy used. In this paper SRF Theory with Proportional Integral (PI) controller technique is used for compensation of balanced/Unbalanced voltage sag and swell. This paper is organized as follows: Section II. Presents System Configuration, Section III. Gives Dynamic Voltage Restorer with super capacitor, Section IV. Discusses Control Strategy of Proposed System, Section V. presents Results and Discussion, finally Section VI. gives Conclusion.

2. System Configuration

Fig-1. Shows system configuration of the three phase distribution system connected to the DVR.

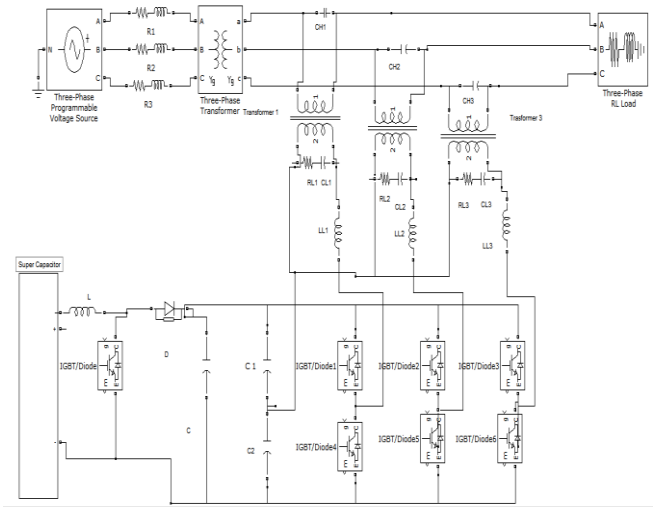


Fig.1 Schematic diagram of DVR connected in three phase distribution system

The three phase programmable voltage source is connected to the three phase sensitive load via three phase transformer. Disturbance at the source side, affect the performance of sensitive loads. This disturbance can be compensated by DVR and it is connected in series to the system via injection transformer. The compensated voltage obtained from the DVR is injected to the system through the injection transformer. The DVR unit is built with VSI unit and super capacitor. The operation VSI unit depends on the control signals received from the control unit. The DVR is represented by ideal voltage source. The reference voltages are generated from controlled algorithm tracked by controller [5, 6].

The proposed DVR is connected to the system through the three single phase injection transformers. DVR is designed according to the voltage needed in the secondary side of transformer. The DVR consists of three single phase VSI units. Each unit is connected to system through the injection transformer. It provides the isolation to the converter. The active power injection to the compensator is obtained from Super capacitor as energy storage. Each phase of the proposed topology consist of R, L, C filters. The filters are installed on either low voltage or high voltage side of injection transformer. The filter circuit comprises R_{L1}, L_{L1}, C_{L1}, R_{L2}, L_{L2}, C_{L2} R_{L3}, L_{L3}, C_{L3}, are installed on the low voltage side in between transformer and inverter. The harmonics appears across the low voltage side of transformer is eliminated using low voltage side filters and on high voltage side capacitors filters C_{H1}, C_{H2}, C_{H3} are placed. The higher order harmonics are appeared at the high voltage side of the transformer and eliminated using high voltage side capacitors filters [7, 8].

3. Dynamic Voltage Restorer

The major objective of the DVR is to increase the power utilization capacity of distribution feeders, reduce the losses and improve power quality at the load. The main assumption is to neglect the variations in the source voltages. This essentially implies that the dynamics of the source voltage is much slower than the load dynamics.

DVR is a series voltage controller and it is connected in series with the load. DVR consists of an injection transformer, harmonic filter circuit, and voltage source Inverter, controller and dc charging circuit. In place of dc charging circuit super capacitor is used to increasing the energy storage capacity [3-5].

The power circuit of DVR consists of four components and these are:

Voltage Source Inverter (VSI)

Voltage Source Inverter consists of storage device and switching devices. It can generate a sinusoidal voltage at required frequency, magnitude and phase angle. In DVR application the VSI is used as a temporary replace the supply voltage or generate the supply voltage which is missing.

Boost or Injection Transformers

Three single phase transformers are connected in series with the distribution feeder to couple the VSI to the higher distribution voltage level. The three single transformers can be connected with star/open star winding or delta/open star winding. The latter does not permit the injection of the zero sequence voltage. The choice of the injection transformer winding depends on the connections of the step down transformer that feeds the load.

Harmonic Filters

The harmonic filters can be placed either on the high voltage side or the converter side of the injection transformer. The advantages of the converter side filters are (i) the components are rated at lower voltage and (ii) higher order harmonic currents are not allowed through the transformer windings.

Energy Storage

This is required to provide active power to the load during deep voltage sags. It is also possible to provide the required power on the DC side of the VSI by an auxiliary bridge converter that is fed from an auxiliary AC supply. In this super capacitor is used as energy storage device.

4. Control Strategy of Proposed System

Fig-2. Shows the control strategy of the proposed system.

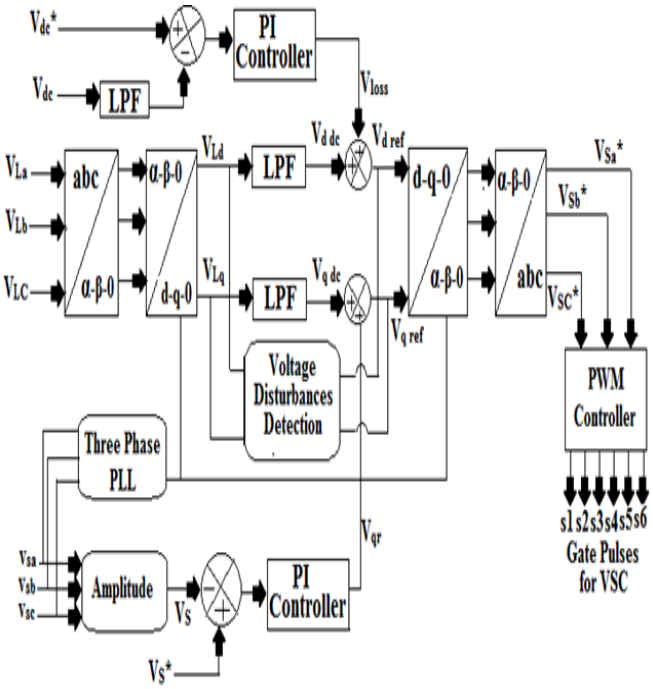


Fig-2. Block diagram of the proposed control scheme for DVR

The control Scheme of DVR is divided in to two parts

a) Reference signal is obtained from the feedback signals

b) Generation of gate signals by using PWM controller and comparison of the reference signal and sinusoidal signal.

In the proposed control Scheme reference signals are generated by using SRF Theory with Proportional Integral (PI) controller technique [9, 10].The reference signals obtained from, the three phase Load voltages are transformed in to α-β-0 axis using following transformation equation.

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} V_{La} \\ V_{Lb} \\ V_{Lc} \end{bmatrix} \quad (1)$$

The reference voltages in d-q-0 frame are obtained by using angle θ. The θ angle is obtained from Three Phase PLL Controller. The transformation for α-β-0 to d–q–0 frame is obtained using Equation (2) [11].

$$\begin{bmatrix} V_0 \\ V_{Ld} \\ V_{Lq} \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} \quad (2)$$

A three phase PLL (Phased lock loop) includes a phase detection scheme, loop filter [9-12]. In phase detection scheme difference in the input and output signal is measured and passed to a loop filter, to generate an error signal which generate output voltage.

The signal obtained from synchronous frame variables will be V_{Ld}, V_{Lq} is passed through Low pass filter to generate exact reference signals. The each voltage component has an average value and oscillating value as given by

$$V_{Ld} = V_{d\,dc} + V_{d\,ac} \quad (3)$$

$$V_{Lq} = V_{q\,dc} + V_{q\,ac} \quad (4)$$

The fundamental voltage component is transferred into average value or dc component and all other higher order harmonic voltage component including negative sequence voltage component are transferred into non dc quantities, They constitute oscillatory component. The oscillatory component appears like ripples. After eliminating the oscillatory voltage component by using filter, the reference voltage components are given in Equation (5) & (6).

$$V_{Ld} = V_{d\,dc} \quad (5)$$

$$V_{Lq} = V_{q\,dc} \quad (6)$$

Source must to deliver the direct axis load voltage component (V_{Ld}) along with the active power voltage component for maintaining the dc bus and meeting the losses (V_{loss}) in DVR. The output of PI controller at the dc bus voltage of DVR is considered as the voltage (V_{loss}) for meeting its losses [12].

$$V_{loss(n)} = V_{loss(n-1)} + K_{pd}(V_{de(n)} - V_{de(n-1)}) + K_{id}V_{de(n)} \quad (7)$$

Where $V_{de(n)} = V^*_{dc} - V_{dc(n)}$ is the error between the reference (V^*_{dc}) and sensed(V_{dc}) dc voltage at the nth sampling instant. K_{pd} and K_{id} are the proportional and the integral gains of the dc bus voltage PI controller

Now the reference voltage is

$$V_{d\,ref} = V_{d\,dc} + V_{loss} \quad (8)$$

The sum of quadratuer axis voltage component ($V_{q\,dc}$) and the component obtained from PI controller (V_{qr}) is used to regulate the voltage at the load end.

The amplitude of ac source voltage Vs is obtained using equation (9)

$$v_{source} = \frac{2}{3}\left(\sqrt{(v_a)^2 + (v_b)^2 + (v_{ac})^2}\right) \quad (9)$$

The amplitude of ac terminal voltage (V_s) at the load, controlled to its reference voltage (V^*_s) using PI controller. The output of PI controller is considered as reactive voltage component (V_{qr}).The reactive voltage component (V_{qr}) is used for Zero voltage regulation at the load end. The reactive voltage component (V_{qr}) is given equation (10)

$$V_{qr(n)} = V_{qr(n-1)} + K_{pq}(V_{te(n)} - V_{te(n-1)}) + K_{iq}V_{te(n)} \quad (10)$$

Where $V_{te(n)} = V^*_s - V_{s(n)}$ is the error between the reference (V^*_s) and actual(V_s) terminal voltage amplitude at the nth sampling instant. K_{pq} and K_{iq} are the proportional and the integral gains of the PI controller [11-14].

Now the quadratuer axis reference voltage is given by

$$V_{q\,ref} = V_{q\,dc} + V_{qr} \quad (11)$$

The reference voltage signals $V_{d\,ref}$, $V_{q\,ref}$ are transformed in to α-β-0 frame obtained by using following transformation Equation (12).[15].

$$\begin{bmatrix} v^*_{s0} \\ v^*_{s\alpha} \\ v^*_{s\beta} \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & cos\theta & -sin\theta \\ 0 & sin\theta & cos\theta \end{pmatrix} \begin{bmatrix} 0 \\ V_{d\,ref} \\ V_{q\,ref} \end{bmatrix} \quad (12)$$

The reference voltages in a-b-c reference frame is obtained by Equation (13)

$$\begin{bmatrix} V^*_{sa} \\ V^*_{sb} \\ V^*_{sc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} 0 & 1 & 0 \\ 0 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} v^*_{s0} \\ v^*_{s\alpha} \\ v^*_{s\beta} \end{bmatrix} \quad (13)$$

The reference signals obtained from the controlled block is transferred to PWM controller block to generate the required gate signals to the voltage source converter for compensation of disturbance in supply and load voltage [16-17].

3. Results and Discussion

The performance of DVR with the proposed Method is evaluated using Matlab/Simulink Software. The simulation results are obtained for the following Disturbances at the source side.

Case –a: Unbalanced Voltage Sag
Case –b: Unbalanced Voltage Swell
Case –c: Unbalanced Voltage Sag &Swell
Case –d: balanced Voltage Sag
Case –e: balanced Voltage Swell
Case –f: balanced Voltage Sag &Swell

CASE-a: Unbalanced Voltage Sag

The unbalanced voltage sag disturbance at source side causes 30% of voltage sag on phase -A. due to this, the phase -A voltage is 30% smaller than from phase -B

and phase-C voltages. The unbalanced Voltage sag is occurred from 0.08m sec to 0.14m sec as shown in fig-1(a). This unbalanced sag causes 30% of disturbance in source current wave form from 0.08m sec to 0.14m sec as shown in fig-1(b). This unbalanced sag also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to unbalanced voltage sag is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage from the duration 0.08m sec to 0.14m sec is as shown in fig-1(c). Using DVR load Current is compensated due to unbalanced sag. The compensated load Current from the duration 0.08m sec to 0.14m sec is as shown in fig-1(d).The corresponding DVR injected voltage, for the disturbances of voltage sag as shown in fig-1(e). Its corresponding DC link voltage wave forms are shown in fig-1(f).

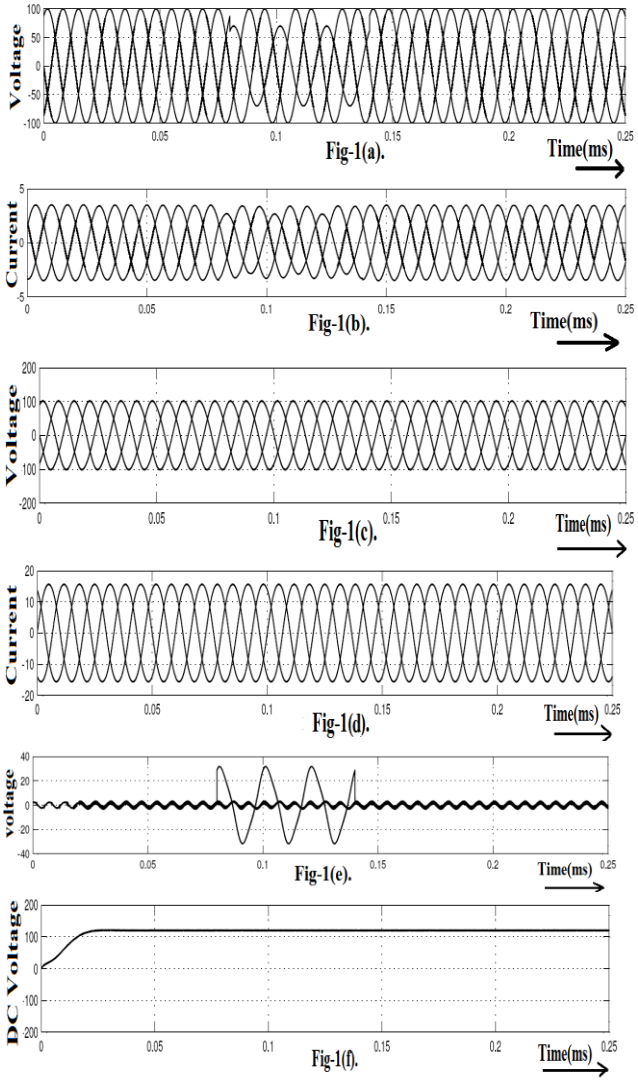


Fig-1(a).Source voltage wave form for 30% of unbalanced voltage sag, Fig-1(b).Source current wave form for 30% of unbalanced voltage sags, Fig-1(c). Compensated Load voltage wave form, Fig-1(d). Compensated load Current wave form, Fig-1(e).DVR Injection voltage during compensation, Fig-1(f). DC link voltage across the super capacitor.

CASE-b: Unbalanced Voltage Swell

The unbalanced voltage Swell disturbance at source side causes 30% of voltage Swell on phase -A. due to this, the phase -A voltage is 30% more than from phase -B and phase-C voltages. The unbalanced Voltage Swell is occurred from 0.08m sec to 0.14m sec as shown in fig-2(a). This unbalanced Swell causes 30% of Swell disturbance in source current wave form from 0.08m sec to 0.14m sec as shown in fig-2(b). This unbalanced Swell also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to unbalanced voltage Swell is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage from the duration 0.08m sec to 0.14m sec is as shown in fig-2(c).Using DVR load Current is compensated due to unbalanced Swell. The compensated load current from the duration 0.08m sec to 0.14m sec is as shown in fig-2(d).The corresponding DVR injected voltage, for the disturbances of voltage Swell as shown in fig-2(e). Its corresponding DC link voltage wave forms across Super capacitor are shown in fig-2(f).

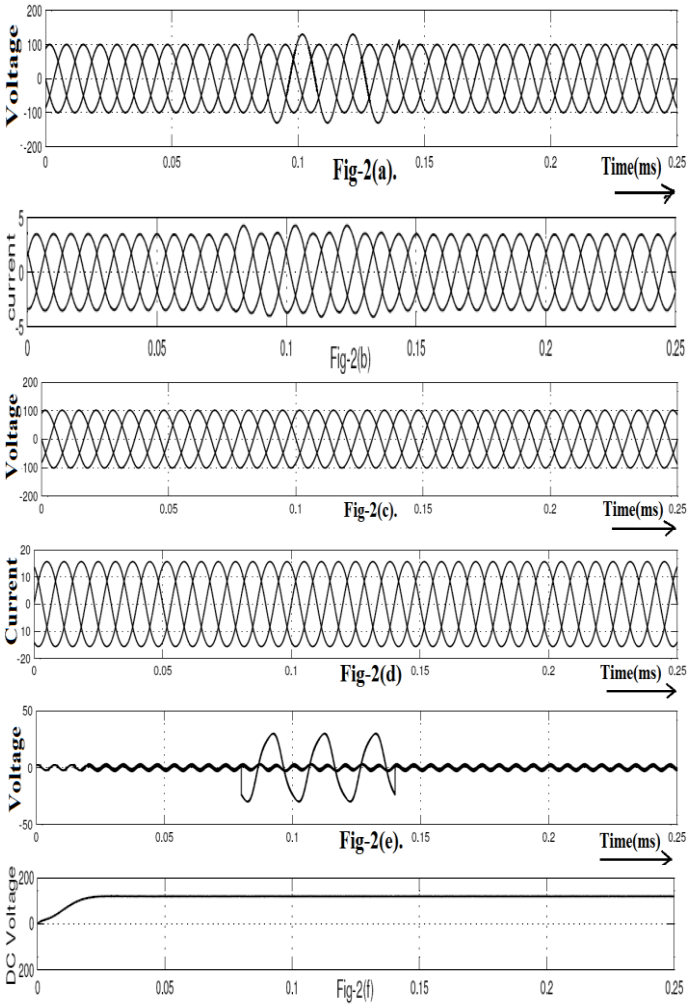
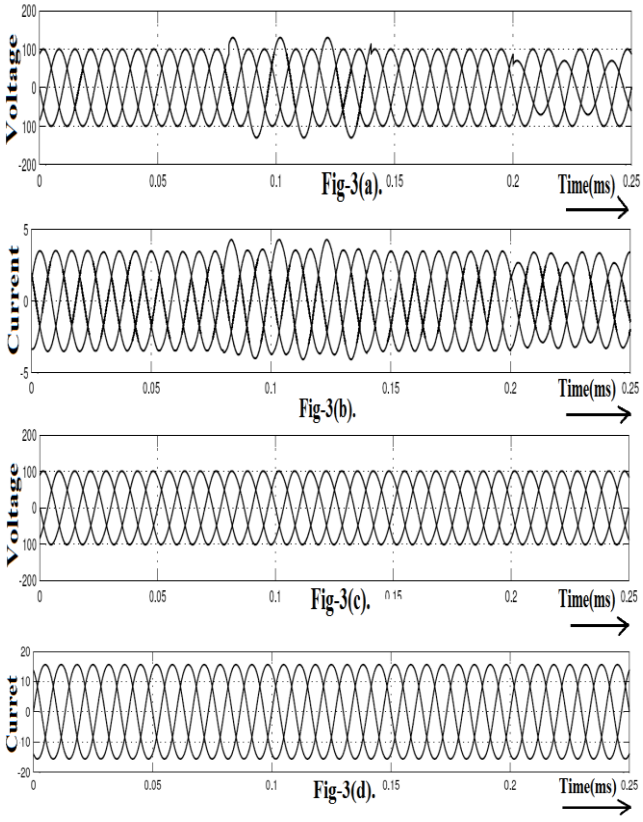


Fig-2(a).Unbalanced voltage swells at the Source side, Fig-2(b).Unbalanced swell current at the source side,

Fig-2(c).Compensated load voltage, Fig-2(d).Compensated load current, and Fig-2 (e) .DVR Injected voltage during compensation, Fig-2(f). DC link voltage across super capacitor.

CASE-C: Unbalanced Voltage Swell & Sag

The unbalanced voltage Swell & Sag disturbance at source side causes the 30% of voltage Swell & Sag magnitude on phase –A. due to this, the phase -A voltage magnitude is 30% smaller during sag, more in the swell compared to the phase -B and phase-C. The unbalanced Swell is occurred from 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown fig-3(a). This unbalanced Swell & Sag causes 30% Swell disturbance in source current wave form from 0.08m sec to 0.14m sec and 30% Sag disturbance in source current wave form from 0.2m sec to 0.25m sec as shown in fig-3(b). This unbalanced Swell & Sag also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to unbalanced voltage Swell & Sag is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage Swell from the duration 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown fig-3(c). Using DVR load Current is compensated due to unbalanced voltage Swell & Sag. The compensated load Swell current from the duration 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown fig-3(d).The corresponding DVR injected voltage, for the disturbances of voltage Swell & Sag as shown in fig-3(e). Its corresponding DC link voltage wave forms are shown in fig-3(f).



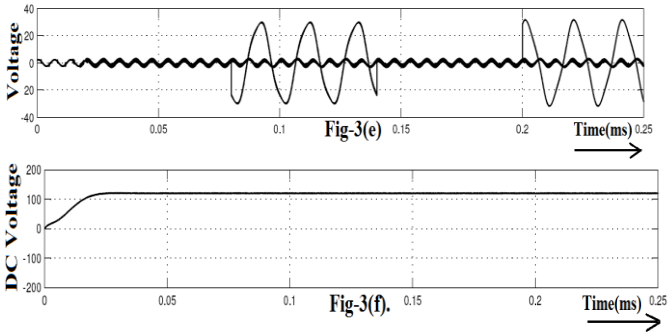
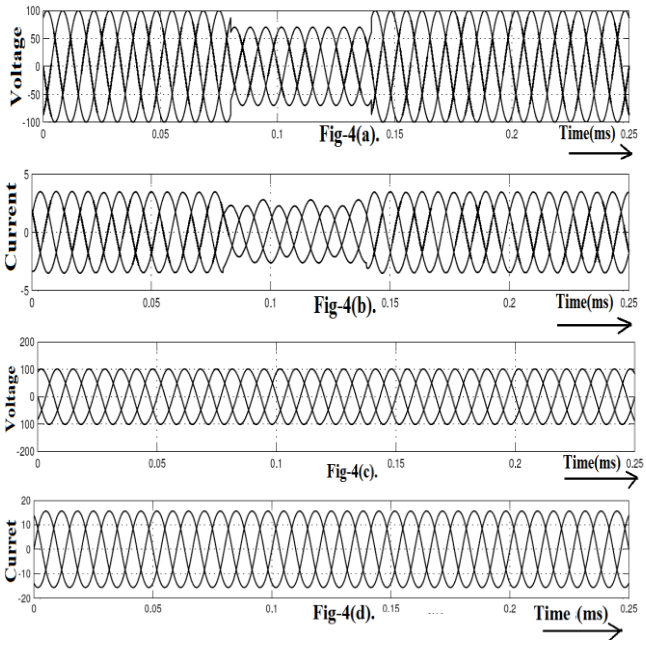


Fig-3(a) unbalanced voltage Swell & Sag at the source side, Fig.-3(b).Unbalanced Swell & Sag current at the source side, Fig- 3(c). Compensated Load voltage, Fig. 3(d) Compensated load current, Fig-3(e).DVR Injected voltage during compensation, Fig-3(f).Dc voltage across super capacitor.

CASE-d: Three Phase Balanced Voltage Sag

The balanced voltage sag disturbance at source side causes 30% of voltage sag on phase -A. Due to this, the phase -A voltage is 30% smaller than from phase -B and phase-C voltages. The balanced Voltage sag is occurred from 0.08m sec to 0.14m sec as shown in fig-4(a). This balanced sag causes 30% of Sag disturbance in source current wave form from 0.08m sec to 0.14m sec as shown in fig-4(b). This balanced sag also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to balanced voltage sag is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage from the duration 0.08m sec to 0.14m sec is as shown in fig-4(c). Using DVR load Current is compensated due to balanced Sag. The compensated load current from the duration 0.08m sec to 0.14m sec is as shown in fig-4(d).The corresponding DVR injected voltage, for the disturbances of voltage sag as shown in fig-4(e). Its corresponding DC link voltage wave forms are shown in fig-4(f).



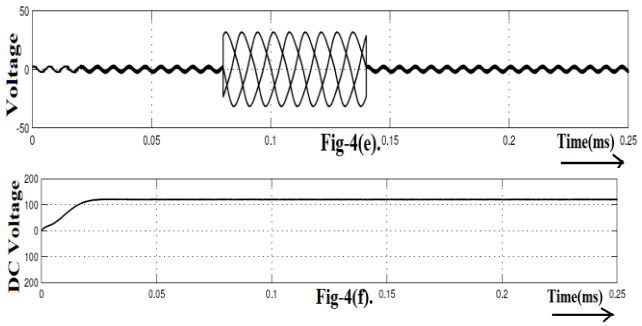
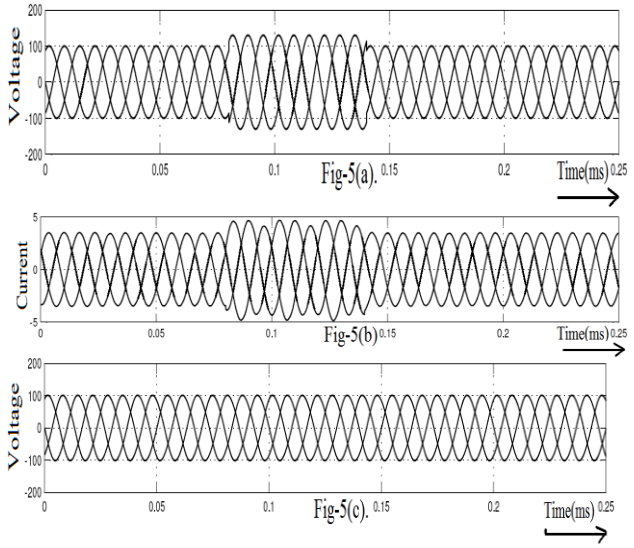


Fig-4(a). Balanced voltage sag at the Source side, Fig-4(b).Balanced Sag current at the Source side, Fig-4(c).Compensated load voltage, Fig-4(d).Compensated load current, Fig-4(e).DVR Injected voltage during compensation, Fig-4(f). DC voltage across super capacitor

CASE-e: Three Phase Balanced Voltage Swell

The balanced voltage Swell disturbance at source side causes 30% of voltage Swell on phase -A. due to this, the phase -A voltage is 30% more than from phase -B and phase-C voltages. The balanced Voltage Swell is occurred from 0.08m sec to 0.14m sec as shown in fig-5(a). This balanced Swell causes 30% of disturbance in source current wave form from 0.08m sec to 0.14m sec as shown in fig-5(b). This balanced Swell also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to balanced voltage Swell is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage from the duration 0.08m sec to 0.14m sec is as shown in fig-5(c). Using DVR load Current is compensated due to balanced Swell. The compensated load current from the duration 0.08m sec to 0.14m sec is as shown in fig-5(d).The corresponding DVR injected voltage, for the disturbances of voltage Swell as shown in fig-5(e). Its corresponding DC link voltage wave forms are shown in fig-5(f).



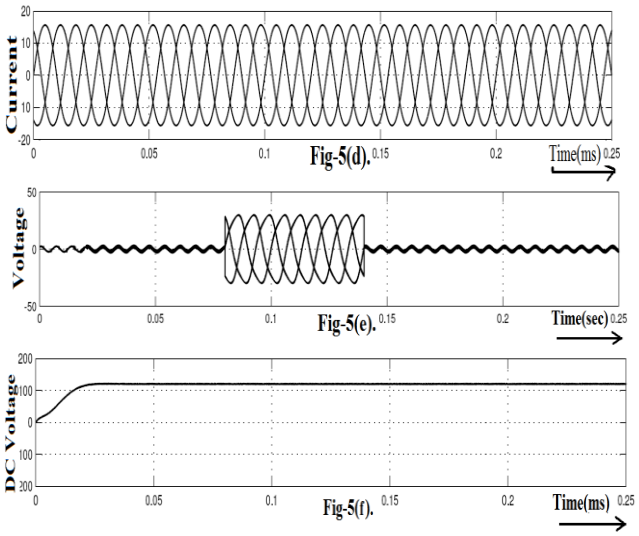
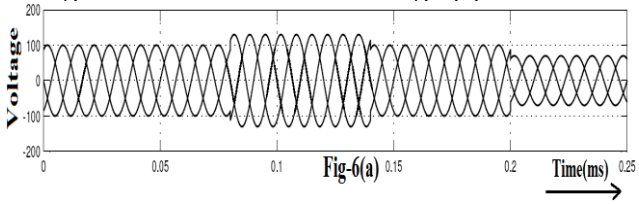


Fig-5(a).Balanced voltage Swell at the Source side, Fig-5(b). Balanced voltage Swell Current at the Source side, Fig-5(c).Compensated load voltage, Fig-5(d).Compensated load current, Fig-5(e).DVR Injection voltage during compensation, Fig. 5(f) DC link voltage across super capacitor.

CASE-f: Three Phase Balanced Voltage Swell & Sag

The balanced voltage Swell & Sag disturbance at source side causes the 30% of voltage Sag & Swell magnitude on phase –A, due to this the phase -A, voltage magnitude is 30% smaller during sag, more in the swell compared to the phase -B and phase-C. The balanced voltage Swell is occurred from 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown fig-6(a). This balanced Swell & Sag causes 30% Swell disturbance in source current wave form from 0.08m sec to 0.14m sec and 30% Sag disturbance in source current wave form from 0.2m sec to 0.25m sec as shown in fig-6(b). This balanced Swell & Sag also causes disturbance in load voltage and current wave form. Using DVR the disturbance due to balanced voltage Swell & Sag is compensated to nearly almost equal to sinusoidal wave form. The compensated load voltage Swell from the duration 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown fig-6(c). Using DVR load Current is compensated. The compensated Swell load current from the duration 0.08m sec to 0.14m sec and Sag from 0.2m sec to 0.25m sec as shown. Fig-6(d).The corresponding DVR injected voltage, for the disturbances of voltage Swell & Sag as shown in fig-6(e). Its corresponding DC link voltage wave forms are shown in fig-6(f).



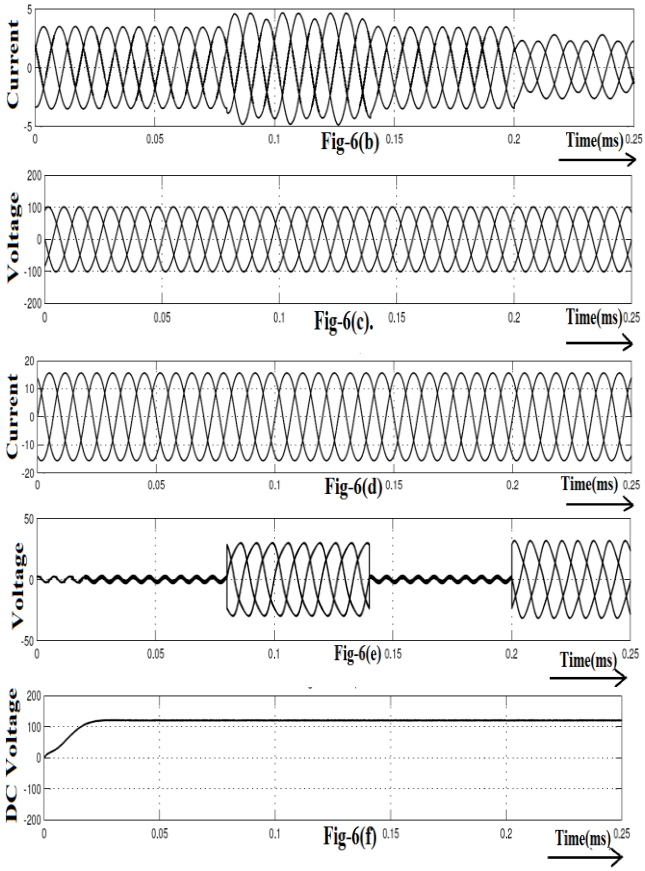


Fig-6(a).Balanced voltage Swell & Sag in the Source voltage, Fig-6(b).Balanced voltage Swell & Sag current at the source side, Fig-6(c).Compensated Load voltage, Fig-6(d).Compensated Load Current, Fig-6(e). DVR Injection voltage during compensation, Fig-6(f). DC link voltage across super capacitor.

CASE-7: THD (Total harmonic distortion) with out and with capacitor on High voltage side of transformer

The Low order harmonic currents are eliminated on low voltage of injection transformer. But the higher order harmonic currents are developed and appeared across the high voltage side of the injection transformer. The higher order harmonic current causes harmonics in the output current wave form. These harmonic currents are eliminated by placing a capacitor on high voltage side of injection transformer. It's corresponding total harmonics distortion (THD) with and without capacitor on high voltage of injection transformer for balanced/unbalanced voltage sag and swell conditions are shown in Fig-7(a)-7(l).

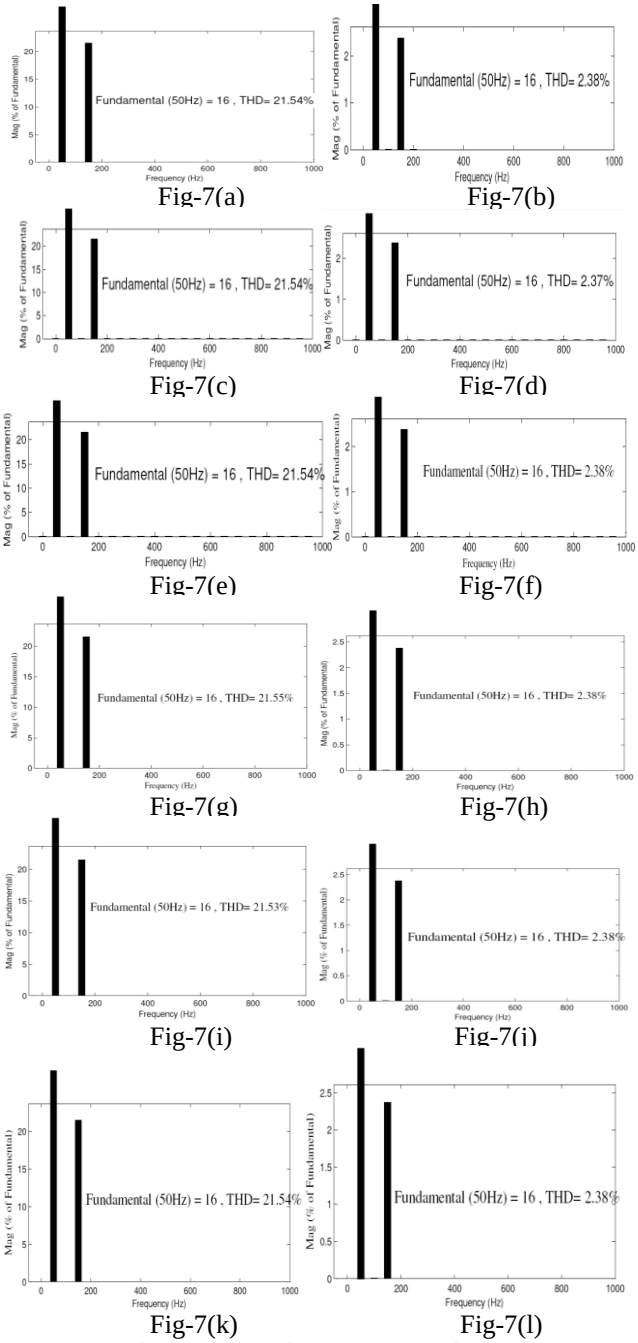


Fig-7(a).Unbalanced voltage Sag without capacitor THD analysis, 7(b). Unbalanced voltage sag with capacitor THD analysis, 7(c).Unbalanced voltage Swell without capacitor THD analysis, 7(d). Unbalanced voltage Swell with capacitor THD analysis, (e).Unbalanced voltage Swell & Sag without capacitor THD analysis, 7(f).Unbalanced voltage Swell & Sag with capacitor THD analysis, Fig-7(a).Balanced voltage Sag without capacitor THD analysis, 7(b).Balanced voltage sag with capacitor THD analysis, 7(c).Balanced voltage Swell without capacitor THD analysis, 7(d).Balanced voltage Swell with capacitor THD analysis, (e).Balanced voltage Swell & Sag without capacitor THD analysis, 7(f). Balanced voltage Swell & Sag with capacitor THD analysis.

The Total Harmonics Distortion (THD)

without capacitor filter is about 21.54%. When the capacitors filter are placed at the high level side THD value decreases to 2.38% is shown in Fig.7 (b). Thus the harmonics current are reduced from 21.54% to 2.38.

VI.CONCLUSIONS

This system is capable to compensate of voltage disturbances at low voltage distribution system. The implementation of super capacitor as an energy storage is to supply real power to the inverter during disturbances thus compensating the balanced/ unbalanced voltage sag and swell in the distribution system. The simulation results show that the performance of the DVR and the implementation of the super capacitor as energy storage are satisfactory in compensation of disturbances in the network such as balanced/ unbalanced voltage sag and swell in the distribution system and THD distortion also reduces. The effectiveness of proposed system is verified through simulation results.

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