# A COMPARATIVE ANALYSIS OF THE PERFORMANCE OF DYNAMIC VOLTAGE RESTORER BASED ON INVERTER TOPOLOGY AND CONTROL TECHNIQUE

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***Abstract:*** *Dynamic Voltage Restorer (DVR) is one of the custom power devices employed in distribution systems to mitigate power quality problems such as voltage sag and swell affecting critical loads. In the event of a voltage disturbance, the DVR injects a voltage in series with the line to maintain the voltage quality at the load terminals. Conventional DVRs are designed based on voltage source inverters and classical control theory. They lack fast dynamic response and require a large rating energy source to mitigate deep voltage sags of longer duration. To overcome this limitation, the design and development of a DVR based on a quasi impedance (Z) source inverter and associated control is being proposed. A Quasi Z source inverter ensures a constant dc link voltage during the voltage compensation in a DVR with reduced energy storage. A sliding mode controller implemented here does not depend on accurate system model and is capable of compensating any variations in the source voltage with good dynamic response. The efficacy of the proposed system is established against the conventional DVR system through simulation studies and validated with an experimental model.*

***Key Words:*** *Dynamic Voltage Restorer (DVR), EnergyStorage, Power quality, Quasi Z source inverters, Sliding mode control*

## I. Introduction

Voltage disturbances are common and undesirable power quality phenomenon in the distribution system which put sensitive loads under high risk. Loads such as medical equipment, factory automations, and manufacturing units of semiconductor-devices, are vulnerable to power-supply disturbances [1-3] and incur huge operational and production losses. Major voltage disturbances such as voltage sags and voltage swells occur due to short circuits in upstream power transmission line or parallel power distribution line connected to the point of common coupling (PCC), inrush currents involved with the starting of large machines, sudden changes of load, energizing of transformers or switching operations in the grid . According to the IEEE 1159-2009 standard, voltage sag is defined as a decrease in magnitude of 0.1to 0.9 p.u. in the RMS voltage at system frequency and with a duration of half a cycle to 1 min [3-4]. A dynamic Voltage Restorer (DVR) is a custom power device which restores the quality of voltage at the load side terminals when the voltage quality at the supply side is affected [5-7].

The DVR injects compensating voltage through a series transformer connected to the line. The energy required for the compensation is drawn from the line or from any other energy source or from a lead acid battery [5-8]. Though fast switching compact IGBTs reduces the size of the inverter, energy storage element and series transformer are bulky, heavy and costly.

Conventional controllers used in DVR require accurate, linear mathematical models and their performance suffer from parameter variations [5-8]. A conventional DVR based on PI controllers and sag detecting circuits are reported in literature [8]. Sliding mode controllers alleviate the need for accurate mathematical models. They, with the knowledge of parameter variation range to ensure stability and satisfactory reaching conditions, perform better in nonlinear systems [9-14]. As the converters are highly variable structure, apart from simple implementation, sliding mode controllers

provide stable and robust operation even for large variation in the supply and load side parameters and exhibit fast dynamic response.

Pulse width modulated (PWM) Voltage source inverters (VSI) are the main power electronic component of a conventional DVR. They require a large dc voltage source as the input source to the VSI [5-8]. A new class of power converters called Z source and quasi Z source converters with reduced component usage, simple control strategies and buck boost capabilities are reported in literature [16] and they find acceptability in renewable energy systems and adjustable speed drives [17-18].

This paper presents the improved efficacy of a DVR with quasi Z source inverter and sliding mode controller in comparison with a conventional DVR. The control strategy used here eliminates the need for separate circuits for sag/swell detection which are reported by authors [15]. This improves the dynamic response of the DVR. The PWM controlled quasi Z source inverter with its buck boost action, reduces the need for large battery storage for compensation of voltage variations of high magnitudes. Thus the proposed DVR is capable of providing compensation for any variation in the supply voltage with an energy storage of lower rating. The validity of the proposed DVR is verified with simulation and a prototype experimental model.

## 2. Design Methodologies of the Proposed DVR

A schematic diagram of the proposed dynamic voltage restorer installed in series with a sensitive load is shown in Fig.1. This single phase DVR consists of a Quasi Z source inverter fed from a battery, a passive filter, an injection transformer, and a sliding mode controller to regulate the inverter output voltage. Pre sag compensation [7] is used in this system.

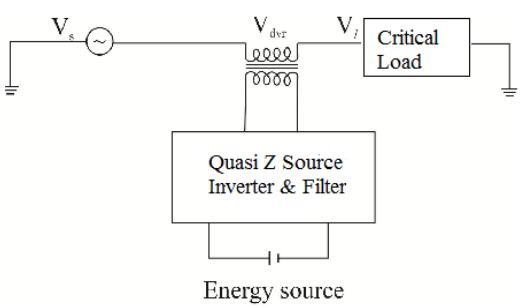


Fig 1. Structure of the proposed DVR

This compensation technique is implemented using a PLL(Phase locked Loop) synchronized with load voltage and a sliding mode controller.

### *2.1 Operation of the Quasi Z source inverter:*

The circuit topology of the Quasi Z source inverter is shown in Fig 2. The most important feature of this inverter compared to conventional voltage source inverter is the introduction of shoot through states along with the normal active states. During the shoot through states, either both switches of the same leg or all the four switches of the inverter are turned on simultaneously, leading the output voltage of the inverter to be zero. This feature enhances the capability of the inverter to act as a voltage boosting circuit.

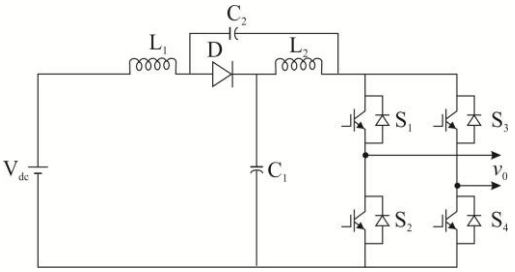


Fig 2. Single phase Quasi Z source inverter

The operation of Quasi Z source inverter is well discussed in literature. A brief analysis relevant to the application in a DVR follows. In a switching cycle with period T, if $T_0$ is considered as the shoot through period, the remaining duration $T_1$ is the active state of the inverter.

Thus $T = T_0 + T_1$ (1)

The shoot through duty ratio $D = \frac{T_0}{T}$ (2)

Equivalent circuits of the Quasi Z source inverter during shoot through states and active states are given in Figure 3 and Figure 4 respectively.

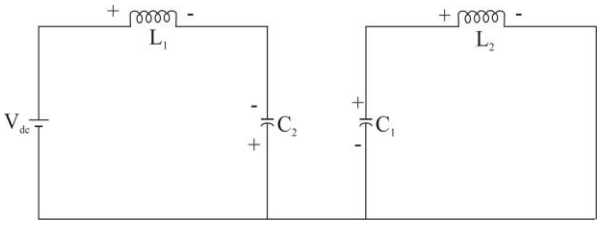


Fig 3. Equivalent circuit during shoot through state

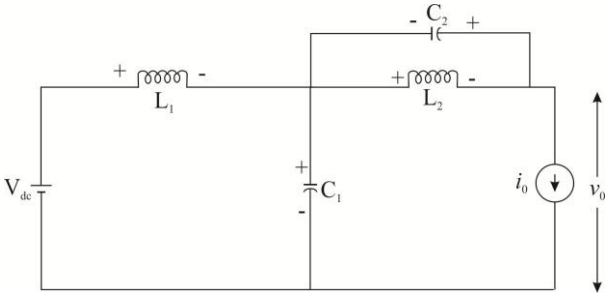


Fig 4. Equivalent circuit during active state

During shoot through the state, voltage across the inductor $L_1$ and $L_2$ are such that

$$v_{L1} = V_{dc} + V_{c_2} \quad (3)$$

$$v_{L2} = V_{c_1} \quad (4)$$

And the output voltage, $v_0 = 0$

During active state, $v_{L1}$ & $v_{L2}$ are found as

$$v_{L1} = V_{dc} - V_{c_1} \quad (5)$$

$$v_{L2} = -V_{c_2} \quad (6)$$

$$v_0 = V_{c_1} + V_{c_2} \quad (7)$$

During steady state, the average voltage across the inductors is zero and the capacitor voltages are

$$V_{c_1} = \frac{V_{dc}(1-D)}{1-2D} \quad (8)$$

$$V_{c_2} = \frac{V_{dc}D}{1-2D} \quad (9)$$

The peak dc link voltage is given as

$$\hat{v}_0 = \frac{V_{dc}}{1-2D} = BV_{dc} \quad (10)$$

where B is the boost factor, $\frac{\hat{v}_0}{V_{dc}} = B \geq 1$

The peak of the output phase voltage from the inverter can be expressed as

$\hat{V}_{ac} = M\frac{\hat{v}_0}{2}$ and thus $\hat{V}_{ac} = MB\frac{V_{dc}}{2}$, where M is the modulation index.

Compared to the traditional VSI, with the well known relationship $\hat{V}_{ac} = M\frac{V_{dc}}{2}$, the output voltage of quasi Z source inverter can be stepped up or down by selecting appropriate boost factor B.

*2.2 Design of the sliding mode controller:*

The schematic block diagram of the proposed DVR is shown in Figure 5. It mainly consists of reference voltage calculator, sliding mode controller, DC voltage source, quasi Z source converter and LC filter. Output of LC filter is connected to the system through a transformer. This section develops a model for the design of sliding mode controller for DVR. Sliding mode controllers are discussed in literature to control voltage source inverters in custom power devices [13-14]. The application of the controller with a Quasi Z source inverter in simple boost control mode for a DVR is designed and developed in this paper. Design of the controller for satisfactory operation involves the following tasks.

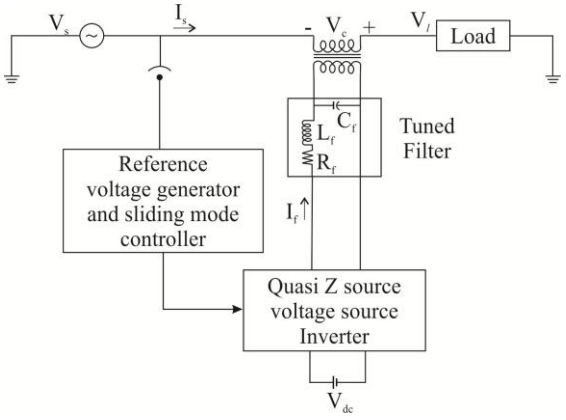


Fig 5. The proposed DVR block diagram

i.Sliding surface selection
ii.Checking for the existence of sliding mode
iii.Checking the reaching condition and
iv.Determination of the control law

The state space model of DVR with reference to Fig. 6 can be written as

$$\frac{d}{dt}\begin{bmatrix} v_c \\ i_f \end{bmatrix} = \begin{bmatrix} 0 & 1/C_f \\ -1/L_f & -R_f/L_f \end{bmatrix}\begin{bmatrix} v_c \\ i_f \end{bmatrix} + \begin{bmatrix} -1/C_f & 0 \\ 0 & -1/L_f \end{bmatrix}\begin{bmatrix} i_s \\ \delta(t)V_{dc} \end{bmatrix} \quad (11)$$

where $i_f$ and $i_s$ are filter inductor current and source current respectively. $\delta(t)$ is the switching function of the inverter, which can be 1 or -1.

*2.2.1 Sliding surface selection:*

In order to control the output voltage of inverter, a suitable sliding surface which will directly be affected by the switching law, is required. From (11), it is seen that the first time derivative of the output $(dv_c/dt) = (i_f - i_s)/C_f = \theta$, does not explicitly contain the control output $\delta(t)V_{dc}$, therefore the second derivative must be calculated

$$\begin{bmatrix} \dot{v}_c \\ \dot{\theta} \end{bmatrix} = \begin{bmatrix} \dot{\theta} \\ \frac{-R_f}{L}\theta - \frac{1}{L_fC_f}v_c - \frac{R_f}{L_fC_f}i_s - \frac{1}{C_f}\frac{di_s}{dt} + \frac{1}{L_fC_f}\delta(t)V_{dc} \end{bmatrix} \quad (12)$$

The phase canonical form (12) shows that as the second derivative of the output variable depends on the control input $\delta(t)V_{dc}$, no further time derivative is required. Taking the tracking error as $e_{v_c} = v_c^{ref} - v_c$, a sliding surface $\rho(e_{v_c}, t)$, is chosen such that

$$\rho(e_{v_c}, t) = k_1 e_{v_c} + k_2 \frac{de_{v_c}}{dt} = 0 \quad (13)$$

Where the constants $k_1$ and $k_2$ are chosen so that a linear combination of the tracking error and it's derivative approaches zero. This is a surface in the error space and is called the sliding surface.

*2.2.2 Existence of sliding mode operation:*

The existence of the operation in sliding mode implies that $\rho(e_{v_c}, t) = 0$. Also, to stay in this regime, the control system should guarantee that $\dot{\rho}(e_{v_c}, t) = 0$. As both the conditions must co-exist, the switching law must ensure that

$$\rho(e_{v_c}, t)\dot{\rho}(e_{v_c}, t) < 0 \quad (14)$$

thus, satisfying the stability condition for the system in sliding mode.

The fulfillment of the above inequality ensures the convergence of the system trajectories to the sliding surface $\rho(e_{v_c}, t) = 0$, since in either of the following cases, the surface approaches zero.

a) If $\rho(e_{v_c}, t) > 0$ and the derivative $\dot{\rho}(e_{v_c}, t) = 0$, or

(b) If $\rho(e_{v_c}, t) < 0$ and $\dot{\rho}(e_{v_c}, t) > 0$, the tracking error will move towards the surface $\rho(e_{v_c}, t)$. As this shows that as $\rho(e_{v_c}, t)$ converges to zero, the trajectories in the system space are forced into the sliding surface and the condition (14) is called the sliding mode existence condition.

*2.2.3 Checking the reaching condition:*

The fulfillment of $\rho(e_{v_c},t)\dot{\rho}(e_{v_c},t)<0$ as $\rho(e_{v_c},t)\dot{\rho}(e_{v_c},t)=(1/2)\dot{\rho}^2(e_{v_c},t)$ implies that the system state always approaches the sliding surface.

### *2.2.4 Determination of the control law:*

After verifying the existence condition, the switching law for semiconductor switches can be devised as

$$\delta(t)=\begin{cases}1 & for \quad \rho(e_{v_c},t)>0\\ -1 & for \quad \rho(e_{v_c},t)<0\end{cases} \qquad (15)$$

In an ideal sliding mode controller, at infinite switching frequency, state trajectories are directed toward the sliding surface and move exactly along the discontinuity surface. Practical power converters cannot switch at infinite frequency, and this implementation involves a comparator with hysteresis 2ε, where switching occur at $\left|\rho(e_{v_c},t)\right|>\varepsilon$ . With this hysteresis comparator the switching law modifies to (16)

$$\delta(t)=\begin{cases}1 & for \quad \rho(e_{v_c},t)>\varepsilon\\ -1 & for \quad \rho(e_{v_c},t)<-\varepsilon\end{cases} \qquad (16)$$

Since the sliding surface and switching does not depend on system operating point, load, circuit parameters, power supply, and the converter dynamics, operating in sliding mode is robust.

## 3. Operation of the Proposed DVR

The control block diagram of the proposed DVR is shown in Fig.6. The reference voltage $V_{cref}$ to be injected by the DVR is obtained by subtracting the reference source voltage and actual source voltage. Using a phase locked loop (PLL) a sine template is generated, which is then multiplied with the peak of the supply reference voltage to obtain the reference supply voltage. The DVR injected actual voltage is then subtracted from the reference DVR voltage to obtain the error signal. This error signal is then processed by the sliding mode controller. The output of the sliding mode controller is the reference signal for the PWM generator of the inverter. Simple boost modulation technique is combined with the triangular carrier PWM technique to obtain the pulse trains for the Quasi Z source inverter to enable the shoot through stages. This equips the inverter to operate in boost mode also, thereby providing compensation for voltage sags with a reduced dc source.

## 4. Simulation Results and Experimental Validation

The system parameters used for the study are shown in table1. Simulation study was done on MATLAB SIMULINK environment. Table 1 shows the ratings of the system used for simulation and experimental study.

Table 1. Sytem parameters

| | | |
|---|---|---|
| Source Voltage | 120V | |
| Frequency | 50 Hz | |
| injection transformer | 1:1, 1KVA | |
| Load | 46Ω, 15mH | |
| DC source battery | 50V, 10Ah | |
| Inverter switching frequency | 10kHz | |
| Quasi Z source impedance | L | 400µH |
| | C | 500µF |
| Filter | R | 0.2Ω |
| | L | 2.5mH |
| | C | 20µF |
| Load Voltage | 120V | |

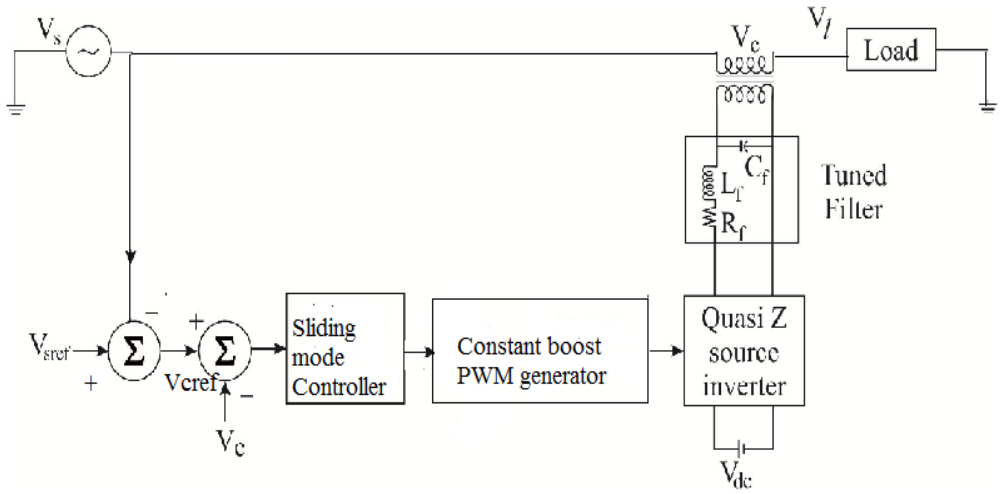


Fig 6. Control block diagram of the proposed DVR

Figure 7 depicts the source voltage, DVR injected voltage and load voltage respectively under voltage disturbance condition. The supply side voltage is generated by a programmable voltage source. The supply voltage is subjected to 16% sag from 0.05sec to 0.3sec. The rms value of the supply voltage is reduced to around 100V and the DVR responds by injecting an appropriate voltage magnitude at proper phase to maintain the voltage profile at the load end.

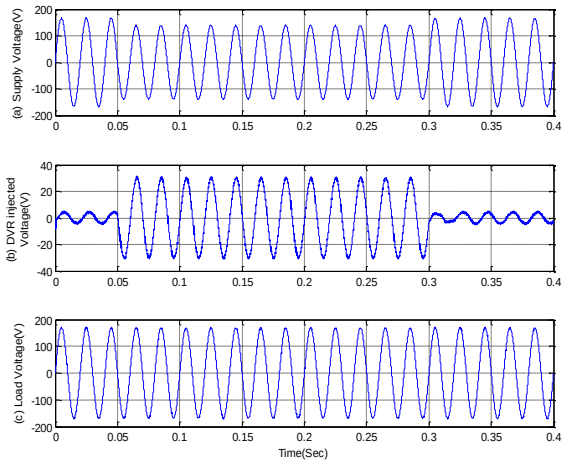


Fig 7. Simulation results for 16% voltage sag

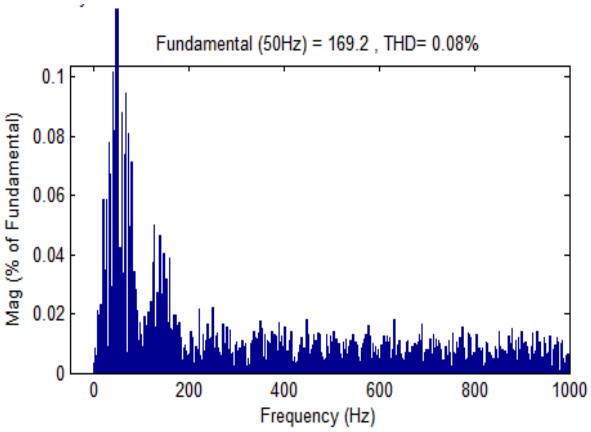


Fig 8. Harmonic spectrum of the load voltage at 16% sag

Figure 8 shows the total harmonic distortion (THD) in the load voltage for the entire duration of 0.4 sec. The rms value of the load voltage, 120 V is maintained with the peak value of around 169.5V. The total harmonic distortion in the load voltage with the injected voltage being a major part of it, is found to be only 0.12%.

Figures 9 & 10 show the voltage waveforms and the harmonic profile of the system respectively, when subjected to a voltage sag of 21% from 0.05 sec to 0.3 seconds. The injected

voltage of the DVR is in phase with the supply voltage and its magnitude is around 25V rms, so that the load voltage is maintained at 120V rms instantaneously with a THD of only 0.08%.

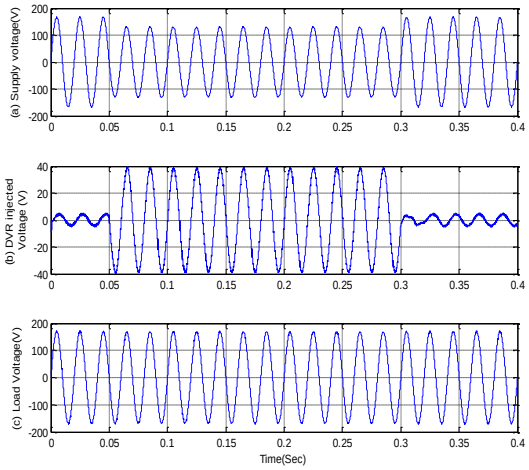


Fig 9. Simulation results for 21% voltage sag

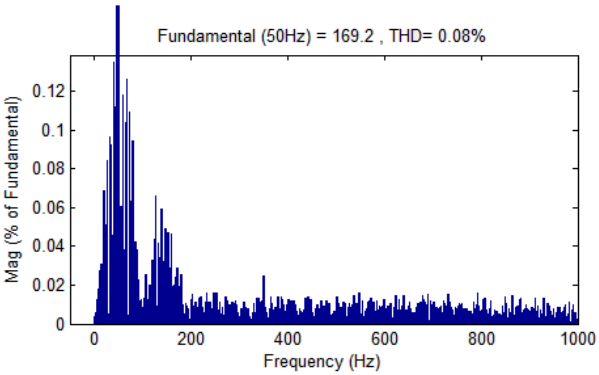


Fig 10. Harmonic spectrum of the load voltage at 21% sag

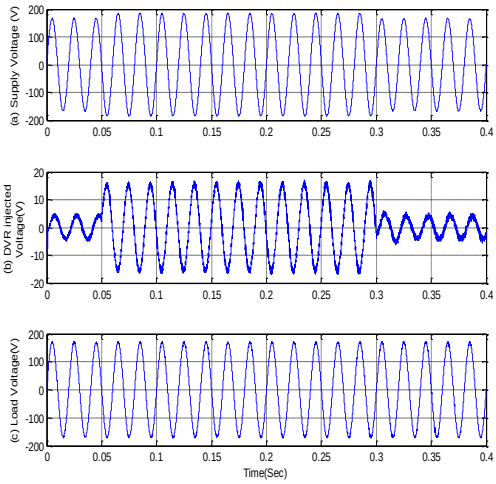


Fig 11. Simulation results for 11% voltage swell

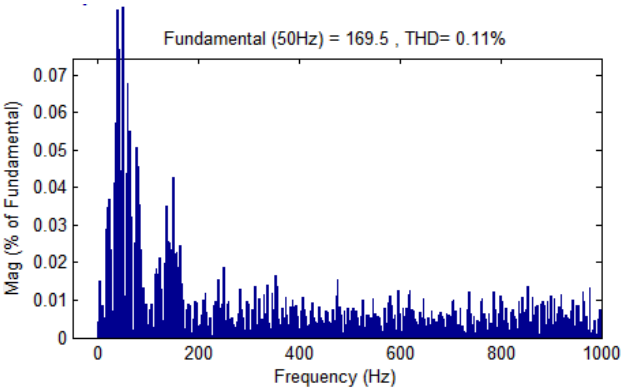


Fig 12. Harmonic spectrum of the load voltage at 11% swell

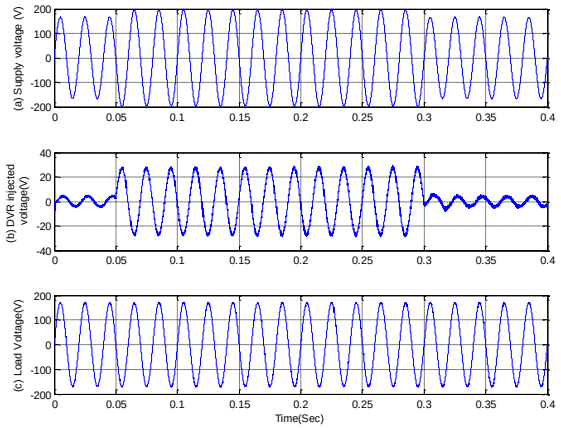


Fig 13. . Simulation results for 18% voltage swell

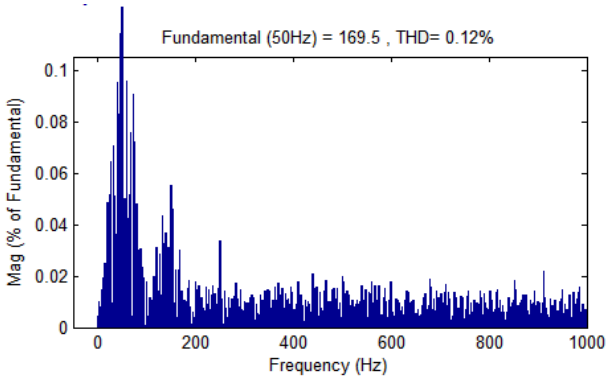


Fig 14. Harmonic spectrum of the load voltage at 18% swell

Investigations under voltage swell conditions were carried out by subjecting the supply voltage to raise to 11% above the rated value from 0.05 sec to 0.3 seconds. The results are shown in 3 plots given by Figure 11, where all voltage magnitudes are marked in Voltage. It can be seen that the DVR injects a voltage in phase opposition to the supply voltage, so that the load voltage profile is maintained at 120V rms throughout the swell duration. The THD content of the load voltage is only 0.11% as shown in Figure 12. Similar tests were carried out on the system to generate results when 18% swell appears in the supply voltage. The voltage waveforms and harmonic profile obtained are displayed in Figures 13 & 14 respectively.

Further, the system was subjected to a voltage sag of 25% from 0.05 sec to 0.2 sec and a voltage swell of 30% from 0.25 sec to 0.35 sec. The results of the simulation studies are given in Figure 15. The harmonic profile of the load voltage is shown in Figure 16. The instantaneous voltage restoration achieved by the DVR is evident from the simulation results.

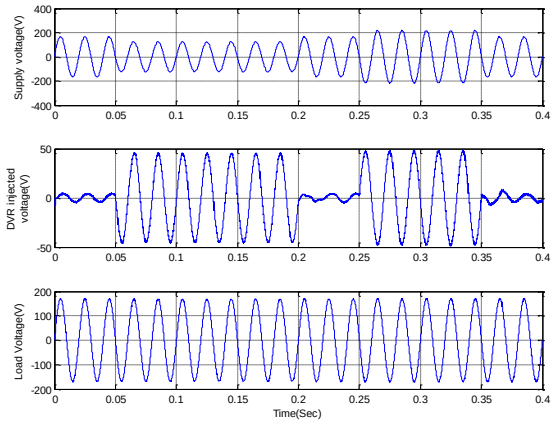


Fig 15. Simulation results for 25% sag and 30% swell

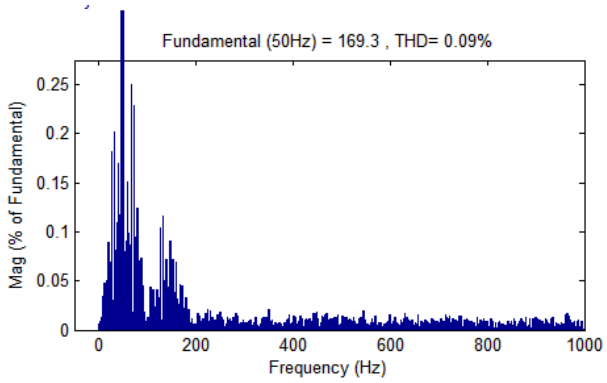


Fig 16. Harmonic spectrum of the load voltage

. Simulation studies were performed for various load condtions, load types and depth of voltage disturbances. Similar studies were performed on a conventional DVR, which uses a PI controller and voltage source inverter with a dc source of 250V, for comparison. Results of the comparative performance studies are summarized through Figures 17, 18 and Table 2. Figure 17 shows two graphs, with graph (a) for the proposed DVR and graph (b) for the conventional DVR, when the system voltage experiences 60% sag at varying load conditions. It shows that the voltage profile of the load voltage is maintained at rated value of 1pu for the proposed DVR, whereas the system with conventional DVR collapses as the load increases. Figure 18 depicts the comparative performance of the DVRs when the system is subjected to varying sag conditions at a fixed load of 5A. Here the proposed DVR performance shown by graph (a) is superior to that of the conventional one shown by graph (b), when the THD content in the load voltage is compared. Table 2 shows the performance comparison of the proposed DVR with the conventional one, for different types of loads, at 50% voltage sag and at 5A load current. The conventional one not only require large battery, but also the quality of the DVR injected voltage is poorer as indicated by the THD value of the load voltage. More importantly, the pu value of the load voltage approaches unity in case of the proposed one, while the conventional DVR supported load voltage is still subjected to 2% to 5% variation. This clearly shows the efficacy of the control and converter system of the proposed DVR.

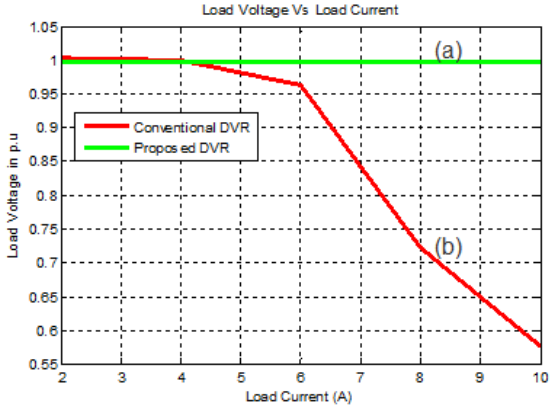


Fig 17. Comparison of load voltage profile for varying load currents at 60% sag, in the conventional and proposed DVR

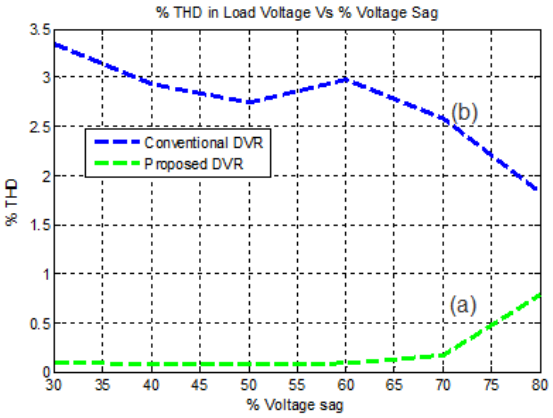


Fig 18. Comparison of the harmonic profile of the load voltage of the two DVRs at different sag conditions.

Table 2. Comparative Performance of the two DVRs with different types of loads

| Types of Load | Conventional DVR | | Proposed DVR | |
|---|---|---|---|---|
| | THD % | Load voltage (pu) | THD % | Load voltage (pu) |
| R Load | 2.75 | 0.988 | 0.07 | 0.9966 |
| RL Load | 4.81 | 0.9641 | 0.07 | 0.9966 |
| Nonlinear loading R type | 2.56 | 0.9886 | 0.07 | 0.9966 |
| Nonlinear loading RL type | 5.03 | 0.9543 | 0.12 | 0.9966 |

A prototype experimental set up of the proposed system is implemented using FPGA. The system voltage is 120V, and the connected load is an R-L type.The experimental platform for the control system of the DVR was built around SPARTAN 3ADSP, which comprises of MATLAB SIMULINK GUI for FPGA implementation (XC 3sd1800a-4fg676). Supply is given to the system using an autotransformer, through which voltage sags and swells are generated to the 120V R-L load. The experimental set up is shown in Figure 19.

The experimental observations for voltage sag and voltage swell conditions are discussed in the following section. The supply voltage, DVR injected voltage, and load voltages are measured by a Precision Power Analyzer (PPA). Figure 20 depicts the measured source voltage ($U_1$), injected DVR voltage ($U_5$) and load voltage ($U_6$), when a voltage sag of 16% is present in the source voltage, effected by the single phase auto transformer. Fig 21 shows the results when the supply is subjected to 21% sag. On comparison with the simulation results for a similar sag conditions, it is evident that the experimental results closely match with the simulation results. Experimental results of a voltage sag of 25% in the system is also given in Figure 22.

Figure 23 depicts the experimental results when a swell of 11% is present in the source voltage. The measured source voltage ($U_1$), injected DVR voltage ($U_5$) and load voltage ($U_6$) show that the DVR injects a voltage in phase opposition to the supply voltage so that the desired load voltage profile is maintained. Figures 24 & 25 give the experimental waveforms when the system is subjected to voltage swells of 18% and 25% respectively. Under 18% voltage swell, the system supply voltage is read by ($U_1$) as 141V rms, and the load voltage read by ($U_6$) as 121V, when the injected DVR voltage as read by ($U_5$) is 19.8V. Under 25% voltage swell, the supply voltage is 150V shown in ($U_1$), DVR injected voltage is 30.5V shown in ($U_5$) and the load voltage 119.7V ($U_6$) as per Figure 25. All the above experimental results closely match with the corresponding simulation results, within the limitations of the experimental set up.

Fig 19. Experimental set up

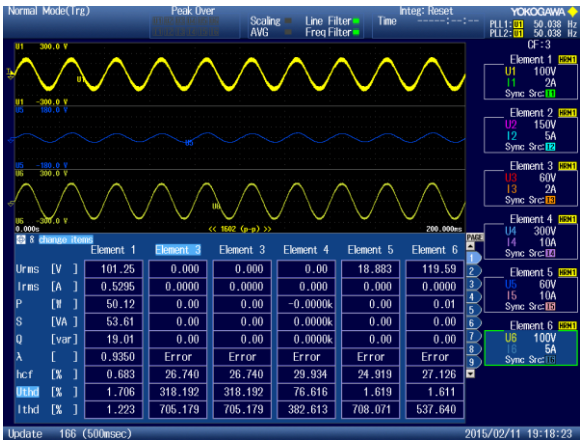


Fig 20. Experimental results for 16% voltage sag

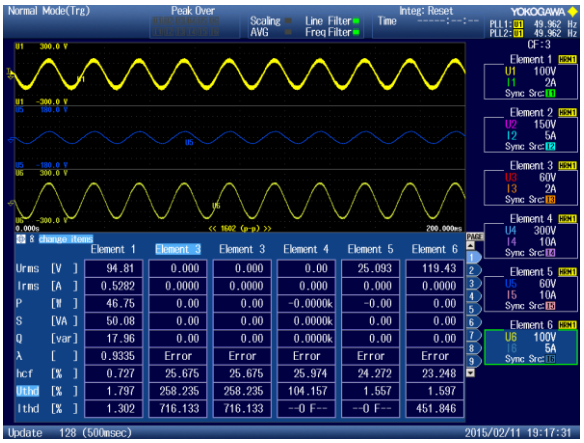


Fig 21. Experimental results for 21% voltage sag

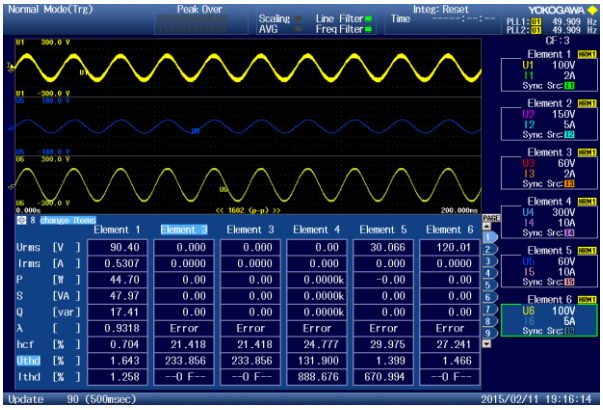


Fig 22. Experimental results for 25% voltage sag

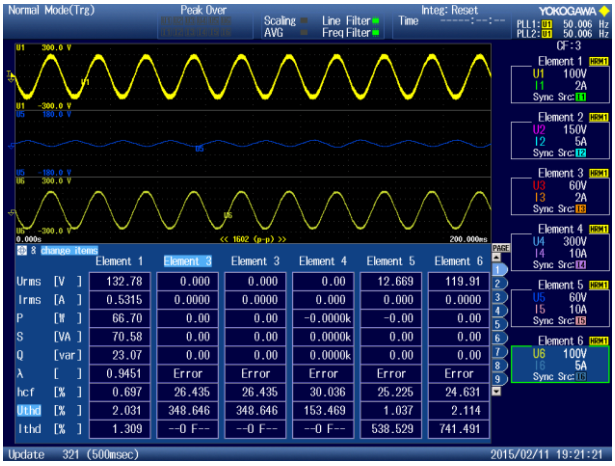


Fig 23. Experimental results for 11% voltage swell

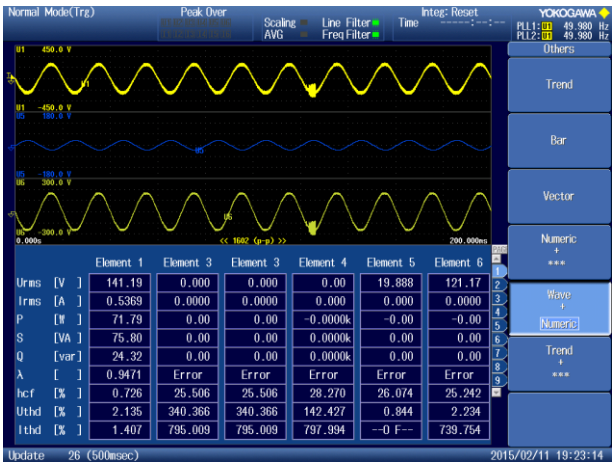


Fig 24. Experimental results for 18% voltage swell

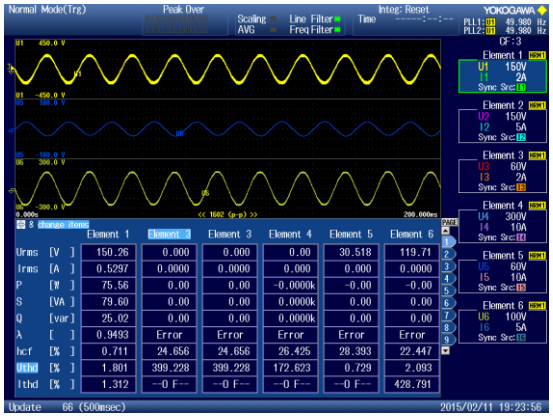


Fig.25. Experimental results for 25% voltage swell

## 5. Conclusions

This paper presents the design, development and performance validation of a single phase DVR based on a Quasi Z source inverter and the control system implementation using a sliding mode controller. The performance of the proposed DVR is compared with the conventional one which employs a voltage source inverter and a PI controller. Pre sag compensation technique is used here, which demands a large energy source to compensate for deep and prolonged voltage sags. The designed DVR is capable of injecting appropriate voltages even when the distribution system is subjected to deep voltage sags, without the need to have an energy source of higher rating. The Quasi Z source inverter with its ability to boost voltage with proper adjustment in the shoot through duty ratio, provides an avenue to implement the DVR capable of withstanding deep voltage sags of longer duration, with reduced energy storage. Here, sliding mode controller is successfully implemented, which gives good dynamic response during sag and swell conditions. It eliminates the need for a separate circuit for sag/swell detection as used in conventional DVRs. The efficacy of the proposed system was compared with the conventional DVR, against few key performance parameters. Validity of the entire system was tested on a laboratory model.

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