MODELLING AND EXPERIMENTATION OF MODIFIED CASCADED MULTILEVEL INVERTER WITH OPTIMIZED OUTPUT

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Abstract-- *Multilevel inverters are becoming more popular in the electrical sector owing to its high output voltage capability. This high output voltage depends upon the no. of levels used in the multilevel inverter which in turn points towards the no. of switches associated with the levels. As long as the levels are increased by virtue of increase in switches, the output voltage waveform tends to be purely sinusoidal. But as the level increases the switching pattern becomes more and more complex. This paper focuses on optimization of AC voltage output from a 15 level Cascaded Multilevel Inverter (CMLI). The proposed CMLI has been remodeled with only one Dc source, 2 capacitors and 4 switches for each bridge with an intention to obtain 15 level output with minimum power consumption and reduced switching losses. As minimum no. of switches are incorporated in the proposed system, the switching pattern can be framed flexible and facile, which can be further extended to n levels with better THD. The switches for the proposed CMLI are controlled through an organized pattern resulting in a near sinusoidal output with a maximum of 15 levels. The proposed system was simulated using MATLAB simulation software. The hardware fabrication of the simulated structure with the corresponding test results are discussed in this paper.*

Index Terms *- Cascaded Multilevel Inverter (CMLI); Pulse width pattern; Optimum output voltage.*

I. INTRODUCTION

With the increasing demand of electrical energy, multilevel inverters emerge as a boon to meet the high power demand of the electrical sector. Conventional single phase or three phase inverters convert DC voltage to 2 levels AC output voltage. These output voltages are not directly suitable for the consumers as the wave form obtained deviates widely from the required sinusoidal shape, which may pave the way for power quality issues. In order to overcome such issues, inverter structure was modified and higher levels were achieved with the increase in switches. Thus the voltage levels and power demand can be increased without involving any transformers for such conversions. These features resulted in the development of various multilevel topologies. Diode clamped MLI, fly back capacitor MLI and cascaded H bridge MLI inverters are the most common topologies [1] – [5]. Among all the conventional topologies Cascaded MLI emerged as more efficient overcoming all the drawbacks of other conventional techniques. The cascaded MLI proved to be much simpler [6] – [7] and modular but depends on the number of DC sources to power each bridge which resulted in increased cost for every increase in output voltage level. The harmonic content present in the AC voltage waveform can be highly reduced by increasing the voltage levels thereby matching the required wave pattern. In order to increase the voltage levels, no. of H bridge levels are increased further rising the input DC source owing to higher power consumption through batteries, DC cells etc. also driving to socio-economic issues. On the other hand increasing the no. of switches would result in more switching losses necessitating the provision for filter circuits making the structure complex. In addition, the structure requires driver circuits and protection circuits for each switch which further increases the system complexity. To overcome the issues of conventional method, MLI was designed with less number of switches.

In this design, each bridge had only 2 switches instead of 4 as in the conventional method. Due to this modification the control circuits and switching losses reduced to a greater extent. The waveforms

appeared to be symmetrical due to the automatic phase shift arrangement of the structure. But the circuit had a drawback when the level has to be increased, the structure becomes complicated and furthermore each bridge requires individual power supply. The drawback in conventional method was rectified on inclusion of capacitors in the cascaded MLI circuit [8] – [12] which was identified as a replacement of DC power sources. The circuit was modified with one DC source powering the top most level bridge and the other level bridges are supplied through the storage capacitors. The capacitors initiate voltage doubling in the circuit which results in higher voltage levels. Furthermore, current distortions can be minimized by operating the switches at zero current condition with the help of these capacitors. The major drawback of Switched capacitor method is that the structure requires auxiliary circuit to charge and discharge the capacitors. Moreover in the absence of freewheeling diode, there are possibilities of fault or harmonic currents affecting the switches. In addition, this structure becomes abstruse as the number of level increases. Another topology investigates in combining the diode clamped inverter to the H – bridge inverter circuit [8] which provides a series connection between the outputs. The voltage balancing of DC link capacitors [13 -19] was carried out by fixing the modulation index for a particular value of THD. But this topology can operated only for that particular modulation index becomes tedious if the no. of levels has to be increased.

In order to obtain an optimal waveform, the conventional CMLI is remodeled with reduced number of switches and their step angles are adjusted based on the factor that with capacitor switching there are many possible combinations of switching states. As the proposed topology uses one DC source, the power conversion circuits and the power consumption are very less. This topology suited for any kind of DC source like batteries, solar power etc. Circuit description, switching angle sequence and comparative outputs are discussed in the fore coming sections.

II. SYSTEM DESCRIPTION

The proposed cascaded multilevel inverter is remodeled for 15 level output voltage. The circuit consists of 3 H– Bridges as shown in Fig 2.1, which incorporates 4 switches in each of them. The proposed circuit is powered by one DC source for any number of levels that can be a battery, solar power etc. This feature eliminated the provision of individual DC source for each level as in the conventional topology. The other levels in the proposed topology are powered through the storage capacitors. Also, with the remodeled circuit of 3 bridges and a single DC source, it is possible to obtain up to 15 levels of output which comparatively provides good performance as the switching losses are very minimal. On the other hand, the circuit is not much expensive owing to the fact that the protection, control and filter circuits are limited.

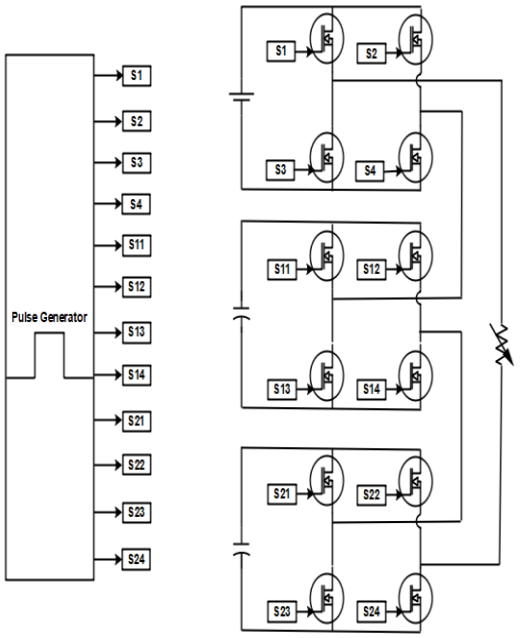

Fig. 2.1 Simulink block diagram of 15 level Cascaded Multilevel Inverter

Hence for a 15 level output, the proposed topology requires only 12 switches namely S1 to S4 for the first bridge, S11 to S41 for the second bridge and S12 to S42 for the third bridge along with a single DC source and 2 capacitors. Each switch is connected to an antiparallel diode for ensuring current by pass and safe operation. Due to the presence of capacitors it is easy to operate the switches in ON and OFF combinations to obtain a pure sinusoidal voltage.

In the proposed system, the pulse widths are modulated to obtain an optimum output voltage which matches the pure sinusoidal waveform thereby reducing the total harmonic distortion.

Table. 1. Organized Switching Pattern

MODES	SWITCHING STATES												VOLTAGE LEVELS
	S_1	S_2	S_3	S_4	S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}	
1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
2	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	Vdc/4
3	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	Vdc/2
4	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	3Vdc/4
5	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	Vdc
6	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	5Vdc/4
7	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	3Vdc/2
8	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	7Vdc/4
9	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	-Vdc/4
10	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	-Vdc/2
11	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-3Vdc/4
12	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	-Vdc
13	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	-5Vdc/4
14	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	-3Vdc/2
15	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-7Vdc/4

The switching patterns are organized to effectively utilize the switches within safe operation and to obtain optimum voltage level constantly matching the desired wave shape. The operation of the remodeled CMLI is explained through the switching pattern shown in Table 1. The operation of the proposed CMLI can be divided into 15 modes each providing a specific voltage level based on the switch turn ON and turn OFF conditions. Initial state starts with 0 level voltages which can be obtained by switching OFF all the switches. The output voltage can be measured between the two terminals as shown in Fig 2.1. From Mode 1 to Mode 8, the output traces the positive pulse pattern and hence the output voltage. On the other hand, Mode 9 to Mode 15 provides negative voltage sequence. In order to obtain 15 level output the voltage levels are divided as 0, Vdc/4, Vdc/2, 3Vdc/4, Vdc, 5Vdc/4, 3Vdc/2 and 7Vdc/4, the same pattern repeats for the negative sequence output. The switches are controlled in order to obtain the above sequence of levels. On the whole the pattern is organized such that for each mode minimum of 4 switches and maximum of 6 switches are fired. The proposed switching pattern reveals that the firing sequence is simpler and can be extended to any levels of output.

III. RESULTS AND DISCUSSION

The proposed system was simulated using MATLAB Simulink software for a 15 level output with an input voltage of 192 V. The results obtained in simulation was Vo = 355 V Vpp, THD =2.31%. The THD results thus obtained during simulation seemed to be appreciable and were within the safer limits. This model was further implemented as hardware with a result of Vo = 348 V Vpp and THD =2.29 %. This section gives a brief description on the simulation and hardware results. Pulse pattern and output waveforms obtained from both simulation and experimental set up are depicted below. The parameters were chosen with intense care in order to avoid the deviation between the simulated and hardware results.

A. Pulse Pattern:

Fig.3.1 a. shows the pulse pattern obtained from the hardware set up, for the switches that are to be used during the positive half cycle. The results shown in Fig. 3.1 b. portraits the positive pulse pattern obtained across switches with a magnitude of 1 V and time period of 20 ms using Matlab simulation software. The switches S1, S11, S12, S4, S41, and S42 are turned ON to get the positive voltage levels. The negative sequence pulses are shown in Fig. 3.2 a. which is in complementary to the positive sequence obtained across each switch. Fig.3.2 b. shows the pulse pattern obtained from PIC microcontroller for the switches that are to be used during the negative half cycle. The switches S2, S21, S22, S3, S31, and S32 are turned ON to get the negative voltage levels.

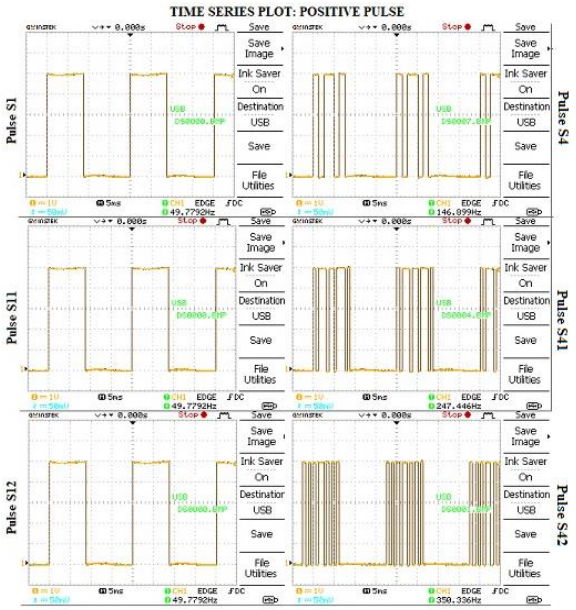

Fig. 3.1 a. Positive pulse pattern using PIC controller

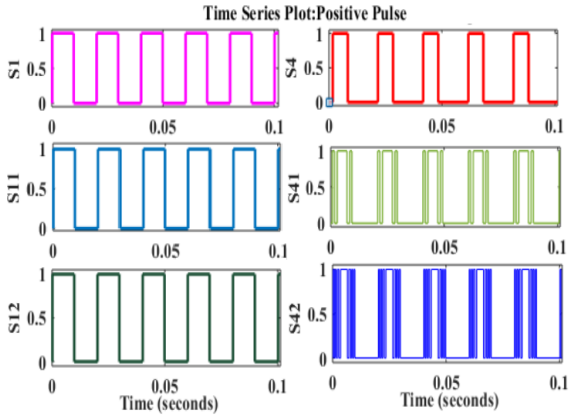

Fig. 3.1 b. Simulated Positive pulse pattern

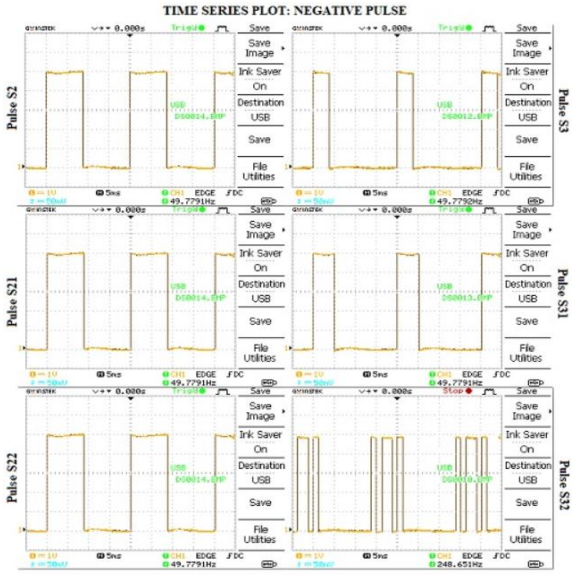

Fig. 3.2 a. Negative pulse pattern using PIC controller

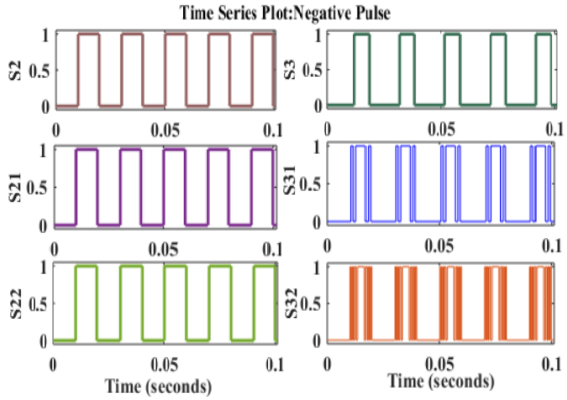

Fig. 3.2 b. Simulated Negative pulse pattern

B. Output waveforms:

The output waveform was nearly sinusoidal with a peak to peak voltage of 335 V, shown in Fig. 3.3. The output voltage waveform is compared with the reference sinusoidal voltage for clear perspective. The comparison is shown in Fig. 3.4 which clearly portraits that the deviation obtained from the modernized PWM technique are very minimal.

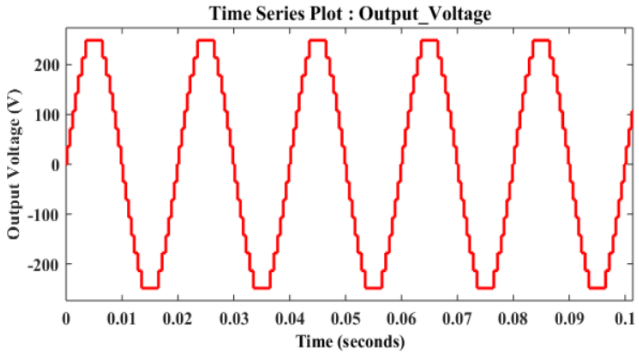

Fig. 3.3 Output voltage waveform

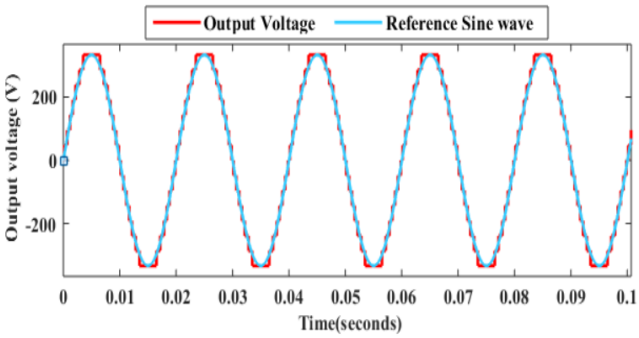

Fig. 3.4 Comparison between actual and the reference waveform

IV. HARDWARE RESULTS

Fig.4.1. shows hardware implementation of the 15level inverter with its corresponding output voltage waveform. The 3 h-bridges are connected back to

back like the cascaded multilevel topology. Two sets of pulses are generated, one for the positive half cycle and other one for negative half cycle. All these pulses are produced using modified PWM technique which is shown in fig.3.1a. and fig.3.2a. The hardware output shown in fig.4.1 has a peak output voltage of 348V at 50Hz frequency. From fig.4.2 we can clearly see that the voltage THD obtained is only 2.29%. Thus the proposed system with the modified PWM technique provides output with better THD. So the proposed system can be used where better performance is expected.

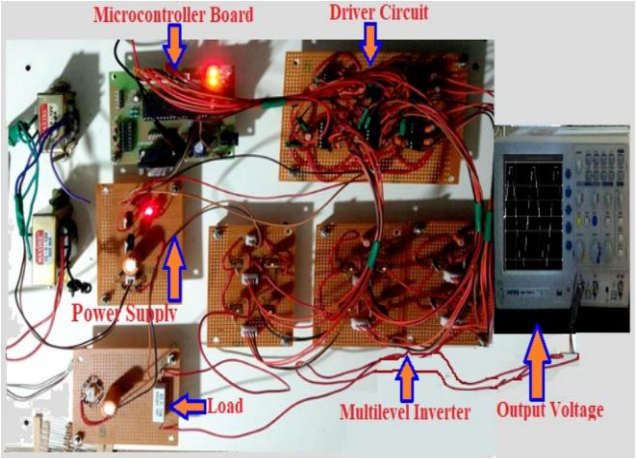

Fig. 4.1. Hardware Implementation of 15level inverter

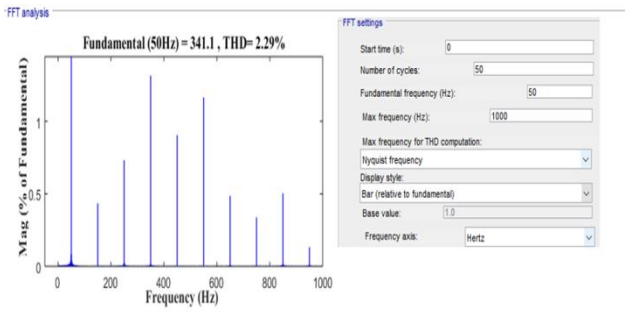

Fig. 4.2. FFT Analysis of modified cascaded MLI

V. CONCLUSION

The proposed CMLI was remodeled with only one Dc source, 2 capacitors and 4 switches I each bridge to obtain 15 level structures with minimum power consumption and reduced switching losses. As minimum no. of switches were incorporated in the proposed system, the switching pattern was simpler and the output was obtained with reduced switching losses [20] – [28]. The switches for the proposed CMLI were controlled through an organized pulse width pattern resulting in a near sinusoidal output with a maximum of 15 levels with a THD value of 2.29 % which was within the bench marks given as per the IEEE standards. Hence the optimization of AC output voltage was achieved through the proposed 15 level Cascaded Multilevel Inverter (CMLI). The proposed system can be further to n levels with better THD. This system best suits for medium and high power industrial applications [29] – [31]. Moreover, the proposed system requires a single DC source which further widens its application in the region of renewable energy sector thus providing harmonic free, green and clean energy.

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