Optimum Gate-Drive Solutions for Soft Switching IGBT Resonant Voltage Source Inverters

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***Abstract* – In static converters for induction heating, generally, resonant inverters are used. The commercially available IGBT devices are designed for hard-switching applications. Special gate drive techniques must be developed for soft switching conditions (zero voltage or zero current switching). In the paper gate drive solutions for soft switching IGBT inverters are investigated. Also short circuit active protection and parallel operation of inverter bridges are presented.**

***Index Terms* – IGBT, Resonant inverter, Soft switching, Short circuit, Parallel operation.**

I. Introduction

Soft switching is a major requirement for power IGBTs operating above a few tens of kHz, as switching losses become prevalent.. IGBT resonant voltage source inverters (RVSI) with operation frequency exceeding 100kHz have been designed for induction heating. Little data is available in the data sheets for device characteristics under soft switching conditions. In the RVSI specific soft-switching mode the IGBTs have unexpected behavior [3]: high turn-off power loss due to enhanced tail current bump, high forward voltage drop, conductivity modulation lag which causes dynamic voltage saturation during the turn-on process. During turn-off an elevated tail current bump was observed in the soft switching environment and was found to vary with output d*v*/d*t*.

A three-stage drive strategy for optimal turn-on of IGBTs in the RVSI specific soft-switching operation is presented in [7]. This paper describes gate drive solutions for enhanced turn-off process and the device's behavior under short circuit and parallel operation conditions. Simulations and experimental measurements in industrial environment have been considered in case of an RSVI designed for induction heating purposes. The output frequency of the inverter with a FZ400R12KS4 (EUPEC) IGBT module in each branch is 100 kHz.

II. IGBT Resonant Voltage Source Inverter Operation

RVSI converter is composed of a DC/DC converter and a resonant load inverter with full bridge topology (Fig. 1).

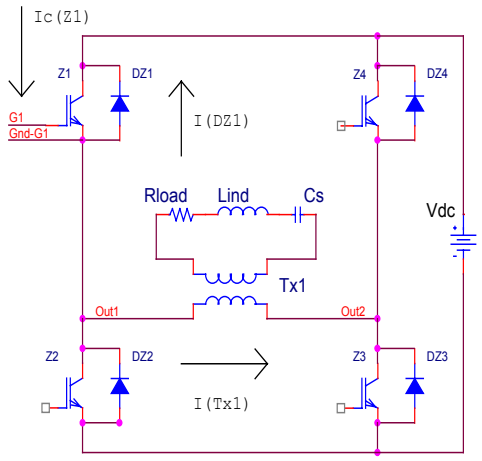

Fig.1. Resonant voltage source converter with IGBT modules (general diagram)

Each branch includes an IGBT module (IGBTs Z_1 to Z_4) with the appropriate reverse diode (DZ_1 to DZ_4). The DC source is a DC/DC converter, which represents a voltage source for the inverter, built with very low ESR filter capacitors.

The power regulation is solved by the DC/DC converter, while the inverter is controlled in a manner that allows high frequency, resonance operation, typical for the inverters used in induction heating plants.

The steady state operation is shown in Figure 2, based on a PSPICE simulation with IGBT modules previously mentioned. Transistors are turned off at small current level and turned on at zero voltage and zero current (Fig.2)

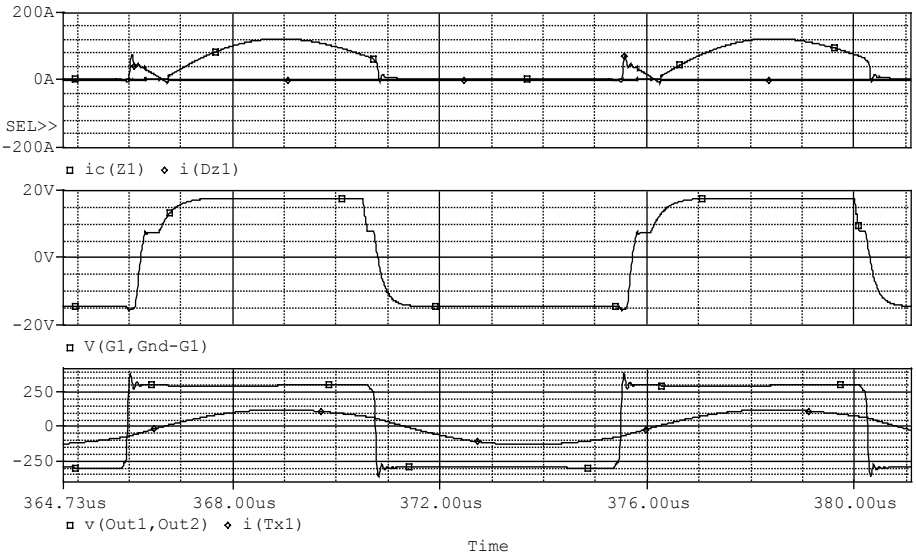

Fig. 2. Characteristic waveforms for RVSI: transistor and diode currents, gate voltage, output current and voltage (PSPICE simulation).

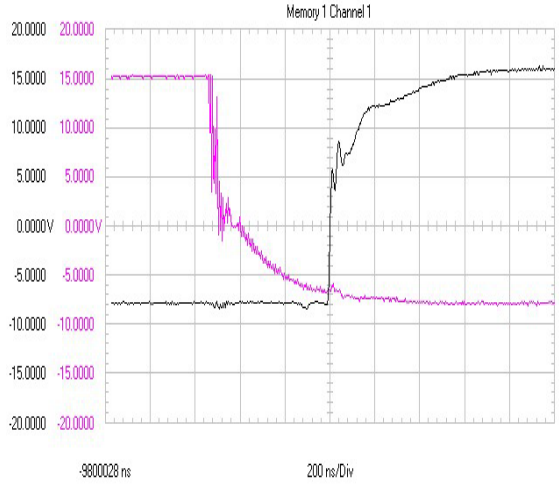

Fig. 3 a. Gate-emitter control voltage V_{GE} and collector-emitter voltage of an inverter leg

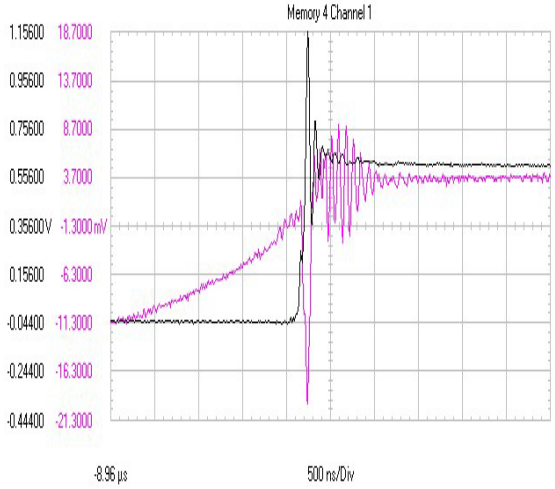

Fig. 3 b. Collector-emitter voltage and collector current of an inverter leg. Insufficient blanking time with associated over-voltage (1mV=2A)

The inverter load consists of a serial R,L,C resonant circuit, with about 100 kHz resonance frequency. The IGBTs are controlled in diagonal (Z_1 and Z_3, respectively Z_2 and Z_4 have identical drive signals). In nearly ideal operating conditions (see the PSPICE simulation of Fig. 2) the output voltage V_{G1}- V_{Gnd-G1} is slightly ahead of the load current I_{Tx1}. In these conditions, as the gate control is simulated only, no additional effects are shown.

The gate-emitter control signal (Fig.3,a) for an inverter leg shows that the turn-off of an IGBT precedes the turn-on of the device placed on the same leg. Under real operating conditions, a well designed drive system assures a soft switching of IGBTs.

If there is no sufficient blanking time, the switching voltage and current on the turning-on device has significant overshot (Fig. 3,b). Therefore it is necessary to develop a proper gate drive strategy, with practical solutions, to reduce or to avoid additional swings, current or voltage overshoots and, consequently, additional switching losses.

The measurements are performed on a VSRI converter of 100 kHz output frequency, , 60kW active output power, designed and built for induction heating purposes. The IBGTs modules are of type FZ400R12KS4 (EUPEC).

III. Optimum Gate-Drive Solutions For Soft-Switching Turn-Off In RVSI

An optimum three-stage active gate drive technique [4] has some basic characteristics (at the turn-off):

- Controlled over-voltage at turn-off;
- Reduced energy loss due to improved d*v*/d*t* characteristics at turn-off;
- Reduced delay time and total switching time at both turn-on and turn-off;

The steps for a three-stage turn-off are as follows:

Stage 1: At the beginning of the stage the gate-emitter capacitance is rapidly discharged till the gate voltage is just enough to support the collector current. At this point the collector voltage starts to rise and the gate voltage is clamped. To minimize the delay caused by the large value of the Miller capacitance at low collector-emitter voltages, a small gate resistor has to be used over this period. When the collector voltage reaches about 10 Volts the Miller capacitance reduces very much and the collector voltage increases steeply (start of the stage 2).

Stage 2: It lasts till the end of rapid fall of the collector current. At the beginning of this stage the collector voltage rises towards the DC bus voltage. When the collector voltage reaches the DC bus voltage the current starts to switch into the freewheeling diode. A large gate resistor should be used to limit the turn-off d*i*/d*t* and thus the collector voltage overshot

It is interesting to see that the turn-off delay is significantly affected by the *Rg* value , but the voltage rate of rise is not affected unless *Rg* is very large. The result is that active snubbing is not possible with limited variation of *Rg*. It was suggested in [1] that adding a gate-to-drain feedback capacitor with a series feedback resistor would allow d*v*/d*t* modulation for IGBTs.

It is shown in [1] that the anode voltage rate-of-fall at turn-on is influenced by much smaller gate resistances than those that influence the anode voltage rate-of-rise at turn-off. The gate drive requirements of the IGBT are inherently asymmetrical and the degree of asymmetry depends on the device base lifetime.

Stage 3: It lasts till the turn-on command. The gate voltage has to be driven to its final negative value. A small gate resistor should be used to drive the gate to the turn-off voltage rapidly. The small resistor also improves noise immunity during the off state of the IGBT.

For IGBTs in RVSI converter the turn-on is started at non-zero (but close to zero) collector current, which is decreasing fast in the vicinity of zero transition. In case of optimal switching, the end of current fall time means the end of voltage rise time. Even in snubberless operation, the ratio of switched current to transistor output capacitance is smaller at RVSl than at hard switching converters. Thus, zero voltage turn-off conditions appear and the turn-off losses are produced mainly by the presence of the tail current.

Under low d*v*/d*t* conditions, the turn-off current waveform shows a tail current “bump” in case of PT or “plateau” in case of NPT transistors due to inadequate charge removal from the drift-region (Fig. 4). Thus, a non-zero phase shift has to be provided with the commutation preceding the zero cross of the load current.

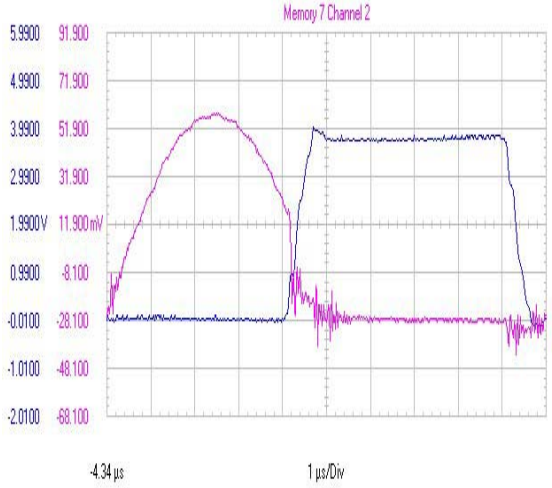

Fig. 4. Characteristic “tail plateau” at the FZ400R12KS4 device under zero voltage switching conditions: collector-emitter voltage V_{CE} and collector current I_C (1mV=2A)

Evolution of the gate voltage at high frequency soft switching in VRSI converter is significantly different from the case of hard switching, especially concerning the level, duration and possibility of interpretation of the Miller plateau (see Fig. 5 a,b and c)

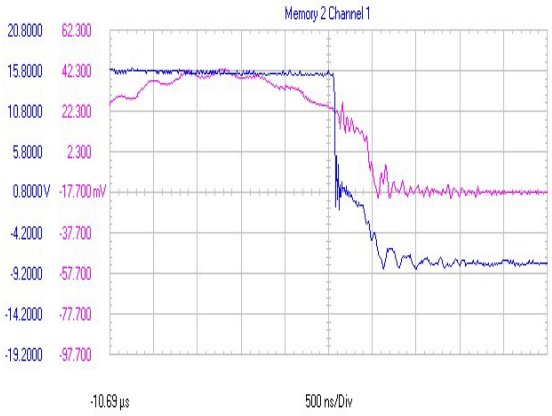

Fig. 5 a. Evolution of the gate-emitter voltage V_{GE} and IGBT collector current I_C i n case of RVSI soft switching, at turn-off

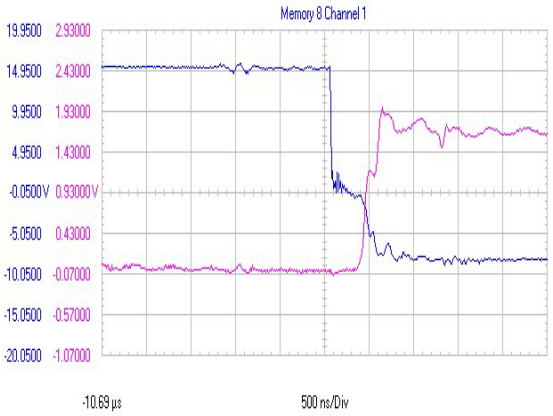

Fig. 5 b. Evolution of the gate-emitter voltage V_{GE} and collector-emitter voltage V_{CE} at soft torn-off

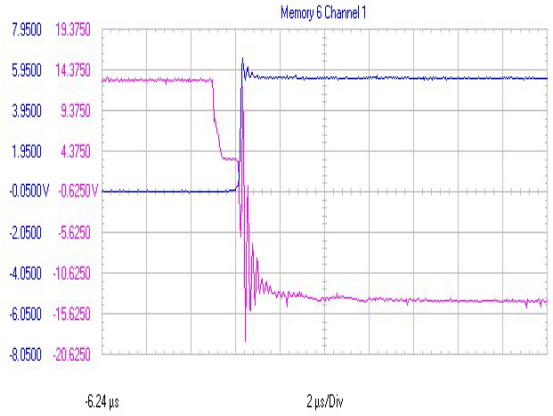

Fig. 5 c. Evolution of the gate-emitter voltage V_{GE},and collector-emitter voltage V_{CE} at hard turn-off

IV. Discussion Of The Adopted Active Short-Circuit Protection Strategy

Simultaneous conduction of both IGBT devices in an inverter leg (cross-over), is a condition also termed 'hard short-circuit' as no current amplitude and slope limitation exists on the DC side (low ESR capacitor tank).

Short-circuit withstanding capability of the IGBT is an important issue. Short-circuit withstanding time can be extended using a reduced gate drive voltage, but this is unpractical because of the increasing conduction losses. Delaying the short-circuit turn-off beyond the duration of the normal half-period (shorter than 5µs) in order to take advantage of the reduced carrier mobility of the MOS channel is also unpractical. It is better to limit the short-circuit current by fast protection much before it reaches its peak value. With a low-inductance layout this calls for reaction time shorter than 500ns, as di/dt can be higher than 5000A/µs (Fig.6.).

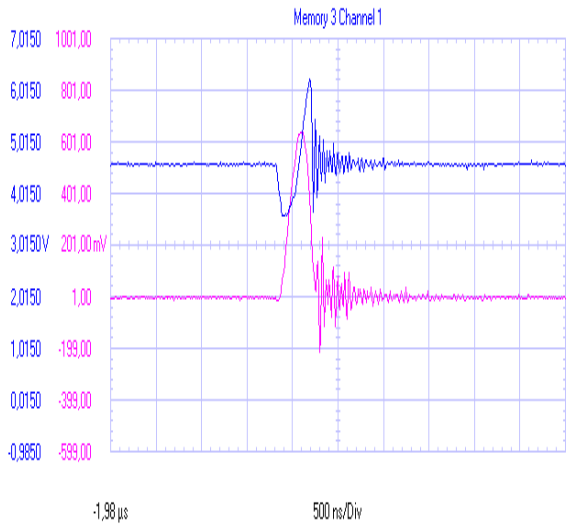

Fig. 6. Collector current I_C (1 mV = 2A) and collector-emitter voltage V_{CE} at hard short-circuit (V_{DC} = 465V, $I_C\hat{}$ = 1350 A, di/dt = 5400 A/µs, reaction time dt_didt = 250 ns)-

The active short-circuit protection is described as follows:

a. The *Desaturation* protection has been traditionally used along with a constant trip threshold. The initially discharged capacitor of an RC network is charged towards a constant voltage and simultaneously clamped by the falling collector-emitter voltage. Trip is triggered when the constant threshold is reached.

An other approach is to use a 'dynamic' trip value set by an RC network. The pre-charged capacitor is discharged beginning with the moment of transistor turn-on, the variation in time of the trip value approximately meets that of the falling collector-emitter voltage

A third approach is to use a delayed validation of the protection having a constant threshold. The delay time is specific for the application and the power device. This method can be further refined by defining a voltage profile decreasing in time, i.e. more trip levels associated with different delays.

In case of zero voltage turn-on in normal operation of the RVSI some differences from the case of hard switching can be observed and are described in [7].

The dynamic collector-emitter voltage spike, which appears at the zero travel of the current, is well above the trip level of the 'de-saturation' protection.

Thus, the resulting ' V_{CE} profile' to be expected is different from the hard-switching one and depends much on the converter operation. The protection has to be activated with a significant delay of 1.5-2 µs, loosing efficiency in limiting the short circuit current in case of 'hard short circuit'.

b. *di/dt* protection

High frequency operation requires reduction to minimum of switching losses. Operation above resonance frequency provides zero voltage turn-on, eliminating the diode recovery problem. Transient loss of this operating condition can result in EMC problems, over-voltage induced by diode snap-off and undesired increase of turn-on losses. Diode peak reverse recovery current depends on the current rate of rise through the power IGBT. Thus, di/dt has to be limited to handle both diode recovery problem and cross-over current due to insufficient blanking time between gating signals of the transistors from the same inverter leg. This blanking time has to be kept as small as possible for reasons explained above,

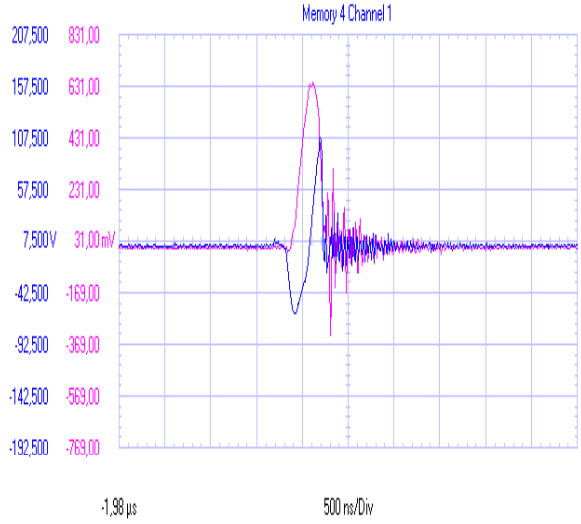

Fig. 7. Collector current I_C and gate-Kelvin emitter voltage V_{PE-E} at short-circuit for V_{PE-E} = 70V, di/dt = 5400 A/µs

tradeoff between stable operation and low losses becoming critical.

Measurement of di/dt becomes practical and efficient by means of the parasitic inductance between the power emitter and the Kelvin emitter of the module. This inductance has a value between 5-15 nH depending on the module.

Fig.7 shows the voltage drop on this parasitic inductance for the FZ400R12KS4 module along with the short-circuit current increasing with di/dt = 5400A/µs, allowing the extraction of the L_{E-PE} = 13 nH parameter.

V. Influence Of Gate Drive Performance On Operation Of Paralelled Inverter Bridges

Parallel operation of two RVSI IGBT-bridges has been studied. As we can expect, gate drive time or signal characteristic differences will cause electrical stress differences over the semiconductor devices. The bridges are connected in parallel through a stray inductance L_{sig}. The paralleled inverters' behavior has been investigated under gate drive differences. The investigations are performed by simulation and practical measurements, paralleling two identical inverter structures (shown in Fig.1) with identical IGBT modules.

Simulation results have shown that gate drive synchronism is the most critical from point of view of dynamic current sharing and more than 30% loss differences can appear between two similar transistors in case of 100 ns delay between the two gate signals (at the operation frequency of 100kHz).

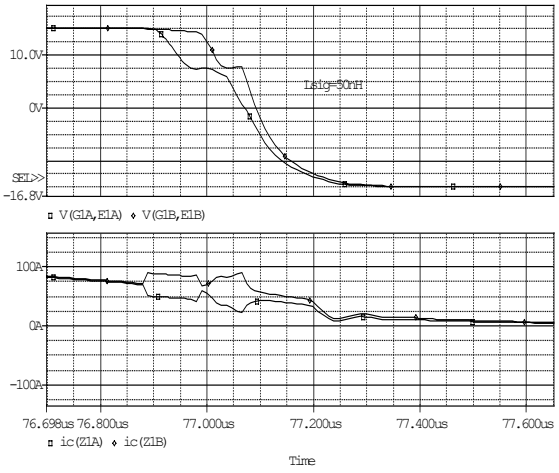

Fig. 8. Gate-emitter control voltages of the two identical placed transistors and emitter currents $I_{C\,Z1A}$, $I_{CZ1B,}$ in case of an asymmetry of 100 ns delay. Detailed representation of the transistor turn-off (the stray inductance is L_{sig} =50nH)- PSPICE simulation

For the given simulation, at 100 ns control signal delay the loss difference between similar IGBT transistors is of 150 W (fig. 8).

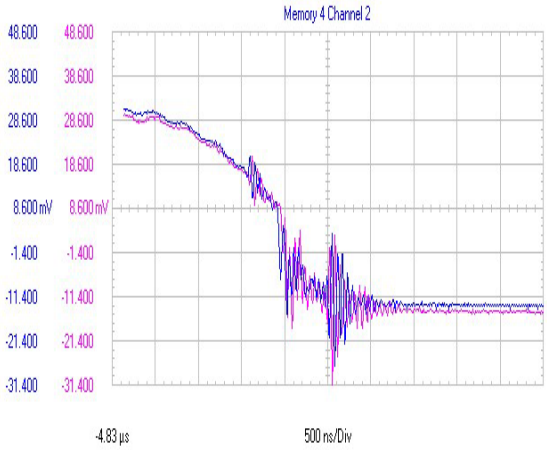

Fig. 9. Current sharing between similar modules at turn-off (2A/mV)

Practical measurements have shown a random delay of less than 30 ns (clock period of the signal processor

used in the control logic) between the two gate signals, resulting
in a good sharing of currents and switching losses (see Fig. 9)

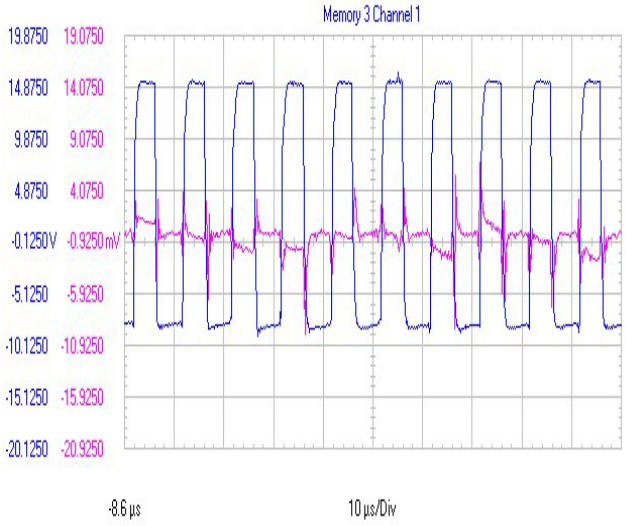

Fig. 10. Gate voltage and the difference between the module currents (2A/mV)

It is shown, that in the above mentioned conditions, when the random delay is less than 30 ns, the current differences (peak values in the vicinity of switching the IGBTs) are less than 15A, the differences during the full conduction period are less than 5A (the peak value of the sine wave current is about 150A)- see Fig.10.

VI. Conclusions

Features of gate drivers that support high frequency operation of IGBTs in resonant voltage source inverters have been presented. Requirements have to be met which are different from those in hard switching conditions. Characteristics of short-circuit protection are of major importance for inverter reliability

References

[1] A.R. Hefner Jr, "An Investigation of the Drive Circuit Requirements for the Power Insulated Gate Bipolar Transistor (IGBT)", *IEEE Trans. Power Electronics,* vol.6, pp208-219, Apr. 1991.

[2] R.Chokhawala, J.Catt and B.R.Pelly, "Gate Drive Considerations for IGBT Modules", *IEEE Trans. Ind. Aplicat*., vol.31, pp.603-611, May./June. 1995.

[3] I.Widjaja, A.Kurnia, K.Shenai, and D.M.Divan, "Switching Dynamics of IGBT's in Soft-switching Converters", *IEEE Trans. Electron Devices,* vol.42, pp 445-454, March 1995

[4] J.Vinod, B.S.Suh, and T.A.Lipo, "High-Performance Active Gate Drive fo High-Power IGBT's", *IEEE Trans. Ind. Aplicat*., vol.35, pp.1108-1117, Sept./Oct. 1999.

[5] A.Ammous, K.Ammous, H.Morel, B.Allard, D.Bergogne, F.Sellami and J.P.Chante "Electrothermal Modeling of IGBT's: Application to Short-circuit Conditions", *IEEE Trans. Power Electron.* ,vol.15, pp 778-790, July 2000.

[6] P.Hofer-Noser and N.Karrer, "Monitoring of Paralleled IGBT/Diode Modules", *IEEE Trans. Power Electron.* ,vol.14, pp 438-444, May 1999.

[7] A.Kelemen, S.Matyasi and I. Szekely, "IGBT Gate Drive Strategy for Soft Turn-on in Resonant Voltage Source Inverters for Induction Heating", *Bulletin of the Transilvania University of Brasov*, vol.9(44), Series A, pp 111-116, 2002