Modeling and Analysis of PFC with Appreciable Voltage Ripple to Achieve Fast Transient Response

Mr.R.Satish Kumar[*]
[*]*PG-Student, Department of Electrical and Electronics Engg.*
*RGMCET, Nandyal, India, E-*Mail: satishraguru@gmail.com.

Dr. D. Lenine[**]
[**] *Associate Professor, Department of Electrical and Electronics Engg.*
RGMCET, Nandyal, India, E-Mail: lenine.eee@gmail.com.

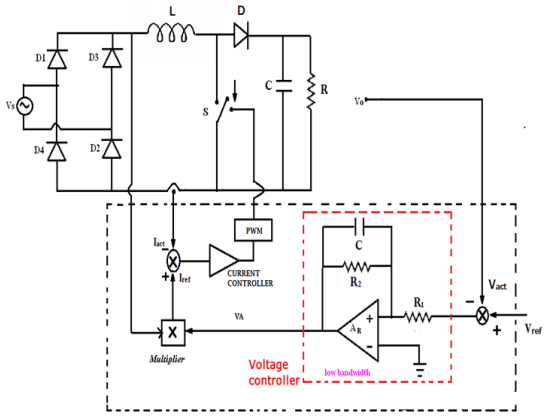
Dr.Ch. Sai Babu[***]
[***]*Professor, Department of Electrical and Electronics Engg.*
JNT University, Kakinada, India, E-Mail:chs_eee@yahoo.co.in.

Abstract*— *The design of an active Power Factor Corrector (PFC) leads to slow transient response in this type of converter. The reason for this is due to compensator placed in the output-voltage feedback loop is frequently designed to have narrow bandwidth to filter the voltage ripple of twice the line frequency obtaining from the PFC output voltage. This feedback loop is designed with this filtering effect because a relatively high ripple would cause considerable distortion in the reference line current feedback loop and line current. However, if the bandwidth of the compensator in the voltage loop is relatively wide, the transient response of the PFC range is improved. As a significance of the voltage ripple at the output of the compensator, both the static and the dynamic behaviors of the PFC change in comparison with no voltage ripple on the control signal. This paper presented, the static behavior of a PFC with appreciable voltage ripple in the output-voltage feedback loop using two parameters: the amplitude of the relative voltage ripple (k) on the control signal and its phase lag angle (ϕ_L).The total power processed by the PFC depends on these parameters, which do not vary with the load and which determine the Total Harmonic Distortion (THD) and the Power Factor (PF) at the input of the power factor correction converter. Finally, the results are verified by MATLAB/ Simulink simulation.

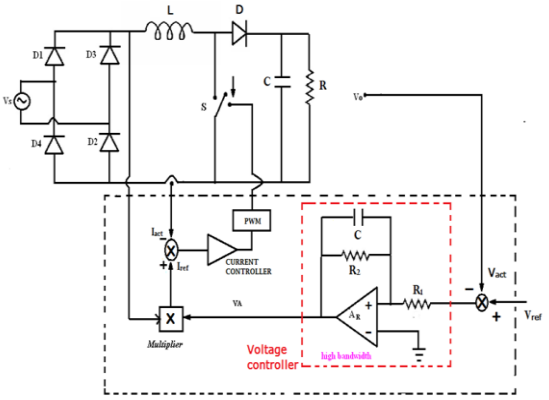
Index Terms— Modeling, AC-DC boost converter, PFC controller, Power supplies.

1. Introduction

In order to limit the harmonic content in mains of supply, the use of active power factor corrector is necessary. Figure 1 shows the general scheme of an active PFC controlled by two feedback loops, which is the most widely-used circuitry to control converters of this type. In this figure1, the two loops are inner current loop and another one is outer voltage loop. The current loop makes the line current follow a reference signal which is obtained by multiplying a rectified sinusoidal waveform (obtained from the line voltage) by V_A. Thus, the line current, i_{gL}, is a sinusoid whose amplitude is determined by the value of V_A. The standard design of the voltage feedback loop is done with low bandwidth to imply low ripple on V_A in order to avoid line current distortion. However, this design with low bandwidth in the output voltage feedback loop, leads to limit the transient response of the PFC.



(a)



(b)

Figure 1 PFC Boost converter with average current mode: (a)Low bandwidth and (b) High bandwidth.

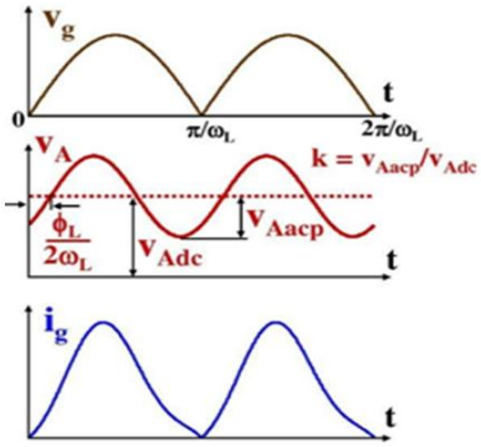


Figure.2 Expected waveforms in a PFC with appreciable voltage ripple on control signal

The transient response of the output voltage loop will be slow with this type of design. To achieve a faster transient response, the bandwidth of the error amplifier A_R, must be relatively high, as a result leading to considerable voltage ripple in the control signal, V_A as shown in Figure. 2 Thus, assuming that A_R has been designed with high bandwidth (allowing non-negligible voltage ripple on V_A so as to achieve a fast response), both the static and dynamic behavior of the PFC change in relation to that corresponding to a design with low-bandwidth in A_R. The voltage ripple on the control signal V_A modifies both the static and dynamic model of the power stage and has a strong effect on the line current waveform obtained at the input of the PFC.

2. Modeling of Output-Voltage feedback loop

The voltage and the current at the input of the power stage, as shown in Fig. 1(b), can be written as follows:

$$v_g(\omega_L t) = v_{gp}\left|\sin(\omega_L t)\right| \quad (1)$$

$$I_{g(}\omega_L t) = \frac{v_{gp}\left|\sin(\omega_L t)\right| v_A(t)}{K_M} \quad (2)$$

Where v_{gp} is the peak value of $v_g(\omega_L t)$, ω_L is the line angular frequency, K_M is a constant and $v_A(t)$ is the voltage at the error amplifier output. This voltage can be rewritten as follows:

$$v_A(t) = v_{Adc} + v_{Aac}(t) \quad (3)$$

$$V_{Aac}(t) = V_{Aacp}\sin(2\omega_L t - \phi_L) \quad (4)$$

Where v_{Adc} is the dc component of $v_A(t)$, $v_{Aac}(t)$ is its ac component, v_{Aacp} is the peak value of $v_{Aac}(t)$ and φ_L is its phase lag angle. The relative value of the voltage ripple on $v_A(t)$ is defined as follows:

$$k = \frac{V_{Aacp}}{V_{Adc}} \quad (5)$$

As there is a influence of voltage ripple on the control signal, $v_A(t)$, all the static electrical quantities of the PFC vary in relation to those corresponding to the standard design case, i.e., with a control signal with no ripple. Figure 2 shows some line waveforms corresponding to a variety of design conditions. As this figure shows, the line current has appreciable distortion, which is a consequence of the voltage ripple on $v_A(t)$. It should be noted that only ripple of twice the line frequency is assumed in $v_A(t)$, which is a logical consequence of the behavior of both the RC output cell ($C_B R_L$) and the error amplifier, A_R, at frequencies greater than twice the line frequency. Therefore, this voltage ripple can be defined by means of only two parameters: its magnitude, v_{Aacp}, and its phase lag angle, φ_L. As the voltage ripple magnitude can be related to v_{Adc} through k (5), then v_{Adc}, k and φ_L completely define the state of the control variable, $v_A(t)$. Where these values have been expressed as functions of k and φ_L and of the power stage variables (i.e., v_{gp}, v_o and R_L). An important design parameter of any PFC is the output voltage ripple. In the case of PFCs with a fast output-voltage feedback loop, this ripple is mainly generated by the current sources. The relative output voltage ripple of twice the line frequency is compared with that of four times the line frequency. Only in the case of high values of k (near to 1) and $\varphi_L \approx -90^o$ does the value of line frequency become significant.

The steady state expressions can be easily obtained as

$$I_{op} = \frac{2V_0\sqrt{1+k2+2k\sin\phi_L}}{R_L(2+k\sin\phi_L)} \quad (6)$$

$$\phi_L = \cos^{-1}[(V_{Aacp}/V_{Adc})\cos\phi_{R2\omega L}] + \phi_{R2\omega L} - \pi/2 \quad (7)$$

The dc component of the output voltage is related to I_{odc} through the impedance of the $R_L C_B$ cell as:

$$V_{odc} = i_{odc}[R_L / (1+R_L C_B S)] \quad (8)$$

3. Simulation Results & Discussion

The simulation model of the PFC boost converter is maintained at 155V for both low bandwidth and high band width. The output voltage has been boosted nearly 400V in both cases. From figure 3 the gate pulses given for closed loop PFC boost converter can be observed clearly and the duty cycle of gate signal has been maintained constant switching frequency (20 KHz).The major difference of low bandwidth model from high bandwidth is considered with the variation of the amplitude of the relative voltage ripple (k) on the control signal and its phase lag angle (ϕ_L) of the output voltage controller. This can be observed from the following figures clearly. Figure 3 Gate Pulses for closed loop system

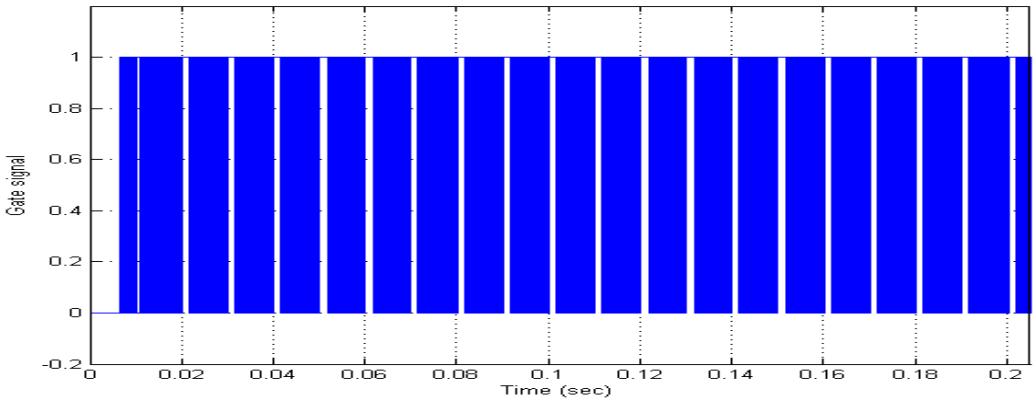
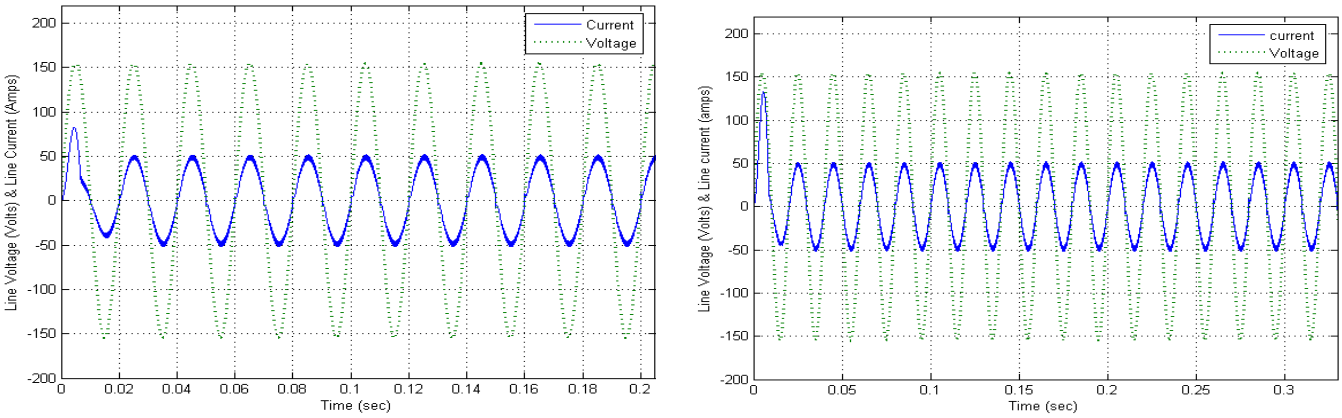
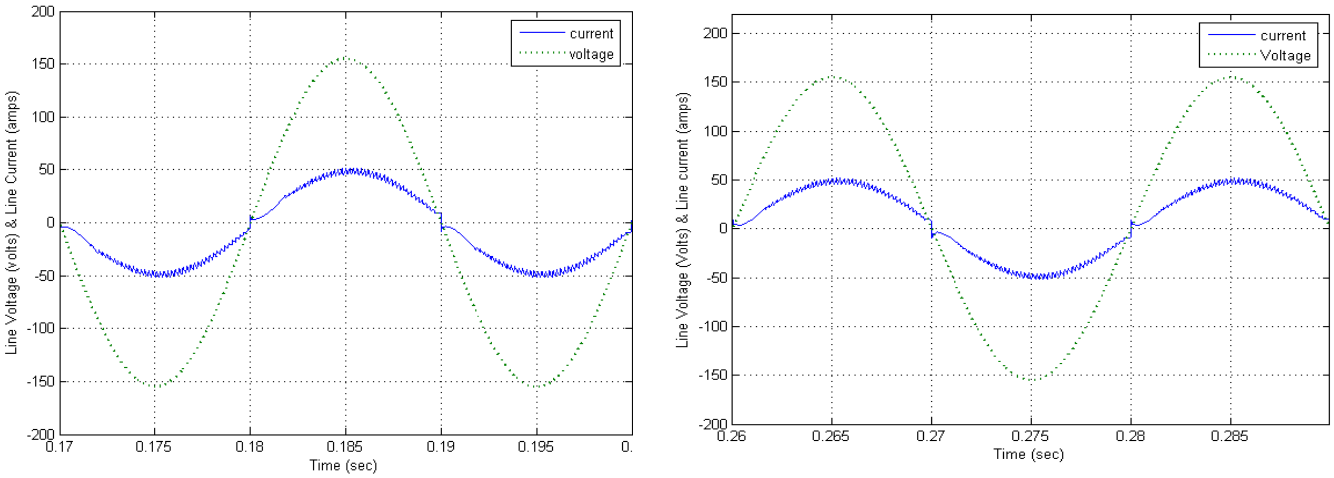


Figure 3 Gate Pulses for closed loop system



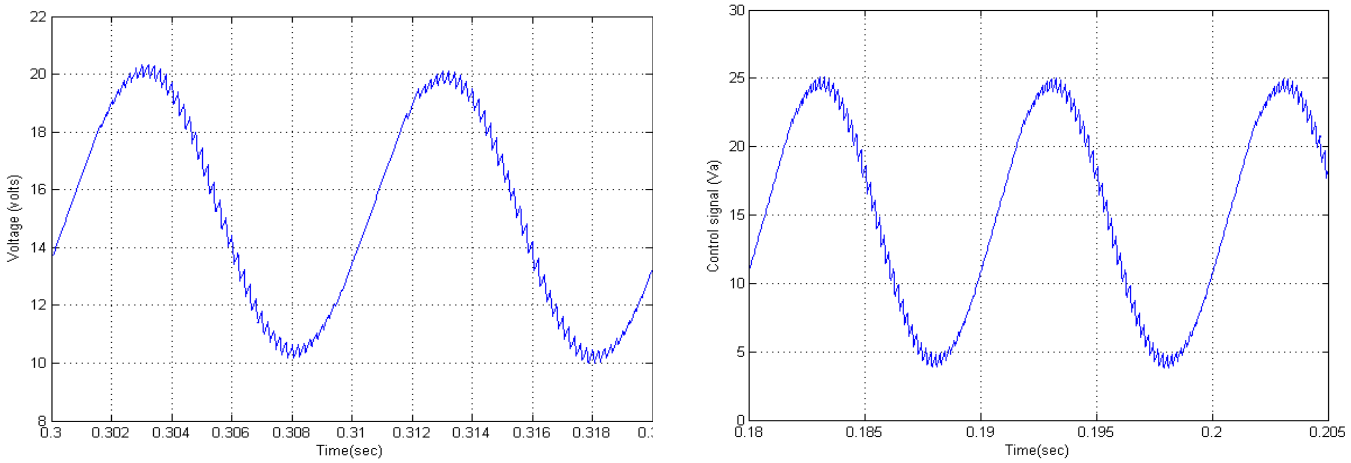
(a) (b)

Figure.4. Response of line voltage & line current: (a) Low bandwidth and (b) High bandwidth



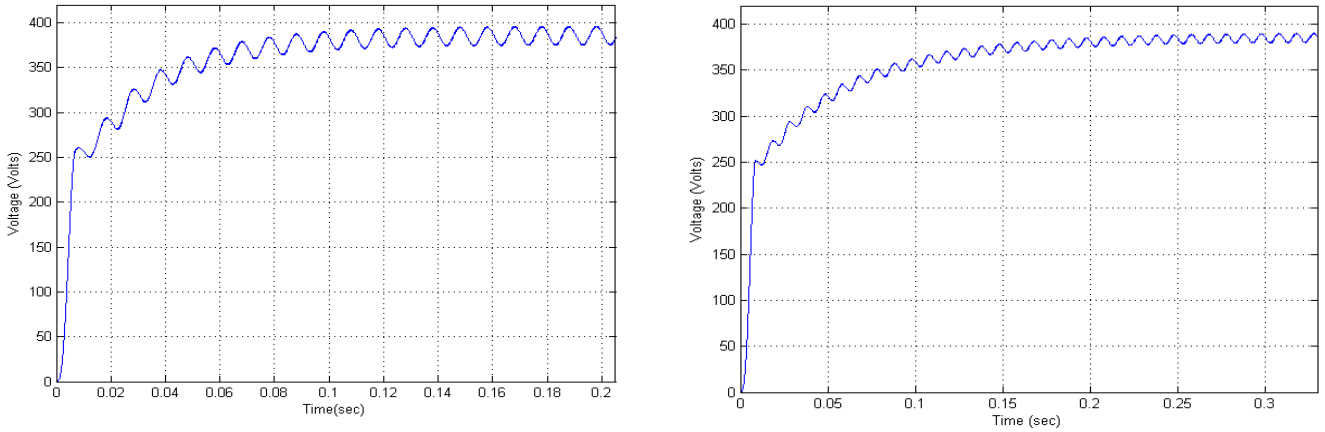
(a) (b)

Figure .5 Zoomed waveforms of Line voltage & Line current: (a) Low bandwidth and (b) High bandwidth



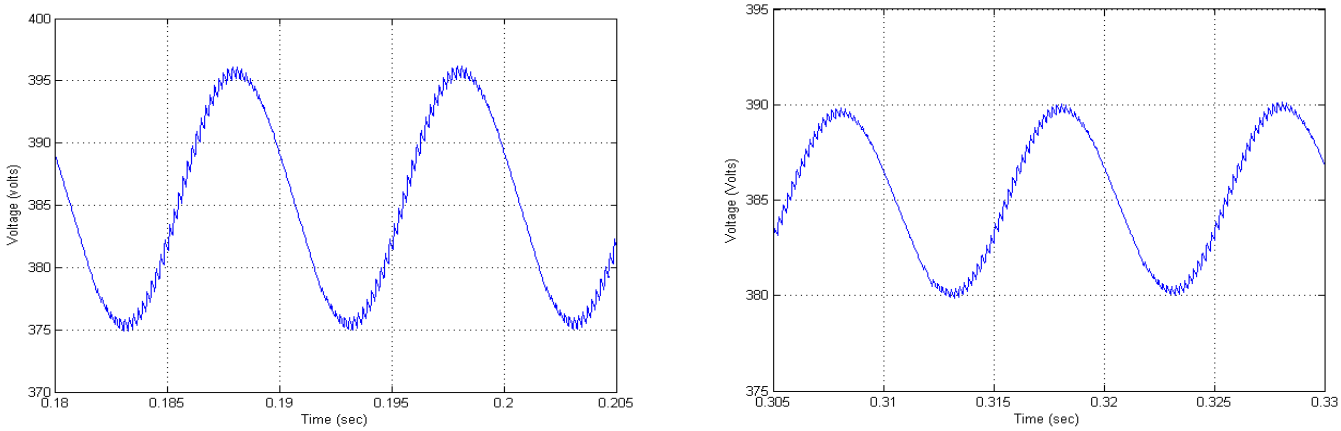
(a) (b)

Figure.6 Control Signal: (a) Low bandwidth and (b) High bandwidth



(a) (b)

Figure.7 Response of output voltage: (a) Low bandwidth and (b) High bandwidth



(a) (b)

Figure.8 Zoomed response of output voltage: (a) Low bandwidth and (b) High bandwidth

It is clear from the the figure 4 (a) & (b) that the power factor has been improved in low band width than that of the high bandwidth. So the classical design of PFC is favorable with low bandwidth to get good power factor but the response is slow at the output side. Figure 5 (a) & (b) shows that the distortion of current response is more in the case of high bandwidth when compared with low bandwidthwidth. Figure 8 (a) & (b) shows the zoomed response of output voltage of boost converter in which the ripple can be observed. Though the ripple content in output voltage is less in case of low bandwidth, the response is slow. Though the ripple content in output voltage is considerable in case of high bandwidth, the response is fast.

Conclusion

The static behavior of a PFC with appreciable voltage ripple in the feedback loop has been observed in this model using two parameters: the amplitude of the relative voltage ripple (*k*) on the control signal and its phase lag angle (ϕ_L). By the variation of these two parameters the required bandwidth to achieve fast transient response with appreciable voltage ripple can be obtained.

Acknowledgement

We express our sincere thanks to RGMCET for providing good lab facilities. This work has been supported by the Research Promotion Scheme grant for the financial assistance provide under ***Ref.No: 8023/RID/RPS-54/Pvt (II Policy) / 2011-12.***

References

1. M. J. Kocher and R. L. Steigerwald, "An ac-to-dc converter with high quality input waveforms", *IEEE Trans. Ind. Appl.*, vol. 19, no. 4, 1983, pp.586-599.
2. L. H. Dixon, "High power factor preregulators for off-line power supplies", *Unitrode Power Supply Design seminar*, 1990, pp I2-1 to I2-16.
3. G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power-factor preregulators: an overview", *6th European Conference on Power Electronics and Applications*, 1995, pp. 3.754-3.759.
4. A. Fernández, J. Sebastián, P. J. Villegas, M. M. Hernando and D. G. Lamar, "Dynamic Limits of a Power-Factor Preregulator", *IEEE Trans. On Ind. Electron.*, vol. 52, no. 1, February 2005, pp.77-86.
5. J. Sebastián, D. G. Lamar, A. Fernández and M. M. Hernando, "Steady state analysis of power factor correctors with a fast output-voltage feedback loop", *IEEE APEC 09*.
6. R. B. Ridley, "Average small-signal analysis of the boost power factor corrector circuit", *VPEC Seminar Proceedings 1989*, pp. 108-120.
7. J. Sebasti´an, D. G. Lamar, M. M. Hernando, M. Rodr´ıguez, and A. Fern´andez, "Average small-signal modelling of the power stage of power factor correctors with a fast output-voltage feedback loop," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 998–1004.
8. J. Sebastian, D. G. Lamar, A. Rodrfguez, M.Arias and A. Fernandez., "On the maximum bandwidth attainable by power factor correctors with a standard compensator," in Proc. IEEE Appl. Power Elctron.Conf.Expo..2009,pp.1872-1878.
9. J. Sebasti´an,A. Fern´andez, P.Villegas, M. M. Hernando, and J.M. Lopera,"A new active input current shaper for converters with symmetrically driven transformer," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 592–600, Mar./Apr. 2001.

R. Satish Kumar was born in Kurnool, Andhra Pradesh, India in 1985. He received the B.Tech (Electrical and Electronics Engineering) degree from JNT University, Hyderabad affiliated college in 2007. He is pursuing M.Tech (Power Electronics) in RGMCET (Autonomous), Nandyal.
e-mail:satishraguru@gmail.com.

D.Lenine was born in Pondicherry, India in 1978. He received the B.Tech (Electrical and Electronics Engineering) degree from Pondicherry University, India in 2004 and the M.Tech (Electrical Drives and Control) from same University in 2006 and Ph.D in Digital Controller based Power Factor Correction Converter from JNT University, Kakinada in 2013. In 2006 (October) he joined the Dept. Electrical and Electronics Engineering , R.G.M. College of Engineering and Technology, Nandyal, as a Assistant Professor. Currently he is working as an Associate Professor in Dept. of EEE. RGMCET, Nandyal. He has published/presented several technical research papers in national and international Journals/conferences. His field of interest includes AC-DC Converter, Power factor correction, Electrical Drives, Digital control Techniques, Digital control of electrical machines and Estimation of machines parameters.
e-mail:lenine_2004@yahoo.com.

Ch. Sai Babu received the B.E from Andhra University (Electrical & Electronics Engineering), M.Tech in Electrical Machines and Industrial Drives from REC, Warangal and Ph.D in Reliability Studies of HVDC Converters from JNTU, Hyderabad. Currently he is working as a Professor in Dept. of EEE in JNTUCE, Kakinada. He has published several National and International Journals and Conferences. His area of interest is Power Electronics and Drives, Power System Reliability, HVDC Converter Reliability, Optimization of Electrical Systems and Real Time Energy Management.
e-mail: chs_eee@yahoo.co.in.