PERFORMANCE ANALYSIS OF MULTILEVEL INVERTER WITH SPWM STRATEGY USING MATLAB/SIMULINK

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Abstract**:** *Lower prices of power switches and new semiconductor technologies, as well as the current demand on high-performance inverters required by renewable energy systems, have extended the applications of multilevel converters. This paper presents the important topologies of multilevel inverter like diode-clamped (neutral-point clamped), and cascaded H-bridge with separate dc sources. This paper also presents the most relevant sinusoidal pulse width modulation method for this family. Simulation and comparison of NPC and cascaded H-bridge multilevel inverter with SPWM switching is done using MATLAB/SIMULINK***.**

Key words*: Multilevel, neutral point clamped, cascaded H- Bridge, Pulse width modulation, MATLAB/SIMULINK, THD.*

1. Introduction

Multilevel converters have been mainly used in medium - or high-power system applications, such as static reactive power compensation and adjustable-speed drives. In these applications, due to the limitations of the currently available power semiconductor technology, a multilevel concept is usually a unique alternative because it is based on low-frequency switching and provides voltage and/or current sharing between the power semiconductors [1]–[4].

On the other hand, for low-power systems (< 10 kW), multilevel converters have been competing with high-frequency pulse width-modulation converters in applications where high efficiency is of major importance. [5]–[10].

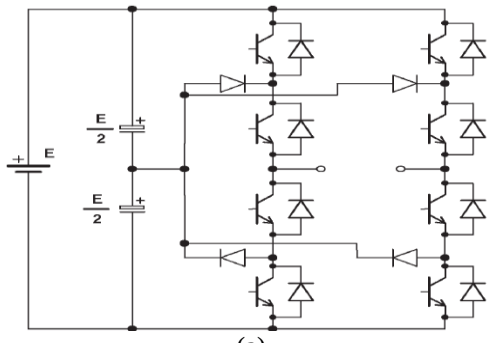
According to these facts, it is evident that a device capable of converting a single dc voltage from a battery bank into an ac voltage is a key element of most stand-alone photovoltaic systems. These dc/ac converters, which are commonly referred to as inverters, have experienced great evolution in the last decade due to their wide use in uninterruptible power supplies and industrial applications. However, it is still a critical component to most stand-alone renewable energy systems, and the development of high performance inverters is a challenge even today [11]–[13].

In both dc- and ac-bus configurations, since the generator does not continuously operate and considering the intermittency of the renewable energy sources, it is possible to conclude that the battery inverter should be designed to fully support the loads at some time periods. Therefore, independently of the system configuration, it is possible to identify that at least one "strong battery inverter" is required.

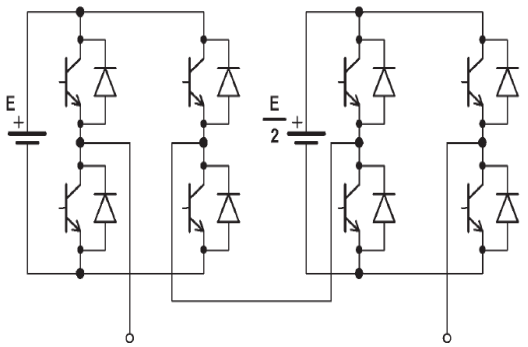
Having in mind that stand-alone renewable energy systems only make sense if they can be reliable and flexible, then all balance-of-system components must be accomplished with these characteristics [15]. This way, to the best of the author's knowledge, the most important characteristics of a renewable energy systems battery inverter, concerning the order of importance, are as follows:

- reliability (most important);
- surge power capacity;
- no-load consumption and efficiency.

This paper investigates about the important topologies of multilevel inverter like diode-clamped (neutral-point clamped), and cascaded H-bridge with separate dc sources. In this paper the simulation and comparison of NPC and cascaded H-bridge multilevel inverter with SPWM switching is done using MATLAB/SIMULINK.



(a)



(b)

Fig. 1. The topologies considered in this paper.
(a) NPC. (b) Cascade H-bridge

2. Feature of Applied Phase Shift Modulation Strategy

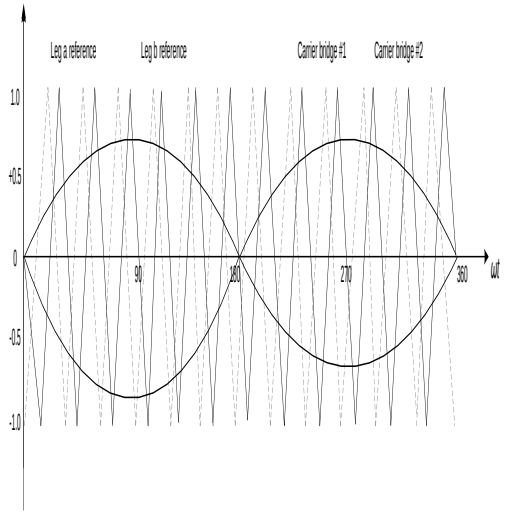


Fig. 1(c). Phase shifted modulation strategy.

- Device voltage sharing is automatic and there is no restriction on switching patterns.
- CMC has smaller dv_o/dt compared to series connected 2-level.
- Because of its modular structure, control is more easily applied.
- Compared to other multilevel topologies, CMC requires least number of components, because there is no need for clamping diodes and flying capacitors.
- Each cell needs an isolated DC supply and normally this requires some sort of complicated transformer arrangement.

The aforementioned disadvantage is not an issue in Photovoltaic applications, because discrete strings of PV modules provide isolated input voltage sources. In photovoltaic applications, the inverter stage can be implemented with or without a DC-DC converter. However, the topology without a DC-DC stage is examined. There are different options for modulation of multilevel converters. One of the simplest strategies is the phase shifted carrier modulation technique as shown in Fig. 1(c). where the n carriers of the full bridge cascaded converters are phase shifted by 180/n degrees. This modulation technique is utilized due to its simplicity [16]

3. Trial of Topologies Using MATLAB/SIMULINK

3.1 Diode-Clamped Inverter

A three-level diode-clamped inverter is shown in Fig. 2(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors *n* can be defined as the neutral point. The output voltage v_{an} has three states: $V_{dc}/2$, 0, and -$V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for -$V_{dc}/2$, switches $S_1'$and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across *a* and 0 is V_{dc}, i.e., $v_{ao}= V_{dc}$. In this case, balances out the voltage

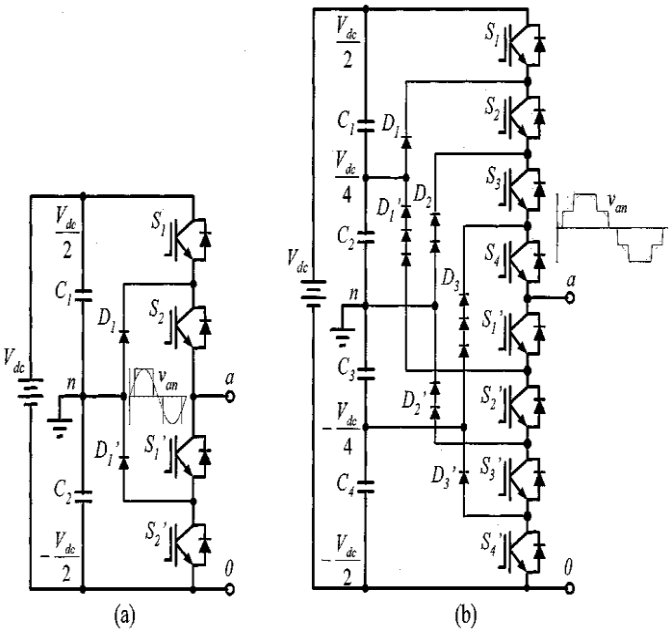


Fig. 2. Diode-clamped multilevel inverter circuit topologies.
(a) Three-level, (b) Five-level.

sharing between $S_1'$and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Notice that output voltage v_{an} is ac, and v_{ao} is dc. The difference between v_{an} and v_{ao} is the voltage across C_2, which is $V_{dc}/2$. If the output is removed out between *a* and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$, and 0.

Fig. 2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors C_1, C_2 , C_3 , and C_4 . For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across *a* and *n*.

1) For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches
   S_1-S_4
2) For voltage level $V_{an} = V_{dc}/4$, turn on three upper switches S_2-S_4 and one lower switch S_1' .
3) For voltage level $V_{an} = 0$, turn on two upper switches S_3-S_4 and two lower switches S_1' and S_2'.
4) For voltage level $V_{an} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches S_1' - S_3' .
5) For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches
   $S_1' – S_4'$.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1 , S_1'), (S_2 , S_2'), (S_3 , S_3'), and (S_4 , S_4').

Although each active switching device is only required to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes must have different voltage ratings for reverse voltage blocking.

Using D_1' of Fig. 2(b) as an example, when lower devices $S_2' – S_4'$ are turned on, D_1' needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly D_2, and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1)$ x $(m-2)$. This number represents a quadratic increase in *m*. When *m* is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.[17]

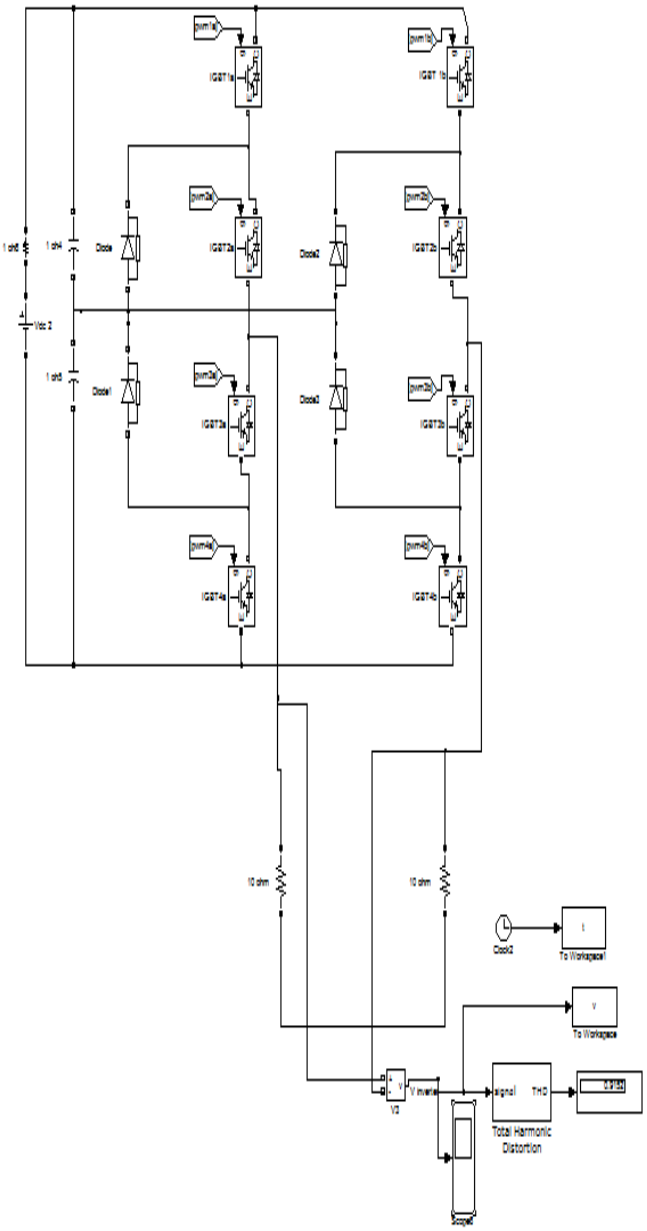


Fig. 3(a). Simulink model of 2-leg, 5-level NPC MLI

Fig. 3(a) shows a Simulink model of 2-leg, 5-level neutral-point-clamped (NPC) inverter. It was the first widely popular multilevel topology, and it continues to be extensively used in industrial applications. Later, the NPC inverter was generalized for a greater number of levels, using the same concept of diode-clamped voltage levels, which resulted in the current designation of a diode-clamped converter [14].

As it can be seen in Fig. 3(a), the five-level NPC inverter uses capacitors to generate an intermediate

voltage level, and the voltages across the switches are only half of the dc input voltage. Due to capacitor voltage balancing issues, practical diode-clamped inverters have been mostly limited to the original three-level structure as shown in Fig. 2(a).

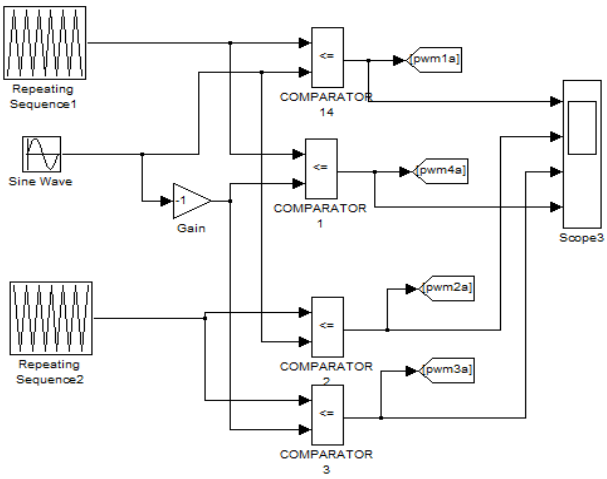


Fig. 3(b). SPWM Switching pattern of leg-1, of 5-level NPC MLI

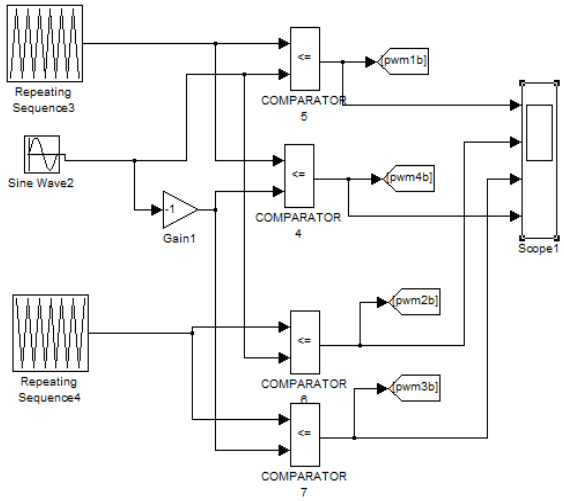


Fig. 3(c). SPWM Switching pattern of leg-2, of 5-level NPC MLI

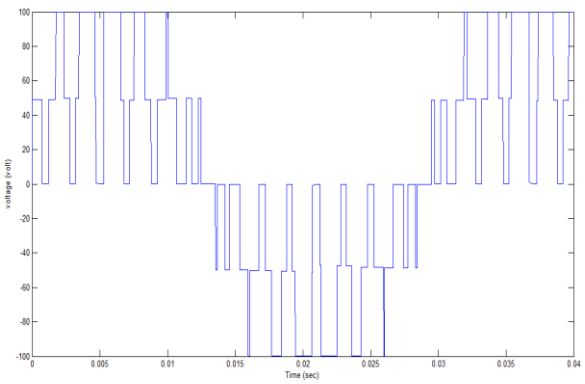


Fig. 3(d). Output voltage waveform of 5-level NPC MLI

Fig. 3(b) shows the SPWM switching for the first leg of the five level NPC MLI in which triangular carrier waveform (repeating sequence) is compared with sinusoidal reference wave form. Fig. 3(c) is for the SPWM switching for the second leg of the five level NPC MLI in which reference sinusoidal wave has phase delay of (3.14/180)*240 with respect to previous sinusoidal reference wave of first leg is done to achieve the five-level output voltage waveform as shown in Fig. 3(d).

3.2 Cascaded H-Bridge Inverter

The Cascaded Multilevel Converters (CMC) is simply a number of conventional two-level bridges, whose AC terminals are simply connected in series to synthesize the output waveforms. Fig. 4. shows the circuit topology for a five-level inverter with two cascaded cells. The CMC needs several independent DC sources which may be obtained from batteries, fuel cells or solar cells.

Through different combinations of the four switches of each cell, each converter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$. The AC output is the sum of the individual converter outputs. The number of output phase voltage levels is defined by n = 2N+1, where N is the number of DC sources. [17]

Although the original cascaded topology requires several isolated dc sources, in some systems, they may be available through batteries or PV panels; thus, it has been used to implement high-efficiency transformer less inverters

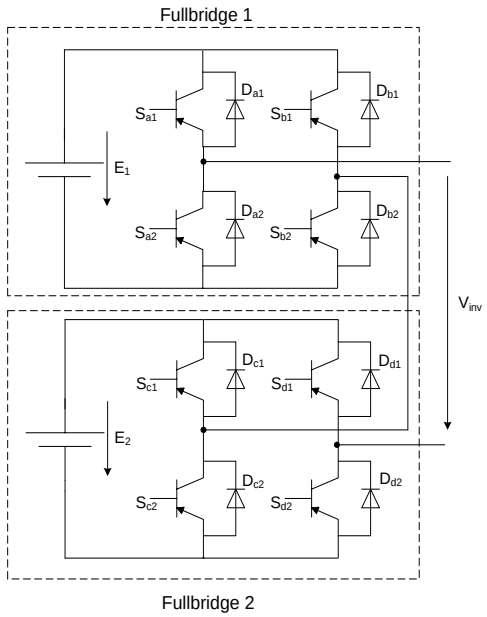


Fig. 4. 5-level Cascaded H- bridge multilevel inverter circuit topology

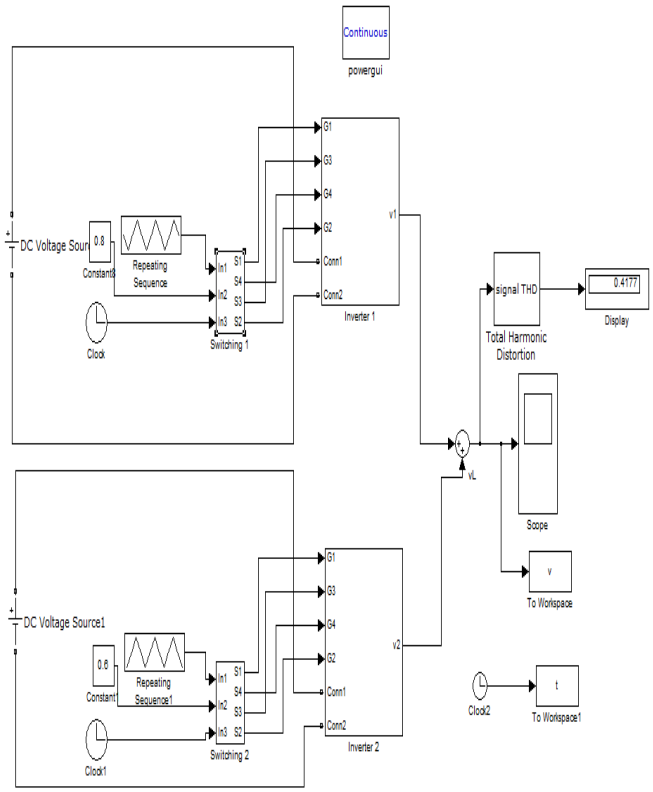


Fig. 5(a). Simulink model of 5-level Cascaded H- bridge multilevel inverter

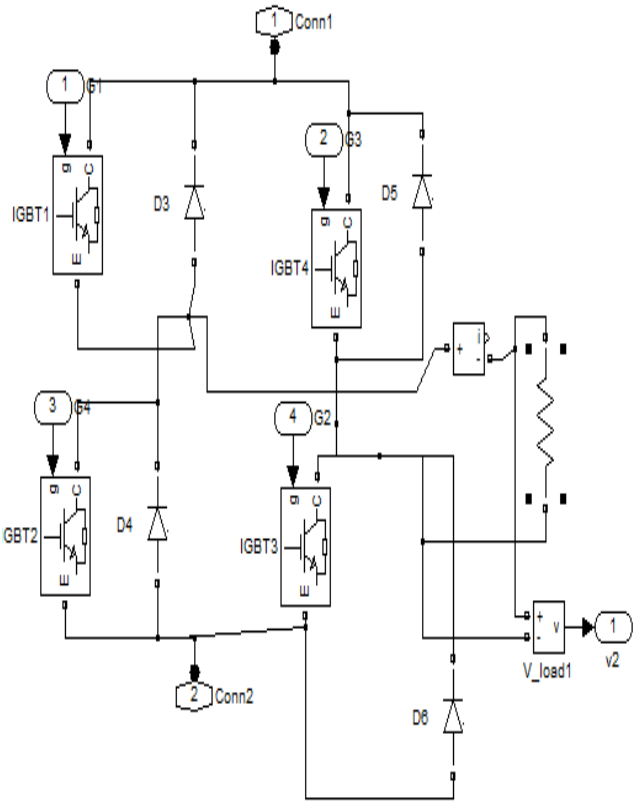


Fig. 5(b). Simulink model of an H- bridge cell used for Multilevel inverter

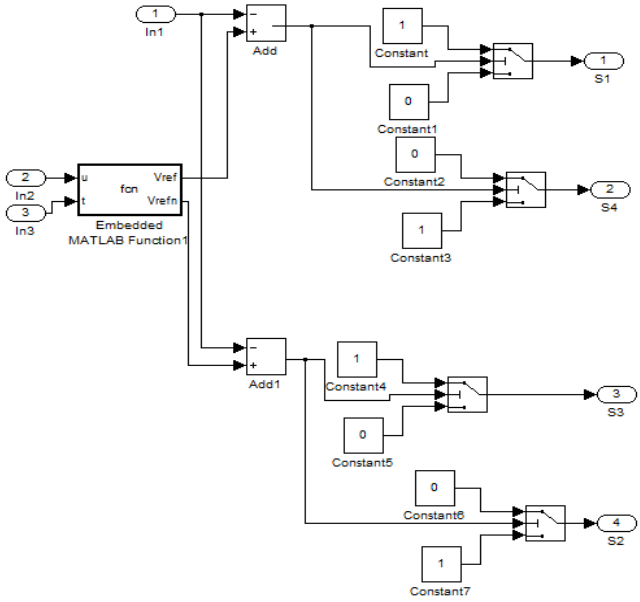


Fig. 5(c). SPWM Switching pattern of 5-level Cascaded H- bridge multilevel inverter

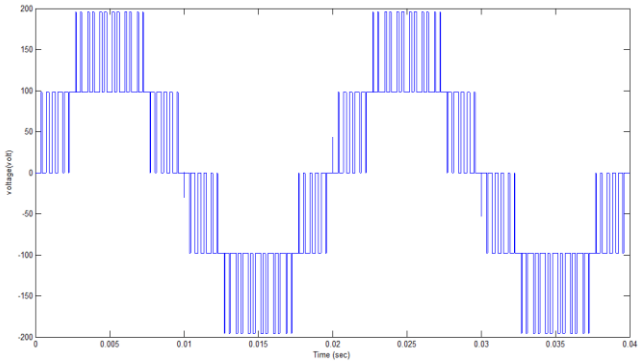


Fig. 5(d). Output voltage waveform of 5-level Cascaded H- bridge multilevel inverter

4. Total Harmonics Distortion (THD)

Total Harmonic Distortion (THD) is the most common power quality index to describe the quality of power electronic converter. In general, all the output voltage of power electronic converters is not purely sinusoidal [18]. The THD of the output voltage can be defined as:

$$THD = \frac{\sqrt{\sum_{n=2,3\ldots}^{\infty} V_n^2}}{V_1} = \frac{\sqrt{V_{rms}^2 - V_1^2}}{V_1}$$

Where n denotes the harmonic order and V_1 is fundamental quantity (voltage). For inverter application, THD represents how close the AC output waveform with pure sinusoidal waveform. A high-quality inverter system should have low THD [18].

5. Comparison of THD in NPC 5-level SPWM inverter and H-bridge cascaded 5-level SPWM inverter

It is seen from the obsevation of the Simulink models of NPC 5-level SPWM inverter and H-bridge cascaded 5-level SPWM inverter that the THD of H-bridge cascaded 5-level SPWM inverter is lower than the NPC 5-level SPWM inverter which is shown in Fig. 6.

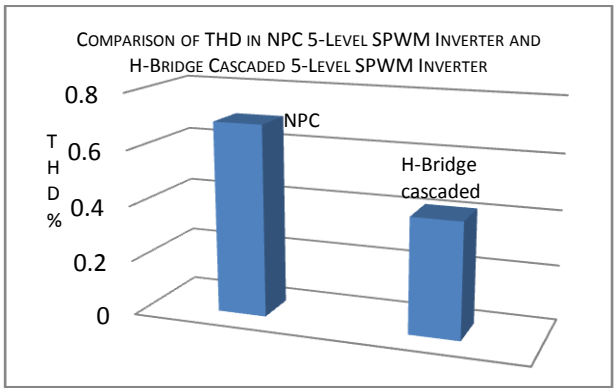


Fig. 6. Comparison of THD

6. Conclusion

It is seen from the study of NPC and Cascaded H-Bridge Multilevel inverters that cascaded inverters have better THD. And they both are very important because their THD is better than conventional three level inverters. Due to decrease in the price of switching devices Cascaded H-Bridge MLI is more promising for Photo-voltaic (PV) applications. A multilevel cascaded inverter is also given preference over others because it utilizes two or more than two different strings of SPV array as a voltage source for each cell of a multilevel inverter.

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