

# MINIMIZING THE THD OF 27-LEVEL CMLIS FOR MANY APPLICATIONS

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**Abstract:** The 27-level cascaded multilevel inverter (CMLI) has recently many applications in electrical power engineering, such as for control of ac motor drives and for interfacing renewable energy sources with the smart grid. This is due to its simplicity of construction as a trinary asymmetric CMLI, that consists of only three H-bridges with unequal dc sources of values  $E$ ,  $3E$  and  $9E$ ., and at the time can provide a nearly sinusoidal output voltage. Minimizing the exact total harmonic distortion (THDE) of the output voltage of the 27-level CMLI is an important issue, since this will improve the performance by decreasing the losses and increasing the efficiency. An approach using a mixed integer nonlinear programming (MINLP) model is introduced to determine the switching angles of the power switches of the 27-level CMLI that minimize the THDE for both single phase and three phase CMLIs. Formulas for the THDE are included in the model for both single phase and three phase cases. The results show very low values of %THDE and of the upper limit of the amplitude of any undesired harmonic relative to the amplitude of the main harmonic (%  $V_{Hmax}$ ) in both cases over wide voltage ranges, which agree with the IEEE standards 519-1992 for voltage distortion limits till 161 kv.

**Key words:** Cascaded multilevel inverters, Exact total harmonic distortion, harmonic analysis, Mixed integer non-linear programming

## 1. Introduction

In recent years multilevel inverters have become a very interesting field of study regarding the industrial applications. These inverters allow the synthesizing of a sinusoidal voltage waveform starting from several levels of dc sources. However, besides that advantage there are other important advantages such as reduced switching losses, low  $dv/dt$ 's and reduced common mode voltages. Due to these characteristics several multilevel inverter topologies have been developed and studied.

Cascaded multilevel inverter (CMLI) is the most recent and popular type of multilevel inverters, that synthesizes a desired sinusoidal voltage from several separate dc voltage sources. The general construction of the CMLI is shown per phase in Fig. 1. It consists of  $S$  H-bridges fed with dc voltages sources  $E_1$ ,  $E_2$ , ..and  $E_S$ . The output voltage is usually constructed in a stair case shape, Fig. 2, to approach synthesizing a sinusoidal wave form, [1].

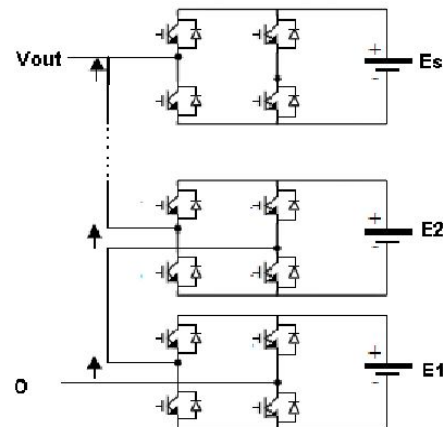


Fig. 1 A cascaded multilevel with  $S$  dc sources

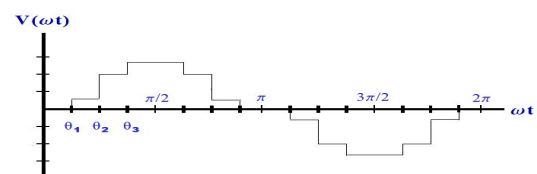


Fig. 2 A staircase output voltage wave form with 3 positive levels

If all the dc sources are of equal value, say  $E$ , the CMLI is called symmetric. In this case the maximum number of the positive levels of the inverter is  $S$  and is obtained by switching on the dc sources sequentially, and these levels may take the values  $E, 2E, \dots$ , and  $S E$ . While if the dc sources are of unequal values the CMLI is referred to as an asymmetric CMLI. In this case the maximum number of the positive levels of the inverter can be increased greatly, since it could be possible to switch on some dc sources positively or negatively within the positive half cycle of the output voltage, thus adding additional positive levels. Generally, the possible positive levels of an asymmetric CMLI are all the positive values of  $I_1 E_1 + I_2 E_2 + \dots + I_S E_S$ , where each of  $I_1, I_2, \dots$ , and  $I_S$  can take one of the values  $-1, 0$  or  $+1$ . The number of all possible levels is  $(3)^S$ , some of them may be redundant. Increasing the number of levels of the inverter means that its staircase output wave form can approach more closely a sinusoidal wave form, which in turn means that the output voltage low order harmonic values and their total harmonic distortion could be reduced greatly, which make asymmetric CMLIs more popular for practical applications [2].

To obtain a staircase output voltage wave form with equal step heights in an asymmetric CMLI, the following uniform step sufficient conditions may be satisfied by the dc sources  $E_1, E_2, \dots$  and  $E_S$ , [3]:

1-  $E_1 \leq E_2 \leq \dots \leq E_S$ ,  $E_1 < E_S$  and each of  $E_2, E_3, \dots$  and  $E_S$  is an integer multiple of  $E_1$ .

$$2- E_j \leq E_1 + 2 \sum_{r=1}^{j-1} E_r, \quad \text{and } j=2, 3, \dots, S$$

It is possible to obtain the maximum number of levels in an CMLI, i.e.  $(3)^S$  non-redundant or different levels, by replacing the inequality sign in the third condition with an equality sign. Thus with  $E_1 = E$  we get  $E_2 = 3E$  and  $E_3 = 9E$  and the associated three H-bridges form the well known trinary asymmetric CMLI with the  $(3)^3 = 27$  levels:  $0, \pm E, \pm 2E, \pm 3E, \dots$  and  $\pm 13E$ , [4]. Trinary asymmetric CMLIs can give a better approximation of a sine wave than other asymmetric CMLIs, [5]. The 27-level asymmetric CMLI is thus recommended for many applications, such as for induction motor traction drives [6,7] and for interfacing renewable energy sources with the smart AC grid [8].

In this paper the 27-level CMLI is considered, and a new approach, depending on nonlinear integer programming optimization for determining the switching angles of this inverter that minimize the THDE, is introduced and applied for single phase and three phase inverters.

## 2. A proposed approach for determining the switching angles of the inverter

A fundamental issue for a CMLI is to find the switching angles (times) of the inverter H-bridges semiconductor power switches that produce the required fundamental voltage and at the same time eliminate or reduce as much as possible the values of all undesired harmonics, which tend to reduce the THDE. Many methods are given in the literature for obtaining the switching angles of symmetric as well as uniform step asymmetric CMLIs. These are mainly:

- 1- Using pulse width modulation (PWM) methods, e.g [9].
- 2- Using a selective harmonic elimination technique, where the zero equations of the undesired harmonics with the equation of the desired amplitude of the main harmonic as functions of the switching angles are solved, e.g. [1].
- 3- Using the method of minimizing the total harmonic distortion using genetic algorithms, e.g. [10,11].

However, all these methods are suitable mainly for CMLIs with small number of positive levels, and thus are not adequate for a 27-level inverter with 13 positive levels.

In addition, the author has introduced a method based on a general linear programming optimization model that could be applied to minimize the values of the undesired harmonics and applied it for the 27-level CMLI [12]. However, this method does not assure minimizing the THDE.

The value of the THDE of the CMLI depend mainly on the values of the switching angles of the inverter, which determine the values of the output voltage at different instantaneous times of the time cycle of the main harmonic. The proposed approach is a nonlinear optimization model that determine these values in order to minimize the THDE. In the next sections this model is introduced and solved using an operation research software package for solving nonlinear mixed integer programming

(NLMIP) optimization problems for both single phase and three phase 27-level CMLI. This model is next solved for different values of the required output voltage.

### 3. The proposed mathematical model

A general uniform step asymmetric CMLI, or a symmetric CMLI, with a step height  $E$  is considered, where all the inverter levels are spaced equally. It is assumed, without loss of generality, that the inverter levels are equally spaced by 1 volt, i.e. normalized with respect to the dc voltage  $E$ . It is assumed also that the inverter output voltage wave form  $F(wt)$  is an odd-sines periodic function, as that shown in Fig. 2. The pattern of this function is generated by on and off switching of the inverter H-bridges semiconductor power switches, and is completely determined by defining the switching pattern over the interval  $0 \leq wt \leq \pi/2$ . The basic approach depends on dividing this interval into  $N$  equal small subintervals, starting at the angles  $0, \tau, 2\tau, \dots, (I-1)\tau, \dots$  till  $(N-1)\tau$ , where  $\tau = \pi/2N$ , Fig.3.

The positive integer values  $X_I, I=1, 2, \dots, N$  are defined over each subinterval, to represent the required instantaneous output voltage level value  $F(wt)$  of the inverter, so that  $F(wt)$  is defined over the interval  $0 \leq wt \leq \pi/2$  by:

$F(wt) = X_I$  for  $(I-1)\tau \leq wt \leq I\tau$  and  $I=1,2,\dots,N$

The odd-sines Fourier series expansion of  $F(wt)$  is given by,[12] :

$$F(wt) = \sum_{m=0}^{\infty} V_{2m+1} \sin(2m+1)wt, \quad \text{where}$$

$$V_{2m+1} = (4/\pi) \int_0^{\pi/2} F(wt) \sin(2m+1)wt \, dwt$$

$$= (8/\pi)(2m+1) \sum_{I=1}^{N} X_I \sin(2m+1)\tau/2 \sin(2m+1)(\theta_I + \tau/2) \quad (3.1)$$

where  $(2m+1)$  is the order of the harmonic,  $m=0,1,2,\dots,\infty$ ,  $\tau = \pi/2N$ , and  $\theta_I = (I-1)\tau$ .

The value of the amplitude of main harmonic corresponds to  $V_1$ , i.e. by substituting  $m=0$  in equation (3.1).

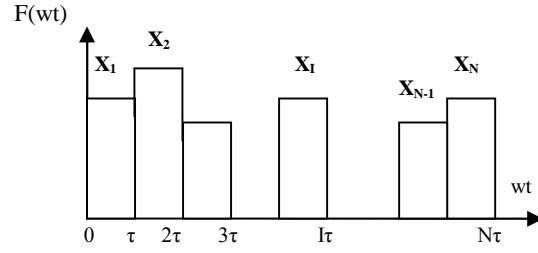


Fig. 3. Representation of  $F(wt)$  by  $X_I, I= 1, 2, \dots, N$  over the interval  $0 \leq wt \leq \pi/2$

Equation (3.1) shows that  $V_{2m+1}$  for any value of  $m$  is a linear function of the integer values  $X_I, I=1,2,\dots,N$ . Variations of the values of  $X_I$  from a subinterval to a next one determine the required switching angles of the inverter that must be applied to produce these levels..

It is required to find the values of  $X_I$  that minimize the value of THDE. A mixed integer nonlinear programming (MINLP) problem is formulated as follows :

Minimize THDE subject to the constraints:

$$* V'_1 - \Delta \leq V_1 \leq V'_1 + \Delta \quad (3.2)$$

$$* X_I \leq X_{I+1}, \text{ for } I=1,2,\dots,N-1, \text{ and } X_N \leq L \quad (3.3)$$

$$* X_I \geq 0 \text{ and integer for } I=1,2,\dots,N \quad (3.4)$$

In constraint (3.2) :  $V'_1$  is the required amplitude of the main harmonic, and  $\Delta$  is a small incremental value,  $\Delta \ll V'_1$ , arbitrary chosen and added to the main harmonic constrain to add more flexibility for obtaining an optimum solution regarding the trigonometric nature of the problem. The value of  $\Delta$  is taken 2% of  $V'_1$ , so that the obtained value of  $V_1$  does not differ practically from the required value of  $V'_1$ . Noting that the IEEE standards for allowable fluctuations in the output voltage for electric services is  $\pm 5\%$  [13] and may be limited for some computer loads to  $\pm 3\%$  [14].

By constraints (3.3) the positive staircase wave form shape is assured with maximum height  $L$ , where  $L$  is the number of the positive voltage levels of the inverter.

Constraints (3.4) are the integer constraints imposed on  $X_I$ .

Once all the parameters of this MINLP model are given, an optimum solution could be obtained that gives the values of  $X_I$  and THDE using any of the well known operations research software packages that solve MINLP optimization problems, e.g. "LINGO" software with "Nonlinear" and "Global" options [15]. Most of these models can solve large size problems with hundreds of variables and constraints.

When solving this MINLP models, it will include the following formulas for calculating the exact total harmonic distortion (THDE) for both single phase and three phase cases, and the upper limit of the amplitude of any undesired harmonic relative to the amplitude of the main harmonic ( %  $V_{Hmax}$  ), to compare these with the required IEEE standards for voltage distortion limits

#### 4. Formulas for calculating %THD and % $V_{Hmax}$ of the undesired output harmonics

##### 4.1 The formulas for calculating the %THDE

The exact total harmonic distortion (%THDE) including all possible undesired harmonics is given by:

$$THDE = [\sum_{m=1}^{m=\infty} \{V_{2m+1}/V_1\}^2]^{0.5}$$

The value of THDE could be obtained as function of the values of  $X_I$  using the following expressions, [16]:

- For single phase CMLI, the output phase voltage THDE is given by:

$$THDE = [ \{ (1/N) ( \sum_{I=1}^{I=N} X_I^2 ) / V_{1rms}^2 \} - 1 ]^{0.5} \quad (3.5)$$

where  $V_{1rms}$  is the root mean square value of the main harmonic.

- For a balanced three phase CMLI, the output phase voltage THDE is given by, assuming that N is a multiple integer of 3,:

$$THDE = [ \{ (1/2N) ( \sum_{I=1}^{I=2N} Z_I^2 ) / V_{1rms}^2 \} - 1 ]^{0.5} \quad (3.6)$$

where:

$$Z_I = X_I - Y_I \quad \text{for } I=1, 2, \dots, N$$

$$Z_I = XX_I - YY_I \quad \text{for } I=N+1, \dots, 2N$$

$$Y_I = -X_{(2N/3)+1} \quad \text{for } I=1, 2, \dots, N/3$$

$$Y_I = -X_{(4N/3)-1} \quad \text{for } I=(N/3)+1, \dots, N$$

$$XX_I = X_{2N+I-1} \quad \text{for } I=N+1, \dots, 2N,$$

$$YY_I = -X_{(4N/3)+I-1} \quad \text{for } I=N+1, \dots, 4N/3$$

$$YY_I = X_{I-(4N/3)} \quad \text{for } I=(4N/3)+1, \dots, 2N$$

##### 4.2 The formula for calculating the % $V_{Hmax}$

To calculate the upper limit of the amplitude of any harmonic among all the undesired harmonics relative to the amplitude of the main harmonic (%  $V_{Hmax}$ ), the MINLP model is programmed to calculate the following values:

1-The maximum amplitude value among all the undesired low order harmonics till the 99<sup>st</sup> harmonic (% $V_{LH}$ ) relative to the amplitude of the main harmonic:

$$V_{LH} = \max_{m=1, \dots, 49} (V_{2m+1} / V_1) \quad (3.7)$$

2- The total harmonic distortion (%THD1) of the low order harmonics calculated till the 99<sup>st</sup> harmonic:

$$THD1 = [ \sum_{m=1}^{m=49} \{ V_{2m+1} / V_1 \}^2 ]^{0.5} \quad (3.8)$$

3- The root of the sum of squares of the amplitudes of all the high order harmonics above the 99<sup>th</sup> harmonic relative to the square of the amplitude of the main harmonic (%  $V_{HH}$ ) is calculated by using the expression:

$$V_{HH} = [THDE^2 - THD1^2]^{0.5} \quad (3.9)$$

From (3.7) and (3.9) an upper limit of the amplitude of any harmonic among all the undesired harmonics relative to the amplitude of the main harmonic (  $\% V_{Hmax}$  ) is taken as:

$$V_{Hmax} = \max ( V_{LH}, V_{HH} ) \quad (3.10)$$

In the next sections when the MINLP model is applied,, the values of the %THDE and the  $\%V_{Hmax}$  are calculated and compared with the IEEE standards 519-1992 for voltage distortion limits for both the %THDE and the  $\%V_{Hmax}$  (IEEE Standard 519-1992), which are, [17].:

\* For output voltages  $\leq 69$  kv , the % THDE must be  $\leq 5\%$  and the  $\% V_{Hmax}$  must be  $\leq 3\%$ .

\* For output voltages between 69 kv and 161 kv , the % THDE must be  $\leq 2.5$  and the  $\% V_{Hmax}$  be  $\leq 1.5\%$ .

### 5.Solution of the model for a 27-level single phase CMLI

The MINLP given in section III is solved for a single phase 27-level CMLI, for the required amplitude of the output voltage  $V_1'$  considering the following:

- 1- Taking  $\Delta = 0.02 V_1'$ .
- 2- Taking the expression for calculating the THDE given by equation (3.5), where  $V_{rms}^2 = 2 V_1^2$  and  $V_1$  is taken from equation (3.1) by substituting  $m=0..$
- 3- Taking the number of subintervals  $N= 180$ ,which corresponds to an interval width  $\tau = 90/180= 0.5^\circ$  ,and the number of positive levels  $L = 13$ .
- 4- Taking expressions (3.8) and (3.10) to calculate THD1 and  $V_{Hmax}$  , substituting for  $V_{2m+1}$  from equation (3.!).

The model solved thus consists of 180 variable correspond to  $X_l$  , which are considered integer and nonlinear, and 361 constraints corresponding to the constraints (3.2), (3.3) and (3.4).

The model is solved for values of  $V_1'$  between 4 and 15, normalized with respect to the reference dc voltage  $E$ . Figure 4 shows the obtained corresponding values of % THD1, % THDE and  $\% V_{Hmax}$  .

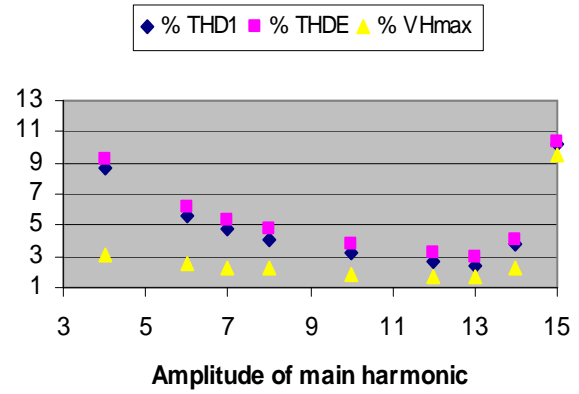


Fig.4 The values of % THD1, % THDE and % VHmax against  $V_1'$

It is observed that for all output voltage amplitudes between 8 and 14 the values of % THDE and % VHmax are less than 5% and 3% respectively, which agree with the IEEE standards for voltage distortion limits for output voltages  $\leq 69$  kv

Some results obtained from the detailed solution of the model at  $V_1' = 14$  and 8 are given next.

For  $V_1' = 14$ , the obtained values are  $V_1 = 13.72$ , %THD1 =3.74 %, %THDE = 4.05 % and  $\% VHmax = 2.27$ . Fig. 5 shows the obtained values of  $X_l$ . Table 1 shows the corresponding switching angles over the whole quarter cycle time interval of  $X_l$  , giving the starting subinterval of each switching interval, the corresponding switching angle and the output voltage (value of  $X_l$ ) over each interval that must be deduced by switching positively or negatively the inverter H-bridges dc sources  $E_1 = E$ ,  $E_2 = 3E$  and  $E_3 = 9E$ .

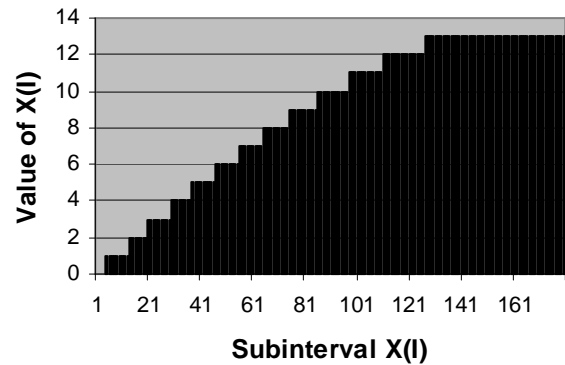


Fig. 5 Values of  $X_l$  that gives  $V_1 = 13.72$

Table 1 The switching angles corresponding to  $X_1$  of Fig.5

Starting subint.	Switching angle	$X_1$ value
5	$2^\circ$	$E = E_1$
14	$6.5^\circ$	$2E = E_2 - E_1$
21	$10^\circ$	$3E = E_2$
30	$14.5^\circ$	$4E = E_2 + E_1$
38	$18.5^\circ$	$5E = E_3 - E_2 - E_1$
47	$23^\circ$	$6E = E_3 - E_2$
56	$27.5^\circ$	$7E = E_3 - E_2 + E_1$
65	$32^\circ$	$8E = E_3 - E_1$
75	$37^\circ$	$9E = E_3$
86	$42.5^\circ$	$10E = E_3 + E_1$
97	$48^\circ$	$11E = E_3 + E_2 - E_1$
111	$55^\circ$	$12E = E_3 + E_2$
127	$63^\circ$	$13E = E_3 + E_2 + E_1$

Fig.6 shows the obtained percentage values of the harmonics relative the main harmonic from the 3<sup>rd</sup> till the 99th harmonic and 2% of the main harmonic.

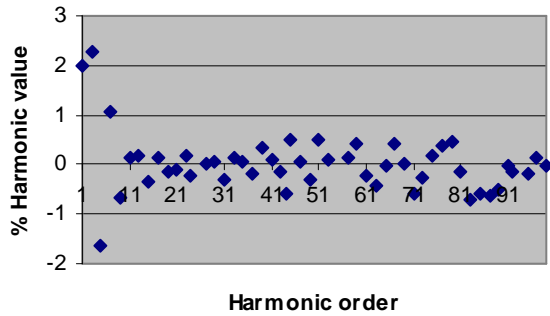


Fig. 6 % Values of harmonics for  $V_1 = 13.72$

It is noted that if a simple low pass filter is put at the inverter output that reduces the values of the 3<sup>rd</sup>, 5<sup>th</sup> and 7<sup>th</sup> harmonics then the values of %THDE and %VHmax will be less than 2.5% and 1.5% respectively, which agree with IEEE standards for voltage distortion limits for output voltages  $\leq 161$  kv ,

For  $V_1' = 8$ , the obtained values are  $V_1 = 8.15$ , %THD1 = 4.13 %, %THDE = 4.70 % and % VHmax = 2.24. Fig. 7 shows the obtained values of  $X_1$ . The corresponding eight switching angles are  $3.5^\circ$ ,  $10.5^\circ$ ,  $18^\circ$ ,  $25.5^\circ$ ,  $33.5^\circ$ ,  $42.5^\circ$ ,  $53^\circ$  and  $67^\circ$ , and the corresponding dc sources values from  $E$  to  $8E$  are obtained in a similar way as shown in table 1.

Fig.8 shows the obtained percentage values of the harmonics relative to the main harmonic from the 3<sup>rd</sup> till the 99th harmonic and 2% of the main harmonic.

Similar results could be obtained when solving the model at any value of the output voltage  $V_1$  between 8 and 14. Noting that the values of  $V_1$  are normalized with respect to the dc voltage  $E$ .

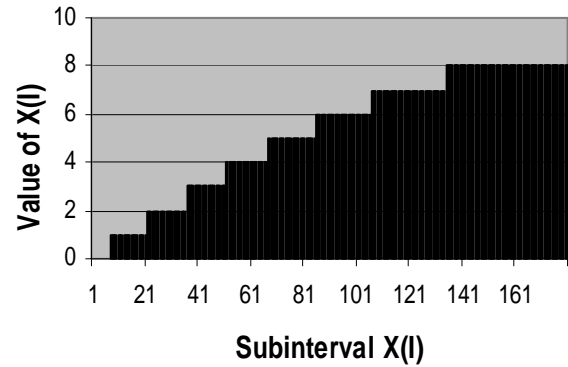


Fig. 7 Values of  $X_1$  that gives  $V_1 = 8.15$

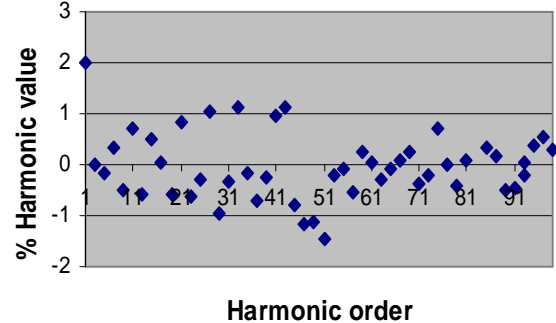


Fig. 8 % Values of harmonics for  $V_1 = 8.15$

## 6. Solution of the model for a three phase CMLI

In a balanced three phase operation the triplen odd harmonics, i.e. the 3<sup>rd</sup>, 9<sup>th</sup>, 15<sup>th</sup>, ..and so on, are self cancelled in the output line voltage assuming a star connected three phase inverter. The procedure carried out in section V with single phase 27-level CMLI is repeated with excluding the triplen odd harmonics ,and using the expression given in (3.6) for the THDE.

The model is solved for values of  $V_1'$  between 4 and 16, normalized with respect to the reference dc

voltage  $E$ . Figure 9 shows the obtained corresponding values of % THD1, % THDE and %  $V_{Hmax}$

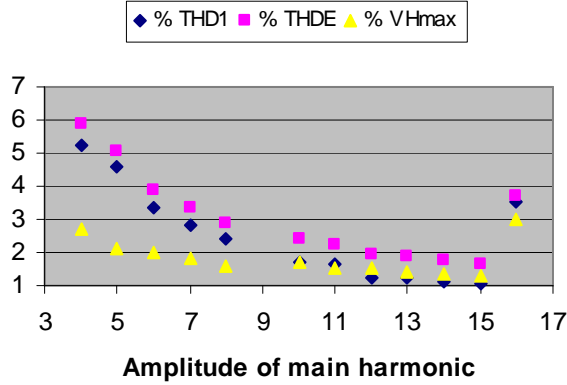


Fig. 9 The values of % THD1, THDE and % VHmax against  $V_1'$

It is observed that for all output voltage amplitudes between 10 and 15 the values of % THDE and % VHmax are less than 2.5% and 1.5% respectively, which agree with the IEEE standards for voltage distortion limits for output voltages  $\leq 161$  kv, and for all output voltage amplitudes between 5 and 10 the values of % THDE and % VHmax are less than 5% and 3% respectively, which agree with the IEEE standards for voltage distortion limits for output voltages  $\leq 69$  kv,

Some results obtained from the detailed solution of the model at  $V_1' = 15, 10$  and 5 are given next.

For  $V_1' = 15$ , the obtained values are  $V_1 = 15.0$ , %THD1 = 1.06 %, %THDE = 1.65 % and % VHmax = 1.27. Fig. 10 shows the obtained values of  $X_l$ . The corresponding switching angles over the whole quarter cycle time interval of  $X_l$  are  $1.5^\circ, 4^\circ, 6.5^\circ, 9^\circ, 13^\circ, 15.5^\circ, 18^\circ, 22^\circ, 26.5^\circ, 31^\circ, 35.5^\circ, 40^\circ$  and  $49^\circ$ . The corresponding dc sources values from E to 13E are obtained in a similar way as shown in table 1.

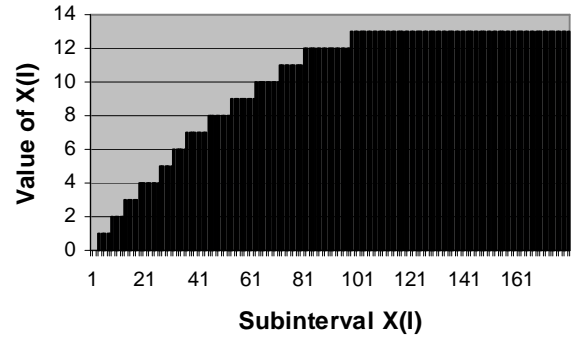


Fig. 10 Values of  $X_l$  that gives  $V_1 = 15$

Figure 11 shows the obtained percentage values of the harmonics relative the main harmonic from the 5<sup>th</sup> till the 97<sup>th</sup> harmonic and 2% of the main harmonic, excluding the triplen harmonics..

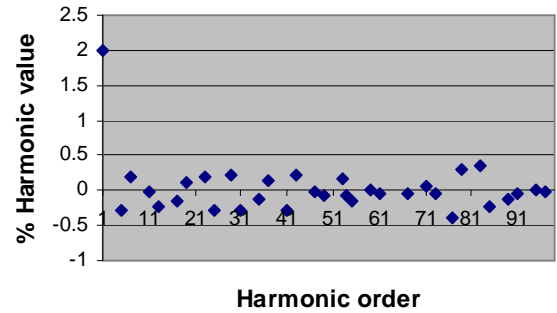


Fig. 11 % Values of harmonics for  $V_1 = 15$

For  $V_1' = 10$ , the obtained values are  $V_1 = 9.86$ , %THD1 = 1.70 %, %THDE = 2.42 % and % VHmax = 1.72. Fig. 12 shows the obtained values of  $X_l$ . The corresponding switching angles over the whole quarter cycle time interval of  $X_l$  are  $18^\circ, 22^\circ, 31.5^\circ, 35^\circ, 45.5^\circ, 49^\circ, 52.5^\circ, 56^\circ, 60^\circ, 64^\circ, 67.5^\circ, 71^\circ$  and  $88.5^\circ$ . The corresponding dc sources values from E to 13E are obtained in a similar way as shown in table 1.

Figure 13 shows the obtained percentage values of the harmonics relative the main harmonic from the 5<sup>th</sup> till the 97<sup>th</sup> harmonic and 2% of the main harmonic, excluding the triplen harmonics..

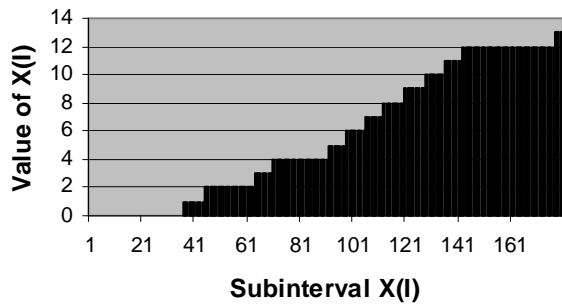


Fig. 12 Values of  $X_I$  that gives  $V_1 = 9.86$

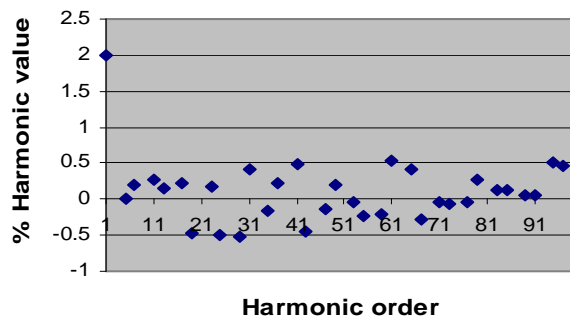


Fig. 13 % Values of harmonics for  $V_1 = 9.86$

For  $V_1' = 5$ , the obtained values are  $V_1 = 5.01$ , %THD1 = 4.58 %, %THDE = 5.04 % and % VHmax = 2.12. Fig. 14 shows the obtained values of  $X_I$ . The corresponding seven switching angles over the whole quarter cycle time interval of  $X_I$  are  $7.5^\circ$ ,  $32.5^\circ$ ,  $40.5^\circ$ ,  $47^\circ$ ,  $60^\circ$ ,  $79.5^\circ$  and  $87.5^\circ$ . The corresponding dc sources values from  $E$  to  $7E$  are obtained in a similar way as shown in table 1.

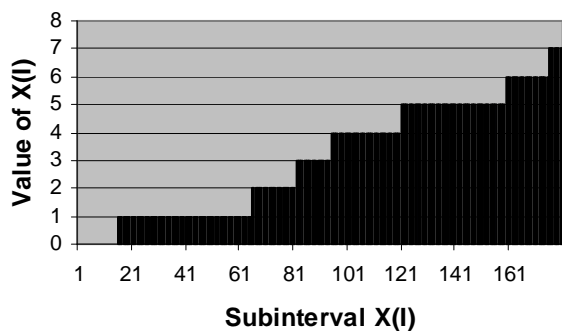


Fig. 14 Values of  $X_I$  that gives  $V_1 = 5.01$

Figure 15 shows the obtained percentage values of the harmonics relative the main harmonic from

the 5<sup>th</sup> till the 97<sup>th</sup> harmonic and 2% of the main harmonic, excluding the triplen harmonics..

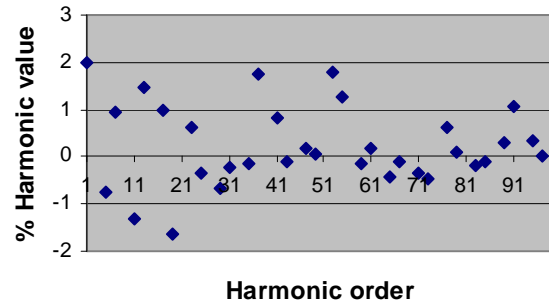


Fig. 15 % Values of harmonics for  $V_1 = 5.01$

Similar results could be obtained when solving the model at any value of the output voltage  $V_1$  between 8 and 14. Noting that the values of  $V_1$  are normalized with respect to the dc voltage  $E$ .

## 7. Conclusions

This paper introduces a general approach for obtaining the switching angles of the power switches of symmetric or asymmetric uniform step 27-level CMLs that minimize the %THDE using a mixed integer nonlinear programming (MINLP) model.. Using MINLP for this problem has many advantages over other methods given in the literature, and specially of being suitable for CMLs with large number of levels. This approach applies special expressions for calculating the THDE for single phase and three phase 27- level CMLs, and is solved for different values of the amplitude of the output voltage .

It is noted that for single phase case the values of %THDE and %VHmax are less than 5% and 3% respectively for all output voltages between  $8E$  and  $14E$ , where  $E$  is a reference dc voltage, which agree with the IEEE standards 519-1992 for voltage distortion limits for voltages  $\leq 69$  kv. While For three phase case the values of %THDE and %VHmax are less than 2.5% and 1.5% respectively for all output voltages between  $10E$  and  $15E$ , which agree with the IEEE standards 519-1992 for voltage distortion limits for voltages  $\leq 161$  kv, and less than 5% and 3% respectively for all output voltages between  $5E$  and  $10E$ , which agree with the IEEE standards 519-1992 for voltage distortion limits for voltages  $\leq 69$  kv



It should be noted that the proposed approach could be applied for symmetric or uniform step asymmetric CMLIs. A 27-level symmetric CMLI needs 13 series connected H-bridges per phase, with equal dc sources. The corresponding asymmetric CMLI needs only 3 series connected H-bridges per phase. This will be at the cost of more switching losses, but this does not represent a serious problem with the recent development of power semiconductor switches with low switching losses. In addition, asymmetric CMLIs need semiconductor power switches with higher voltage ratings, and thus are more suitable for medium voltage applications, while symmetric CMLIs are more suitable for high voltage applications, [1].

In all the cases discussed the applied MILP model assumes dividing the quarter time cycle of the main harmonic in  $N=180$  subintervals to obtain reasonable results. Accordingly, the applied MLNLP model contains 180 variables which are considered integer and nonlinear. The solution for most cases consumes very large time on a usual personal computer to obtain an exact global optimum solution. However it was observed that a feasible solution with stable fixed value of the objective function of the model was achieved in less than 50 minutes in all cases, so the maximum solution time was limited in all cases by one hour. There is no proof that the solutions obtained are the global optimal solutions, but they are at least solutions close to the optimum ones. These solutions are that given in this paper, and they show good results.

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