UTILIZTION OF XILINX FPGA BUILT-IN ANALOG-TO-DIGITAL CONVERTER FOR DATA ACQUISITION IN POWR ELECTRONICS CONVERTER

Chuen Ling TOH **Lars E. NORUM**
Norwegian University of Science and Technology, Norway
chuenling@uniten.edu.my lars.norum@ntnu.no

Abstract: *Power Electronics Multilevel Converters require a large number of high speed current and voltage measurements. In this work, we are utilizing the Xilinx FPGA internal built-in Analog-to-Digital Converter for this purpose. To increase the total number of available analog inputs, an external multiplexer is used. Therefore, an XADC external multiplexer controller is proposed to rotate these analog inputs for conversion. Additionally, this controller will coordinate data storage for each data conversion. The feasibility of the proposed XADC external multiplexer controller is evaluated experimentally.*

Key words: *Xilinx Analog-to-Digital Converter (XADC), Power Electronics Converter, Xilinx Zynq-7000 EPP.*

1. Introduction

To control the flow of energy in future power systems, Power Electronic Converters will play an important role [1]. As shown in Fig. 1 (a), the output voltage and/or current of the power converter will normally be fed back through a controller. Hence, some high-speed data converters are required. In recent years, the conventional 2-level power converter is being supplanted by multilevel power converter to meet the demand in medium voltage (≥ 1 kV) and high voltage (≥ 132 kV) applications [2], [3].

The main advantage of multilevel power converter is to use low voltage (240V–415V) power semiconductors to enable higher voltage operation. Fig. 1 (b) shows a power circuit topology of a multilevel converter, named as Modular Multilevel Converter (MMC). Modular Multilevel Converter may contain a large number of Sub-Modules (SM). In this example, the Modular Multilevel Converter is configured with six units of Sub-Modules per phase. All Sub-Modules are identical. Each of them may consist of two power switches as illustrated in Fig. 1 (c). Fig. 1 (d) shows an example of three possible generated output voltages from a multilevel converter. The goal is to synthesize sinusoidal output voltage with many staircase steps. This helps to lower the total harmonic distortion at the ac terminal. However, the demand of sensors, ADCs and IO ports for multilevel converter increases proportionally to the expansion of voltage steps.

Digital Signal Processor (DSP) and FPGA have been widely used to implement the control functions in power electronics system [4]. Data conversion circuits are normally assembled on a DSP board [5]. In recent years, advanced FPGAs with built-in ADC have also been introduced [6], [7]. Most of the design support approximately 16 to 18 channels of analog inputs. However, the available analog inputs will become insufficient. For instance, the multilevel converter shown in Fig. 1 (b) has required eighteen analog input channels for acquiring each sub-module capacitor voltage level. The required number of input channels increases

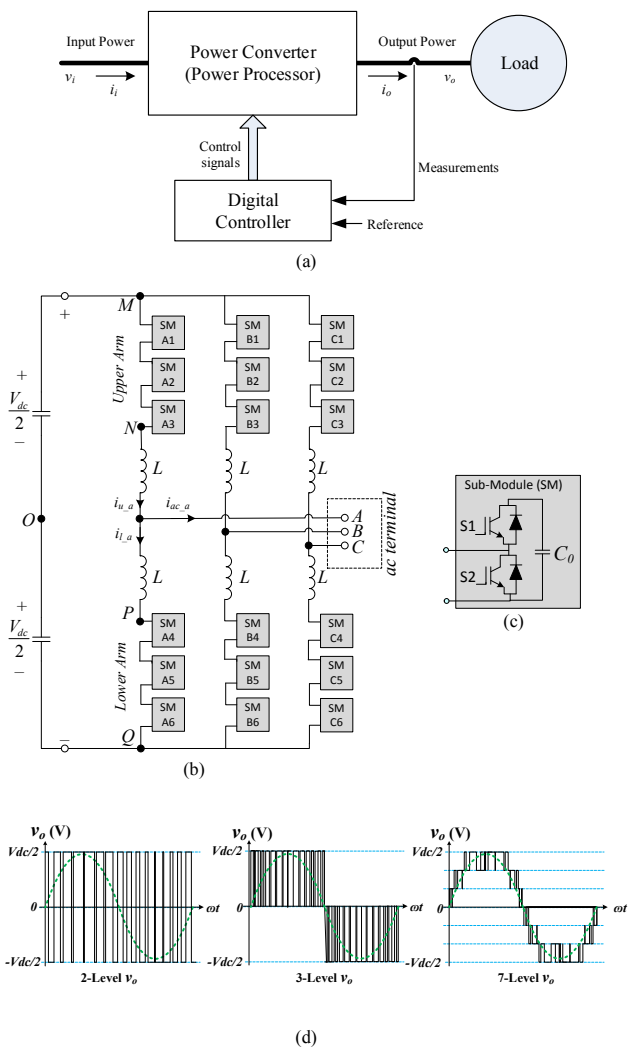

Fig. 1. (a) Block diagram of power electronics system [1]; (b) Power circuit of a multilevel converter named as Modular Multilevel Converter (MMC); (c) Power switches configured in half-bridge configuration in each Sub-Module (SM); (d) Single phase output voltage waveforms generated by power electronics converter in 2-level, 3-level and 7-level.

proportionally to the total number of sub-module employed in this converter.

This paper will focus on implementing the Xilinx built-in Analog-to-Digital Converter (XADC) for analog data conversion. The aim is to expand the number of analog input channels which are highly demanded in multilevel converter applications. An external multiplexer is implemented to expand the number of existing input channels which are offered by the FPGA. In addition, a controller is designed to ensure Round-Robin scheduling among these external input channels. This controller is also responsible to coordinate data storing (conversion results) based on its respective address. The feasibility of the proposed design will be evaluated using one phase of a small scale Modular Multilevel Converter as shown in Fig. 1 (b).

The remaining paper is organized as follows: Section II gives an overview of the Modular Multilevel Converter. The capacitor voltage balancing control with Level Shifted Pulse Width Modulation strategies are implemented. Section III proposed an external multiplexer control circuit to increase the number of available analog inputs channel for XADC. The design is validated through an implementation of a small scale Modular Multilevel Converter in Section IV. All experiment results will be presented.

2. Modular Multilevel Converter (MMC)

As shown in Fig. 1 (b), each phase leg of Modular Multilevel Converter consists of two arms. Each arm contains a number of identical Sub-Modules, *SM*, and an arm inductor, *L*. The ac terminal of the phase is located at the midpoint of the upper and lower arms. To ensure an equal number of positive and negative voltage levels being generated at the ac side, both arms should employ equal number of sub-modules. A unit of sub-module can be considered to be a controllable voltage source. It will either switch to 0V or the full voltage of capacitor, V_c. The power semiconductor which is connected in half-bridge configuration can be triggered in three different switching states. A detail description can be found in [8]. The arm current direction decides to charge or discharge the capacitor when a sub-module is inserted [9], [10]. The ac output voltage is controlled by inserting or bypassing units of V_c. by neglecting the voltage drop across the arm inductors, the output voltage, v_{AO}, is given as:

$$v_{AO}(t) = v_{NM}(t) + \frac{V_{dc}}{2} = v_{PQ}(t) - \frac{V_{dc}}{2} \quad (1)$$

This paper will implement capacitor voltage balancing control with Level-Shifted Pulse Width Modulation (LSPWM) [9], [11], [12]. A brief review on these control and modulation methods will be given using phase-a of the Modular Multilevel Converter shown in Fig. 1 (b).

LSPWM requires a pair of 180° phase shifted sinusoidal waves and six carrier waves (in phase). LSPWM performs arm's based modulation as highlighted in Fig. 2. Sub-modules on each arm are controlled individually by a modulating wave. These sinusoidal waves are commonly known as upper and lower modulating signals, v_{mod_up} and v_{mod_low}. Each of them will be compared with three units of triangular waves to obtain three specified duty cycles (gating signals). The distribution of theses duty cycles mainly depends on the

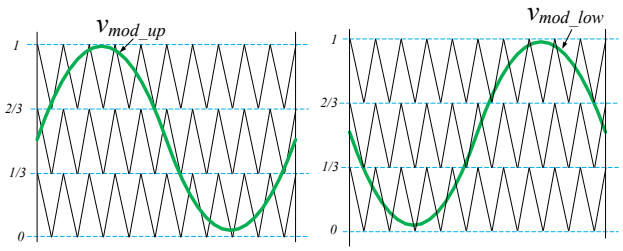

Fig. 2. LSPWM modulation for upper and lower arms' capacitor voltage balancing control.

The capacitor voltage balancing control is also executed independently on each arm. All input data will be read once in every 250 µs. These data include capacitor voltage measurements (V_c) and arm currents direction (i_{arm}). Sorting algorithm will first sort V_c in descending order. If positive arm current is measured, the longest duty cycle will be assigned to the sub-module which is then ranked at the bottom of the list (sub-module with the lowest V_c level). This action will charge up the capacitor in that particular sub-module. However, if negative arm current is sampled for the same sub-module (lowest V_c level), the shortest duty cycle must be assigned. This will help to minimize the discharging event occurred in that capacitor. Inaccurate data sampling will cause the MMC fails to operate.

In this paper, the capacitor voltage measurements will be converted using the built-in Xilinx Analog-to-Digital Converter (XADC). XADC comprises two units of 12-bit ADC. Each of them achieves 1 Mega Sample per Second (MSPS). Although XADC reserves seventeen pairs of differential input pins for analog signal conversion [7]. An external multiplexer circuit is designed mainly for the aim to serve complex MMC with a greater number of sub-modules.

3. XADC External Multiplexer Controller Design

Fig. 3 shows an implementation of a 8:1 external multiplexer to Xilinx Zynq XC7Z020 programmable logic. Eight additional analog inputs ($V_{exP[7:0]}/V_{exN[7:0]}$) can be connected to a dedicated channel (V_P/V_N) via XADC header J40 [13], [14]. Three functional logic modules are configured in the programmable logic. They are MMC Controller, XADC and XADC external multiplexer controller (XADC_exmux _ctrl). Level-Shifted Pulse Width Modulation and capacitor voltage balancing control logic designed are wrapped up in the Modular Multilevel Converter controller. XADC can be instantiated using Vivado Design Suite and customized with

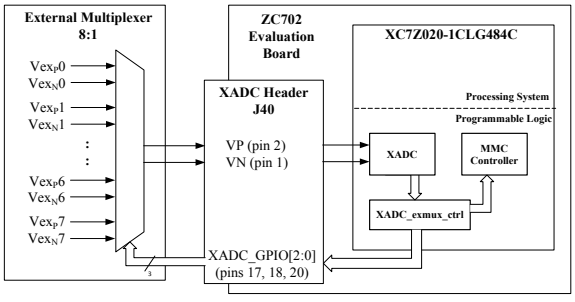

Fig. 3. Block Diagram of a 8:1 external multiplexer connected to ZC702 evaluation board via XADC header J40

the parameters given in Table 1. With this setting, the XADC will alternately switch between two channels for data conversion. Die temperature will be sampled periodically for triggering the over temperature alarm if it exceeds 125°C [7]. Conversely, the capacitor voltage measurements will be sequentially fed in for conversion process using the dedicated channel (V_P/V_N). By default, the converted data of die temperature is kept in status register 00_H while the dedicated channel stores its data at register 03_H.

Since eight additional analog inputs are connected through the dedicated channel, the converted data must be diverted to other registers before it is overwrote. Therefore, the XADC external multiplexer controller is proposed with two main aims. Firstly, it is responsible to generate external multiplexer address to select an analog input (V_{exP_i}/V_{exN_i}) for conversion. The simple Round-Robin scheduling will be employed to ensure its fairness. Secondly, it also has to coordinate data storage wisely. The following sub-session will first review the timing requirements for continuous sampling mode follows by the discussion of the controller design.

3.1 Continuous Sampling Mode Timing

As shown in Table 1, XADC is configured as channel sequencer mode which means die temperature and dedicated channel will take turn for data acquisition repeatedly. The conversion process is divided into two phases; i.e. acquisition and conversion phases. It achieves faster sampling rate mainly due to the separate Track-and-Hold amplifier. XADC will start acquiring the voltage for the subsequent channel while the current conversion is being processed. Fig. 4 (a) illustrates the continuous sampling mode timing diagram. Assume that N^{th} sample is carried out on dedicated channel with the external multiplexer selecting an additional analog input, (V_{exi}), for conversion. The acquisition of die temperature (N^{th}+1) sample starts eight ADCCLK clock after the N^{th} conversion has taken place [7]. Signal *MUXADDR* indicates the channel which is being acquired.

Table 1
XADC Setup Parameters

Interface Options	DRP
Startup Channel Selection	Channel Sequencer
Timing Mode	Continuous Mode
DRP Timing Options • DCLK Frequency • ADC Conversion Rate	 150 MHz 1000 KSPS
External Multiplexer	Enable
Channel for External MUX	VP/VN
Channel Sequencer • Channel enable • Transfer characteristic	 Die Temperature, V_P/V_N Unipolar

On the rising edge of *BUSY* signal, new data sampling will be initiated. XADC performs data conversion in approximately twenty-one ADCCLK clock cycle. The conversion result is ready on the falling edge of *BUSY*. The *BUSY* signal will tie to LOW for another four ADCCLK cycles to transfer the conversion result into the correspondent status register. The address of status register which is being written is denoted by *CHANNEL* address bus. Finally the End-Of-Conversion (*EOC*) pulse will be triggered to complete the process. The 16-bit converted data, *DO* turns valid on the data bus when data ready signal, *DRDY* rises.

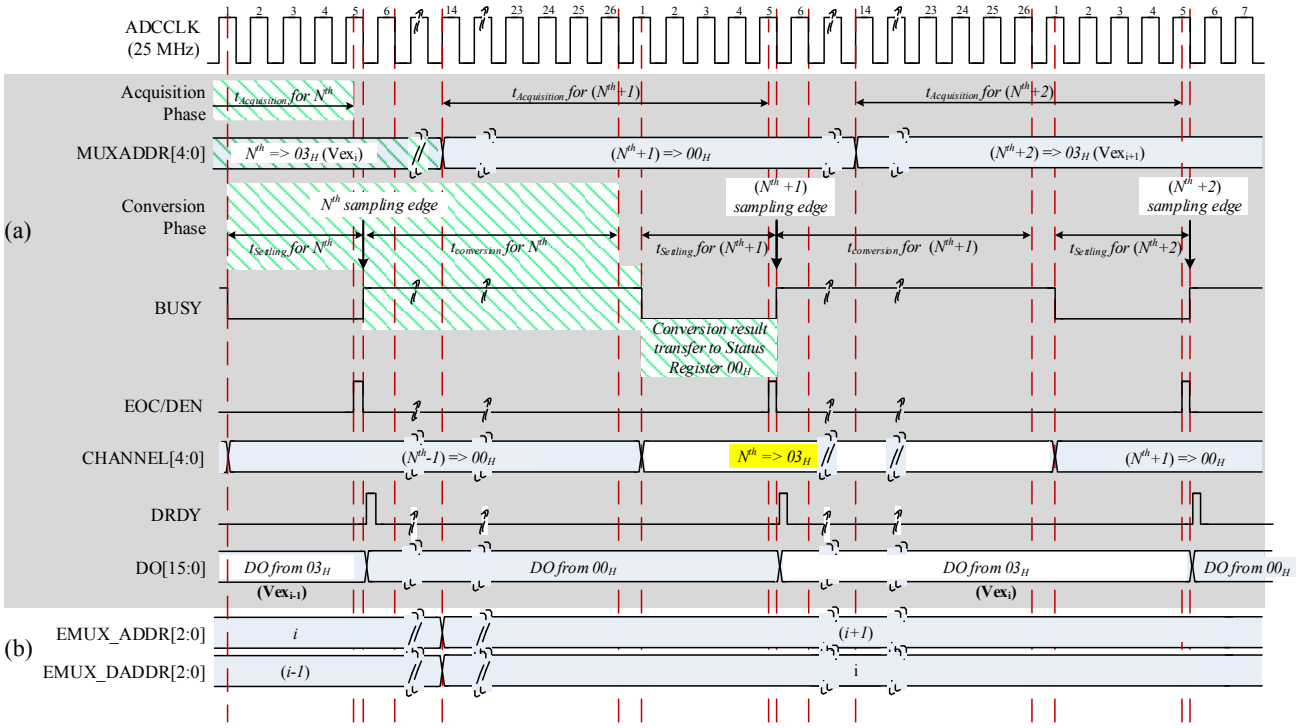

Fig. 4. Timing diagram (a) External multiplexer with continuous sampling mode; (b) proposed external multiplexer channel updates

Fig. 4 (b) shows two address bus generated by the proposed external multiplexer controller. External Multiplexer Address bus (*EMUX_ADDR*) is responsible to select one of the analog inputs for conversion. Since eight units of analog input use identical channel for conversion, another signal name as External Multiplexer Data Address bus (*EMUX_DADDR*) is produced to read out the corresponding conversion data specifically.

3.2 XADC External Multiplexer Controller Design

Fig. 5 (a) illustrates the signal interfaces between XADC and the proposed controller block (*XADC_emux_ctrl*). Signal *MUXADDR* is used to control the address variations for the external multiplexer. On the other hand, the data ready signal (*DRDY*), *CHANNEL* address bus and the 16 bit output data bus are used for the dedicated channel data storage.

The capacitor voltage measurements of each sub-module will be sampled in Round-Robbin scheduling based on the address generated from the external multiplexer controller. A Finite-State-Machine shown in Fig. 5 (b) is designed for this purpose. This Finite-State-Machine closely monitor the *MUXADDR* signal sent from XADC module and generate the appropriate external multiplexer address (*EMUX_ADDR*). After the system is out of reset, the Finite-State-Machine will enter State *S0*. When *MUXADDR* bus indicates the acquisition phase of die temperature is initiated, it will transition to State *S1* (MUXADDR = 00_H). An increment of the external multiplexer address will be executed. A simple three bits counter is used to rotate the external multiplexer address from 0 to 7 repeatedly. This Finite-State-Machine will transfer back to State *S0* at the beginning of the acquisition phase of dedicated channel (MUXADDR = 03_H).

The output signal of this Finite-State-Machine, which named as External Multiplexer Address (*EMUX_ADDR*), will be used to generate the External Multiplexer Data Address (*EMUX_DADDR*). *EMUX_DADDR* is formulated as follows:

$$EMUX\_DADDR = EMUX\_ADDR - 1 \qquad (2)$$

with this information the conversion data can be read out accordingly. Equation (3) and (4) formulate the enable conditions for eight external multiplexer analog inputs ($V_{exP[7:0]}/V_{exN[7:0]}$) and die temperature.

$$Vex_{i\_en} = DRDY \ \textbf{AND} \ (CHANNEL == 03_H) \ \textbf{AND} \ (EMUX\_DADDR == i) \qquad (3)$$

$$temp_{en} = DRDY \ \textbf{AND} \ (CHANNEL == 00_H) \qquad (4)$$

where i varies from 0 to 7. Channel 03_H indicates the dedicated channel whereas the die temperature channel is represented by 00_H.

The proposed controller reserves nine individual registers for storing the data. These registers are controlled separately with the above mentioned enable signals. For instance eight registers (*Vexi_DO*) are reserved for the external analog inputs data conversion. Likewise, the die temperature conversion result which appears on data bus *DO* will be stored in the register *Temp_DO* when *DRDY* pulse asserts with the *CHANNEL* address gives 00_H. Although 16-bit conversion results are always produced from XADC, the 12 MSBs (most significant bits) represents the valid data [7].

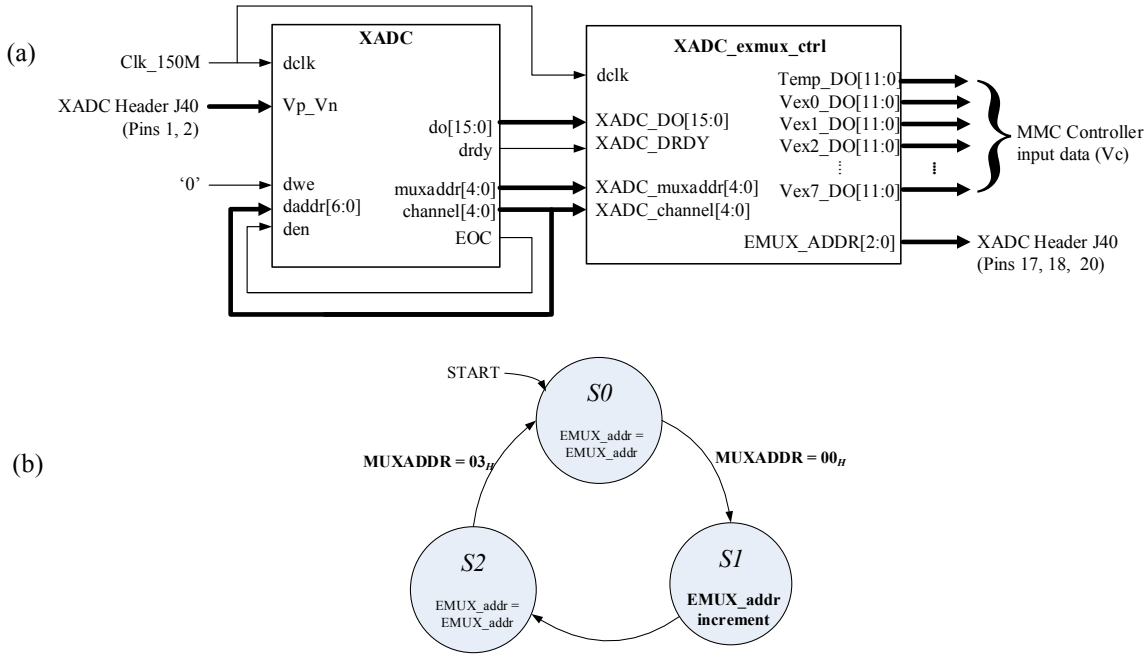

Fig. 5. (a) Functional block diagram of XADC wizard and the proposed XADC external multiplexer controller, (b) *XADC_emux_ctrl* Finite State Machine

4. Experimental Results

The feasibility of the proposed controller will be evaluated through a small scale Modular Multilevel Converter (MMC) prototype as shown in Fig. 6. This experiment is conducted using one phase. The MMC's parameters are given in Table 2. Xilinx Zynq-7000 EPP ZC702 evaluation board is implemented as the master controller board. An analog multiplexer, ADG507A is assembled on XADC External Multiplexer board. ADG507A provides eight analog channels with sixteen differential pins. This device requires approximately 600 ns transition time to switch from channel to channel [15]. Thus the proposed solution does not increase the acquisition time even through the capacitor voltage acquisitions are alternated with the conversion of die temperature.

In this setup, six pairs of differential pins are used. For instance, the capacitor voltage, V_c, of Sub-Module (SM) A1 is connected to V_{ex0}. V_{ex0} indicates differential pair of V_{exP0}/V_{exN0}. Fig. 6 shows the rest of the input channels allocation for other Sub-Modules. Arms currents are measured and sampled simultaneously using standalone hardware. The digital data will be sent in directly via Xilinx FPGA Mezzanine Card XM105 Debug card. Besides, switching commands are also distributed directly from this card.

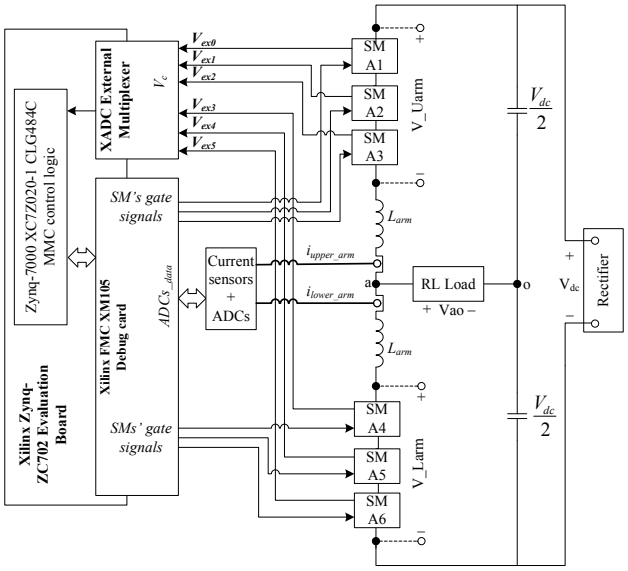

Fig. 6. Modular Multilevel Converter (one phase) experimental setup

Table 2
Parameters of the Modular Multilevel Converter Setup

Rated power	500 W
Number of SMs per arm	3 units
SM's capacitance	6800 µF, 100 V
Arm inductance	1.3 mH
DC Link Voltage	10 V
DC link Capacitor	3300 µF, 450 V
RL Load	R = 5 Ω, L = 8mH
Number of output voltage levels	7
Switching frequency	2 kHz

Fig. 7 shows that a sampling event occurs at t_{C0} when the *BUSY* signal arises. This sampling event is referring to dedicated channel with the external multiplexer selecting the capacitor voltage measurement of sub-module A2 for conversion (*MUXADDR* = 3 and *EMUX_addr* = "001"). At t_{C1}, the conversion is completed with the conversion result written to the status register 3 (*CHANNEL* = 3). The data ready signal, *DRDY*, pulses at t_{C2}, indicates valid output data is now available on *XADC_DO* data bus. The proposed controller triggered on *Vex1_en* as the condition in (3) is fulfilled. Therefore, the data is latched into register *Vex1_DO* as shown in Fig. 8.

New acquisition phase is always initiated on subsequent channel. It starts approximately 320 ns after a conversion has begun. Referring back to Fig. 7, the *MUXADDR* bus changes to 0 at t_{A0} which indicates XADC starts acquiring die temperature channel although the BUSY signal is still holding high for the conversion of capacitor voltage measurement from sub-module A2. The proposed controller will update a new address to the external multiplexer at this instance. This ensures the hardware reserves enough transitional time to switch from analog input V_{ex1} to V_{ex2}.

Fig. 9 proves that XADC only switches between two channels for conversion. The *CHANNEL* address bus always alternates between channel 0 (die temperature) and 3 (dedicated channel which is used to acquire capacitor voltage measurements from six units of su-module). The proposed controller has successfully implemented Round-Robin scheduling to rotate the external multiplexer channels in ascending order. It also manages to produce corresponding enable signals based on (3) and (4). These signals are responsible to latch the conversion data from status registers. Each sub-module's capacitor voltages will be periodically updated every 16 µs.

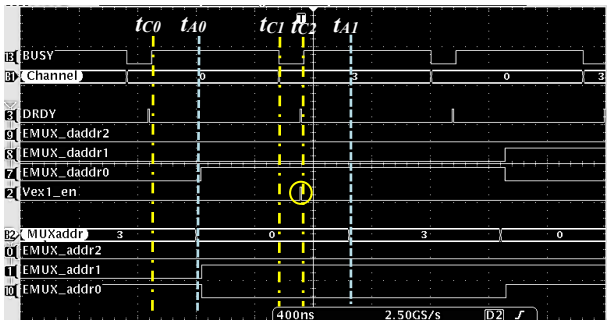

Fig. 7. The proposed controller triggers Vex1_en for data storage

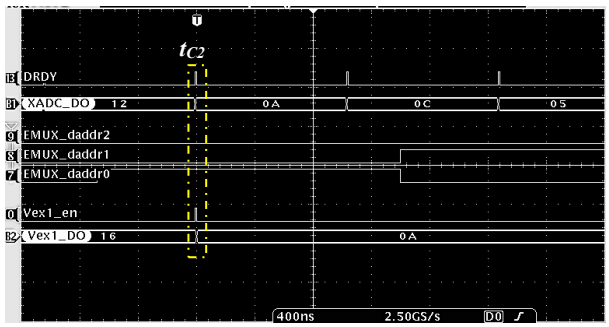

Fig. 8. The converted result is kept into register *Vex1_DO*

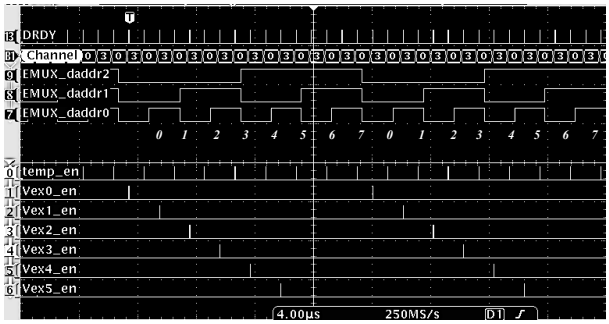

Fig. 9. The proposed controller rotates the external multiplexer address in ascending order

The feasibility of the proposed XADC external multiplexer controller is proved by the experiment results obtained from operating the Modular Multilevel Converter. Fig. 10 (a) presents the voltage waveforms produced by the converter. The balance three-level arm voltages, V_Uarm and V_Larm, demonstrate the control algorithms work correctly with precise capacitor voltages acquisition. Thus, the seven-level load voltage, Vao, is produced according to (1). Fig. 10 (b) illustrates current waveforms of the Modular Multilevel Converter. A sinusoidal load current is lagging behind the load voltage due to 8mH load inductance.

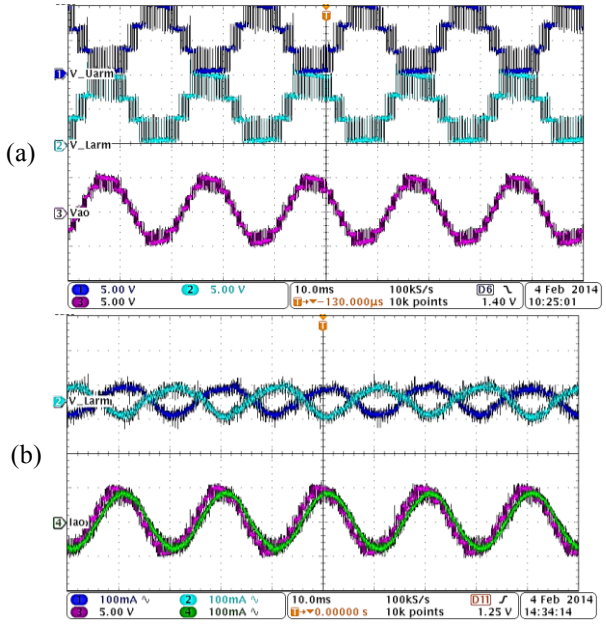

Fig. 10. (a) Upper arm voltage, V_Uarm; lower arm voltage, V_Larm; load voltage, Vao; (b) Upper arm current, I_Uarm; lower arm current, I_Larm; load voltage, Vao and load current, Iao

5. Conclusion

In this work, we have implemented an external multiplexer controller customized for Xilinx Analog-to-Digital Converter (XADC). The proposed controller provides eight additional analog input channels to XADC using an external multiplexer. These additional input channels will be selected for conversion in Round-Robin scheduling. The converted data are kept separately in a set of registers. This design is highly suitable for complex multilevel power electronics applications, which requires more input data acquisition. The feasibility of the proposed controller has been evaluated experimentally using a Modular Multilevel Converter which employs six units of sub-modules per phase. Level Shifted Pulse Width Modulation and capacitor voltage balancing control are chosen as the modulation and control schemes for this Modular Multilevel Converter. The capacitor voltage measurement from each sub-module is sent to the XADC using an external multiplexer. With the proposed external multiplexer controller, all data are updated precisely and accordingly. As a result, the Modular Multilevel Converter is operated as expected producing 7-level output voltage with a sinusoidal current wave.

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