PERFORMANCE ANALYSIS OF SYMMETRICAL AND ASYMMETRICAL CASCADED H BRIDGE INVERTER

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Abstract: *This paper presents the comparative analysis report based on the conventional cascaded H-bridge inverter with equal DC sources (symmetric) and the proposed cascaded H-bridge inverter with unequal DC sources (asymmetric). This paper also analyzes the restriction on selecting unequal DC sources. It is shown that the proposed scheme provides the more number of voltage levels with the same number of switches as in conventional cascaded multi level inverter.*

Key words: *Cascaded H-bridge multi level inverter, Unequal DC sources, Asymmetrical.*

1. INTRODUCTION

Multilevel converters are currently considered as one of the industrial solutions for high dynamic performance and power-quality demanding applications, covering a power range from 1 to 30 MW. Among the reasons for their success are the higher voltage operating capability, lower common-mode voltages, reduced voltage derivatives dv/dt stress, voltages with reduced harmonic contents, near sinusoidal currents, smaller input and output filters (if necessary), increased efficiency, and, in some cases, possible fault-tolerant operation [7][12]. These converters have the ability to synthesize output voltage waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating.

A comparative evaluation of cascaded H-bridge multi level inverter with equal DC sources and unequal DC sources in the output voltage using hybrid PWM switching method is reported.

The cascaded structure utilizes more isolated DC sources [12]. If dc voltage sources of all H-bridge cells are equal (symmetrical arrangement), the number of output phase voltage levels 'm' in a cascaded inverter is defined by m=2n+1, where 'n' is the number of separate dc sources. On the other hand, if at least one of the dc voltage sources is different of the other ones, the multilevel inverter can be called as asymmetric hybrid multilevel inverter [1]. It is possible to verify that asymmetric multilevel inverters can generate a larger number of levels with the same number of cells [4].

Applications, modulation strategies and control of multilevel inverters using H-bridge series-connected cells are presented in [1], [2], [9], and [14]. A generalized design methodology for hybrid multilevel inverter is proposed in [3], and the analysis and comparison of hybrid multilevel voltage source inverters is presented in [11]. This paper will develop the design methodology based on the design method developed in [13] for a 4.16kV/500hp three-phase induction motor. It will be demonstrated the impact of this methodology in the number of possible configurations and number of levels reached and the total harmonic distortion (THD) in the inverter output.

2. CASCADED H-BRIDGE INVERTER

Cascaded H-bridge multilevel inverter is shown in Fig. 1. The output phase voltage $V_a(t)$ is the sum of the output voltages of each cell $V_{a1}(t), V_{a2}(t), V_{an}(t)$. Where $V_{a1}(t)$ is the output of the cell with the lowest voltage and $V_{an}(t)$ with the highest voltage.

An output phase-voltage waveform is obtained by summing the bridges output voltages

$$V_{a(t)} = \quad V_{a1(t)} + V_{a2(t)} + \cdots + V_{an(t)} \qquad (1)$$

Where 'n' is the number of cascaded bridges.

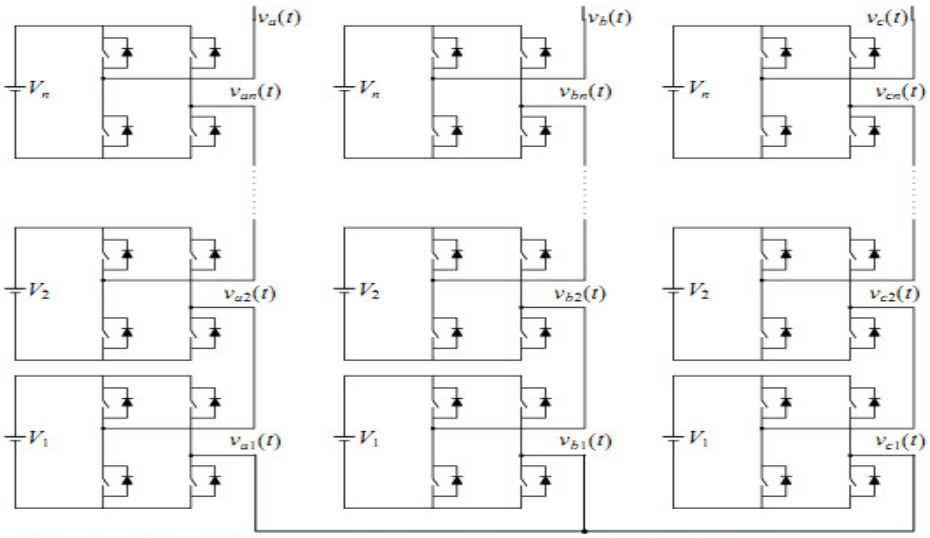


Fig. 1 – Circuit diagram of a three-phase cascaded multilevel inverter.

2.1 Restrictions to define the dc voltage sources

To define the amplitude values of the DC voltage sources, the following restrictions should be respected:

i. DC voltage sources should be arranged so that the second source is equal or higher than first, and so on;

ii. DC voltage source values must be normalized in function of the lowest source voltage, and normalized values must be natural numbers;

iii. Adjacent levels must be equally spaced;

iv. Adjacent levels must be modulated at high frequency;

v. The highest voltage cell must process power levels equal or lower than the load;

vi. Any cell cannot regenerate power.

2.2 Choosing the appropriate configuration

The steps presented in the previous section will be performed here after. The restriction (i) considers that the DC voltage sources are arranged in an increasing way, and are given by (2)[13].

$$V_1 \leq V_2 \leq V_3 \qquad (2)$$

The restriction (ii) guarantees that every DC voltage sources are multiples of V_1 , and its normalized values are given by (3)[14], being $V_{base}=V_1$.

$$V_j = \frac{V_{cc,j}}{V_{base}} \; and \; V_j \in N, \qquad j = 1,2, \dots \dots n \qquad (3)$$

The restriction (iii) is given by (3). The conditions (iii) and (iv) guarantee that every output inverter voltage levels are equally spaced [11].

$$V_j = 1 + 2\sum_{k=1}^{j-1} V_{k,} \qquad j = 2,3, \dots \dots n \qquad (4)$$

The sum of normalized values of DC sources by phase is σ_n , (5), and the number of levels is given by m (6), [11].

$$\sigma_n = \sum_{j=1}^{n} V_k \qquad (5)$$

$$m = 1 + 2\sigma_n \qquad (6)$$

Respecting the restrictions (i), (ii) and (iii), three sets of possible DC voltage sources obtained. The first is: $V_1 = 1, V_2 = 1, V_3 \leq 5$. The second is $V_1 = 1$, $V_2 = 2$, $2 \leq V_3 \leq 7$. And the third set is $V_1 = 1$, $V_2 = 3$, $3 \leq V_3 \leq 9$.

It presents a total of eighteen combinations that can be utilized, which are shown in Table I. The symmetric topology presents the lowest number of levels, 7, while the configuration 1-3-9 will present the maximum number of levels, 27.

TABLE I
Configurations for uniform adjacent levels

Candidate	V_1	V_2	V_3	m
1	**1**	**1**	**1**	**7**
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	1	5	15
6	1	2	2	11
7	1	2	3	13
8	**1**	**2**	**4**	**15**
9	1	2	5	17
10	1	2	6	19
11	1	2	7	21
12	1	3	3	15
13	1	3	4	17
14	1	3	5	19
15	1	3	6	21
16	1	3	7	23
17	1	3	8	25
18	1	3	9	27

The restriction (iv) is employed to guarantee that all levels are modulated at high frequency, (7). With this the output voltage harmonic content will be concentrated around of the switching frequency of the inverter with lowest DC voltage source [7].

$$V_j = 2\sum_{k=1}^{j-1} V_k\,, \qquad j = 2,3,\ldots..n \tag{7}$$

After to apply this restriction, the possibilities decrease from eighteen to nine alternatives, that will be divided in two subsets: first,V_1=1,V_2=1,$V_3 \leq 4$ and second, V_1=1,V_2= 2, $2 \leq V_3 \leq 6$, Table II. Providing a maximum of 19 levels for the configuration 1-2-6.

TABLE II
Configurations for uniform adjacent levels and all levels modulated at high frequency

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	2	2	11
6	1	2	3	13
7	1	2	4	15
8	1	2	5	17
9	1	2	6	19

For the next analysis, the frequency (m_f) and amplitude (m_a) modulation indexes are given by (8) and (9), [Ref.11]. Being, f_s is the switching frequency of the lowest power inverter, f_r is the frequency of the reference signal and V_{refp} is the normalized peak value of the fundamental component of the reference signal:

$$m_f = \frac{f_s}{f_r} \tag{8}$$

$$m_a = \frac{V_{refp}}{\sigma_n} \tag{9}$$

Based on restriction (v), it is guaranteed that the highest power cell doesn't process a fundamental voltage higher than the load, for all values of m_a, (10), which V_n must be a natural number smaller or equal than has been found (7), [10].

$$V_n \leq \frac{\pi}{2}\sum_{k=1}^{n-1} V_k \qquad \epsilon \quad N \tag{10}$$

The restriction (v) determines that the maximum normalized value reached for the highest DC voltage source is four, and consequently now there are seven possibilities, Table III.

TABLE III
Possible Configurations for: uniform adjacent levels, all levels modulated at high frequency, and V_3 does not process a voltage higher than load voltage.

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	1	2	9
3	1	1	3	11
4	1	1	4	13
5	1	2	2	11
6	1	2	3	13
7	1	2	4	15

The restriction (vi) establishes that none of cell can synthesize negative fundamental voltage for all excursion of m_a. Thus, uncontrolled rectifiers can be employed as front end converter. With this requirement only two configurations can be implemented, and they are presented in Table IV.

TABLE IV
Possible Configuration for: uniform adjacent levels, all levels modulated at high frequency, V_3 does not process a voltage higher than load voltage and it utilizes only uncontrolled unidirectional rectifier. Also no over modulation in the small power cell.

Candidate	V_1	V_2	V_3	m
1	1	1	1	7
2	1	2	4	15

3. ANALISIS OF TYPES 1-1-1 AND 1-2-4

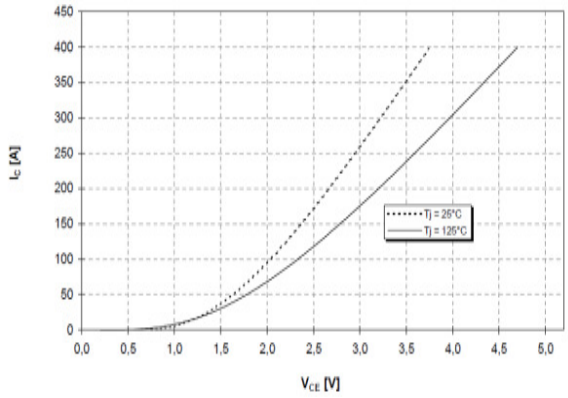
3.1 Total Harmonic Distortion

The total harmonic distortion of a signal is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency (1).

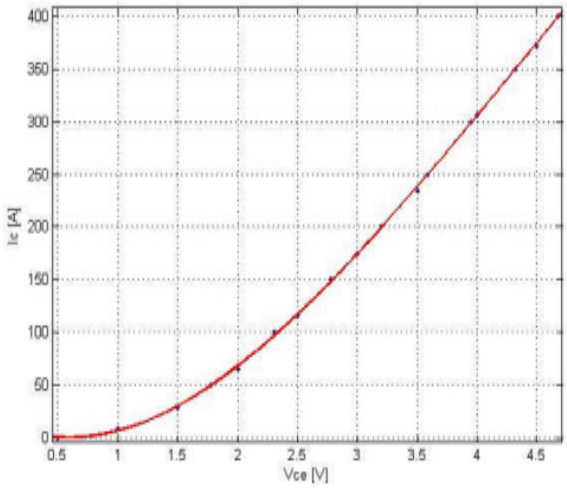
$$THD\% = \frac{100}{V_1}\sqrt{\sum_{h=2}^{\infty} V_h^2} \qquad (11)$$

3.2 Power Losses Analysis

The analysis of losses for cascaded H-bridge hybrid multilevel inverter is a complex process, due to the wide number of operation states of this converter. Moreover, this analysis becomes more difficult by using a hybrid modulation technique, because the semiconductor devices command signals and the switching frequencies are different for every cells. To derivate the losses analysis there is a need for the semiconductors devices information provided by the manufactures datasheets. Therefore, this analysis strongly depends on the power devices used. The use of components of different manufacturers can point to distinct results. The functions of V_{ce} ($i_{load}(\theta)$), $V_F(i_{load}(\theta))$, $E_{on}(i_{load}(\theta))$ and $E_{off}(i_{load}(\theta))$ are obtained from the respective data sheet. For example, Fig.2 shows the voltage-current curve of IGBT/BSM200GB170DLC (1.7KV/200A) from datasheet and its fitted curve from cftool of MATLAB are shown. This curve fitting toolbox imports the points from an actual curve and finds the simulated curve by using mathematical models to fit the points and then exports the fitted curve [13].



(a)



(b)

Fig.3. Voltage-current curve of IGBT (a) actual curve from datasheet, (b) fitted curve from cftool.

The mathematical model found from this semiconductor curves used in this work are given by,

3.2.1 IGBT/BSM200GB170DLC (EUPEC) [13]:

$$v_{ce} = \left(2.197.e^{0.001896.I_{load}} - 1.822.e^{-0.0223.I_{load}}\right)$$

$$v_F = \left(1.456.e^{0.001729.I_{load}} - 1.415.e^{-0.03326.I_{load}}\right)$$

$$E_{on} = 3.104.e^{-9}.{I_{load}}^3 - 1.878.e^{-7}.{I_{load}}^2 + 0.000358.I_{load} + 0.0007119$$

$$E_{off} = 0.0003271.I_{load} - 0.0008491$$

$$E_{rec} = 1.906.e^{-9}.{I_{load}}^3 - 1.636.e^{-6}.{I_{load}}^2 + 0.0005078.I_{load} + 0.000305$$

(12)

Based on the models for each device, the conduction and switching power losses are calculated for each semiconductor of the output inverter. The sum of all results is computed to obtain the total power losses.

Then the methodology to determine the conduction and switching losses is discussed hereinafter, where total losses is the sum of all losses (13).

$$P_{Total} = P_{cond.loss} + P_{switch.loss} \qquad (13)$$

3.2.2 Conduction Losses

Conduction losses are those that occur while the semiconductor device is conducting current. A simplified model of the solid-state device is used to determinate the conduction losses. These models are given in (14) for an IGBT and a diode, respectively [10], and [13].

$$V_{ce}(\theta) = V_{ce} + R_{ce}.|i_{load}(\theta)|$$

$$V_F(\theta) = V_F + R_F.|i_{load}(\theta)| \quad (14)$$

Where, $V_{ce}(\theta)$ and $V_F(\theta)$ are the on-state saturation voltage of the IGBT and diode, respectively, V_{ce} and V_F are the voltage drop for zero current of the IGBT and diode, respectively, R_{ce} and R_F are the equivalent resistance of the resistive components of voltage drop across the power device. $i_{load}(\theta)$ is the load current, given in (15).

$$i_{load}(\theta) = m_{a.} I_{max}(\theta - \emptyset) \quad (15)$$

Here, φ is the load power factor angle. To determine the conduction losses of the IGBT and diode the load current sense must be observed. If $i_{load}(\theta) \geq 0$, then the IGBT is conducting, otherwise the diode is conducting (16).

$$P_{cond.sw} = \frac{1}{2\pi}\int_0^{2\pi} V_{ce}(\theta).i_{load}(\theta).v_{cmd.swx}(\theta)d\theta$$

$$P_{cond.D} = \frac{1}{2\pi}\int_0^{2\pi} V_F(\theta).i_{load}(\theta).v_{cmd.swx}(\theta)d\theta \quad (16)$$

Where, $v_{cmd.swx}(\theta)$ is the command signal of the switch SWx. The total conduction losses are obtained from (17).

$$P_{Cond.loss} = P_{cond.sw} + P_{cond.D} \quad (17)$$

3.2.3 Switching Losses

The most accurate method of determining switching losses is to plot the current and voltage waveform in the controllable switch during the switching transition and multiplies the waveform point by point to get an instantaneous power waveform. The area under the power waveform is the switching energy at turn-on or turn-off [13]. However, in this paper, the turn-on, turn-off and recovery losses are calculated based on the information of the manufacturer (data sheet), turn-on energy losses per pulse ($E_{on}(i_{load}(\theta))$), turn-off energy losses per pulse ($E_{off}(i_{load}(\theta))$) and reverse recovery energy ($E_{rec}(i_{load}(\theta))$).The switching losses are obtained by identification of every instant of commutation, as at turn-on instant as turn-off instant during all reference period. Therefore, the turn-on losses, turn-off losses and reverse recovery losses are given by (18).

$$P_{turnon} = \frac{1}{2\pi}\sum E_{on}(i_{load}(\theta))$$

$$P_{turnoff} = \frac{1}{2\pi}\sum E_{off}(i_{load}(\theta))$$

$$P_{recovery} = \frac{1}{2\pi}\sum E_{rec}(i_{load}(\theta)) \quad (18)$$

The total switching losses will be the summation of turn-on, turn-off and recovery reverse losses, given by (19).

$$P_{switch.loss} = P_{turnon} + P_{turnoff} + P_{recovery} \quad (19)$$

4. SIMULATION RESULTS

A computer simulation has been created in MATLAB/Simulink and the FFT analysis is taken to compare the Total Harmonic Distortion (THD) of 7 level symmetrical and the proposed 15 level asymmetrical cascaded H bridge (CHB) inverter. For k-number of DC sources, the associated number of voltage levels equal to $2^{k+1} - 1$. Therefore the output has 15 levels for k=3. , + 7, + 6, + 5,+ 4, + 3, + 2, + 1 and 0. Steady state phase to ground voltage and its THD spectrum is shown in Fig 4.a for 7 level CHB inverter and in Fig4.b for 15 level CHB inverter.

The high number of levels generated by15 level inverter can be clearly appreciated to get nearly sinusoidal voltage waveform than7 level inverter. From the figures 4.a and 4.b it was recorded that 18.24% of THD for 7 level inverter and 11.04% of THD for 15 level inverter. Also it is noted that the output voltage of seven level inverter attains only 300V, but the output voltage of fifteen level inverter attains about 700V which increases the power output.Thus the asymmetrical multilevel inverter is used to obtain a high resolution, and to get better the efficiency and reduced harmonics.

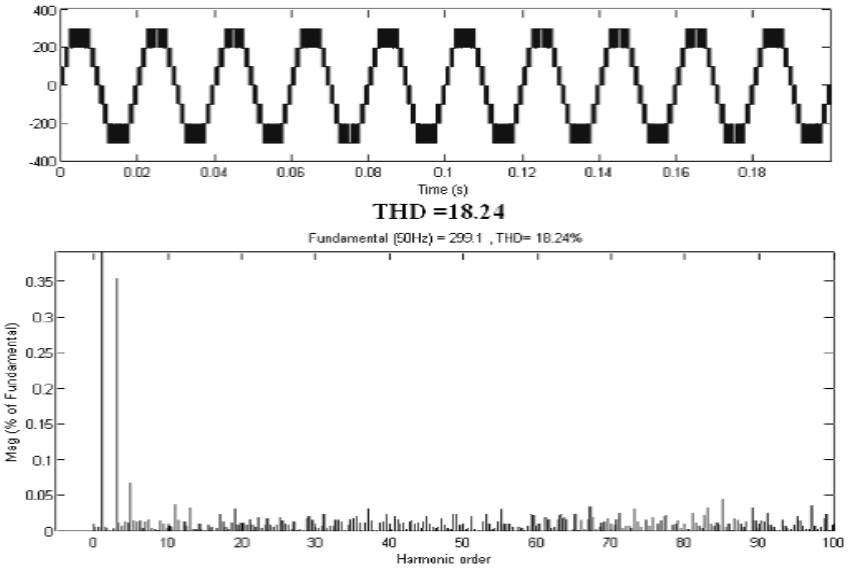


Fig.4.a. A 7 level inverter Phase voltage (V_{an}) and its THD spectrum.

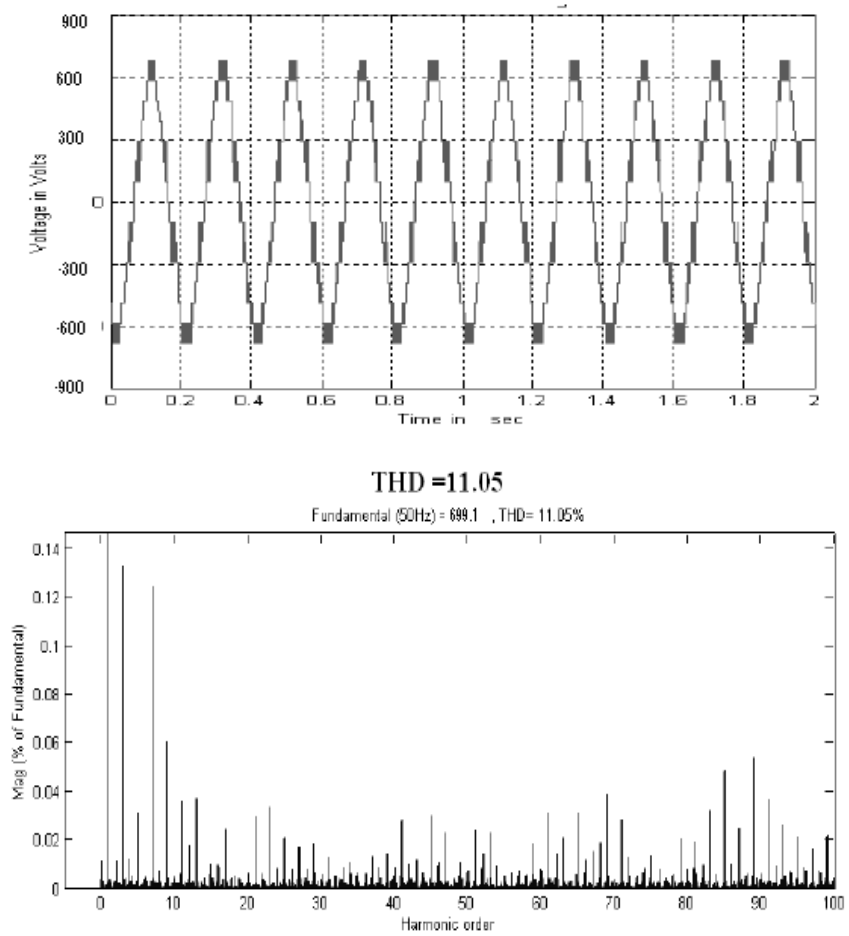


Fig.4.b. A 15 level inverter Phase to neutral voltage (V_{an}) and its THD spectrum.

Due to the effect of the hybrid modulation strategy, , the switching losses in the cells 3 and 2 are very small in comparison with the cell , because the cell 3 is commutated at the fundamental frequency of output, and the cell 2 also at low frequency and only cell 1 operates at high frequency. On the other hand, if a conventional PWM technique had been used for all cells, they would present similar switching losses.

V.CONCLUSION

This paper applies a generalized design methodology to determine the DC voltage sources of a hybrid multilevel inverter. For three cells cascaded H-bridge multilevel inverter was possible to reduce the number of configurations into two, 1-1-1 and 1-2-4. The configuration 1-2-4 synthesizes fifteen levels, while the type 1-1-1 only seven levels on output phase voltage. This difference guarantees the configuration 1-2-4 with the Total Harmonic Distortion smaller than configuration 1-1-1, This will reduce the volume of the output filter, when it is necessary. It was presented a methodology to calculate the conduction and switching losses when a hybrid modulation strategy is used. One example to determinate losses was shown. Based on every restriction presented, i.e on level numbers, Total Harmonic Distortion, and the number of semiconductors devices used, it is concluded that the configuration 1-2-4 is the recommended topology than 1-1-1, because it can produce greater number of levels with the same number of switches as in the conventional configuration 1-1-1 and thus enhances the operation of cascaded H-bridge inverter.

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