THD mitigation in various level quasi Z-source cascaded inverter by hybrid step modulation-SHEPWM method

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Abstract: *The recent increase in non-linear loads has developed its major impact in harmonics mitigation and voltage gain improvement. Wherever, conventional cascaded multilevel inverter (CMI) has its buck operation and complexity while that switching leads to further loss. This complexity can be minimized by developing a topology with the combination of quasi Z-source cascaded multilevel inverter (QZS-CMI) which can combine its benefit to boost up voltage in single stage and generate high-quality output voltage waveform with improved reliability. This is done by combination of step modulation and selective harmonic elimination (SHE) PWM. This technique has its own advantage in reducing the switching frequency and complexity of the system. This technique is applied for the different levels in QZS-CMI with respect to voltage gain improvement and reduction of total harmonic distortion (THD) to the IEEE Standard 519. To validate the simulation results this technique is implemented in hardware model of 450W/150V inverter with ARM-processor.*
Key words: *ARM-processor, CMI, Step modulation, THD, QZS.*

1. Introduction

Multilevel voltage source inverters are evolving rapidly as a new breed of power converter options for medium and high-power applications [1,2]. The three main topologies of the multilevel inverters are: diode-clamped [3], capacitor-clamped [4] and cascaded multilevel inverter (CMI) with separate DC sources [5]. Among different multilevel topologies, the cascaded inverter has been identified as a suitable topology due to its feature of single phase power conditioning and simplicity in DC link voltage regulation [6,7]. However, each module of the conventional CMI acts as a buck inverter, so it requires DC–DC boost converter added into each module [8]. Hence a two-stage inverter is required for each module. This topology involves extra power switches, inductors, power circuit and control implementation which add complications, along with increased system cost and power loss. The Z-source inverters (ZS) [9] and quasi Z -source inverter (QZS) [10] have been developed as new power converter topology due to their combined advantage of voltage buck boost capabilities and maintain constant voltage in the inverter output. The ZS/QZS has been proposed to be coupled with CMI for its medium voltage high-power generation in the recent literature [11,12,13] .This system presents high consistency because of supporting shoot-through states (non-active mode) and low cost, when compared to conventional CMI based power generation system
The modulation method is an important aspect to properly operate the QZS-CMI. Presently, there are many pulse-width modulation techniques (PWM) available for CMIs. These techniques can be generally classified into three categories; programmed PWM[14], sine wave PWM and multilevel space vector modulation (MSVM).The sine wave PWM based multi-carrier PWM (MC-PWM) can be further categorized into phase-shifted [15], phase disposition and phase opposition disposition [16,17]. The MC-PWM method need *k*-level inverter requires (*k*-1) carriers all having the same frequency and amplitude and also operating at higher switching frequency. The MSVM technique has the advantages of ideal harmonic character and high voltage utilization [18]**.** However increasing cascaded levels, the selection of space vectors and calculation of switching time becomes more complicated. To overcome these disadvantages of the above modulation scheme, step modulation with selective harmonics elimination PWM (SHEPWM) method is used in this proposed work. The step modulation [19] is especially suitable for CMI, the switching angle developed by this ideology for a multilevel inverter can produce a step waveform very much similar to a sinusoidal waveform.

Control method and circuits of this inverter based on high-volume, low-cost, low-voltage power MOSFETs is experimentally established as a possible economic alternative to an IGBT based system [20]. The microcontroller chosen for the hardware model is the existing 32-bit digital signal processor [21]. The hardware description model requires larger memory requirement for analog to digital conversion and PWM, which motivates to switch over to ARM (advanced RISC machine) processor [22]. The ARM processor has additional

advantages of real time control, fast processing, and high end communication protocol, further the system can be operated in both 32 bit and 64 bit.

This work investigates the performances of 3-level, 7-level, 15-level and 31-level QZS-CMI in terms of voltage gain, total harmonic distortion (THD), cost and the dynamic performances of connecting single phase load for satisfying IEEE standard 519 [23]. The simulated results are further verified experimentally with the ARM-processor to study the performance of the QZS-CMI with step modulation and SHEPWM technique to choose the specific level of operation to operate the system under IEEE standard.

2. Topology description.

Cascaded H-bridge (CHB) multilevel inverter is composed of a multiple units of single-phase H-bridge power cells. The H-bridge cells are usually coupled in cascade on their AC side to achieve medium-voltage operation and low harmonic distortion [7]. The output voltage is the sum of the voltage that is generated by each cell. The numbers of output voltage levels are *2k+1*, where *k* is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. QZS inverters have been developed which feature several improvements and no disadvantages when compared to the traditional ZSIs [24,25]. The QZS has three dissimilar operation states, namely active state, zero state, and shoot-through state. The proposed work is discussed n-layer single phase QZS-CMI based power system. This system possesses the characteristics of both the QZS inverter and the cascaded multilevel inverter. Each inverter bridge of the QZS-CMI is connected to a separate isolated dc supply. Every module's capacitor voltages and DC-link voltage can be derived using Equation (1).

$$\begin{cases} v_{C1n} = \dfrac{1-D_n}{1-2D_n} v_{dcn} \\ v_{C2n} = \dfrac{D_n}{1-2D_n} v_{dcn} \\ \hat{v}_{PNn} = v_{C1n} + v_{C2n} = \dfrac{1}{1-2D_n} v_{dcn} \end{cases} \quad (1)$$

Where $n \in \{1, 2, 3, 4\}$, Dn is the shoot-through duty ratio of the n^{th} module.

The output voltage of QZS-CMI is

$$v_H = v_{H1} + v_{H2} + v_{H3} + v_{H4} \quad (2)$$

In this paper voltage relationship among H-Bridges are in the ratio of 1:2:4:8. Fig. 1 shows the schematic of the proposed 31-level QSZ-CMI for a single-phase system. This circuit topology is identical to that of a traditional 9-level inverter, except that asymmetrical separate voltages are employed [26].

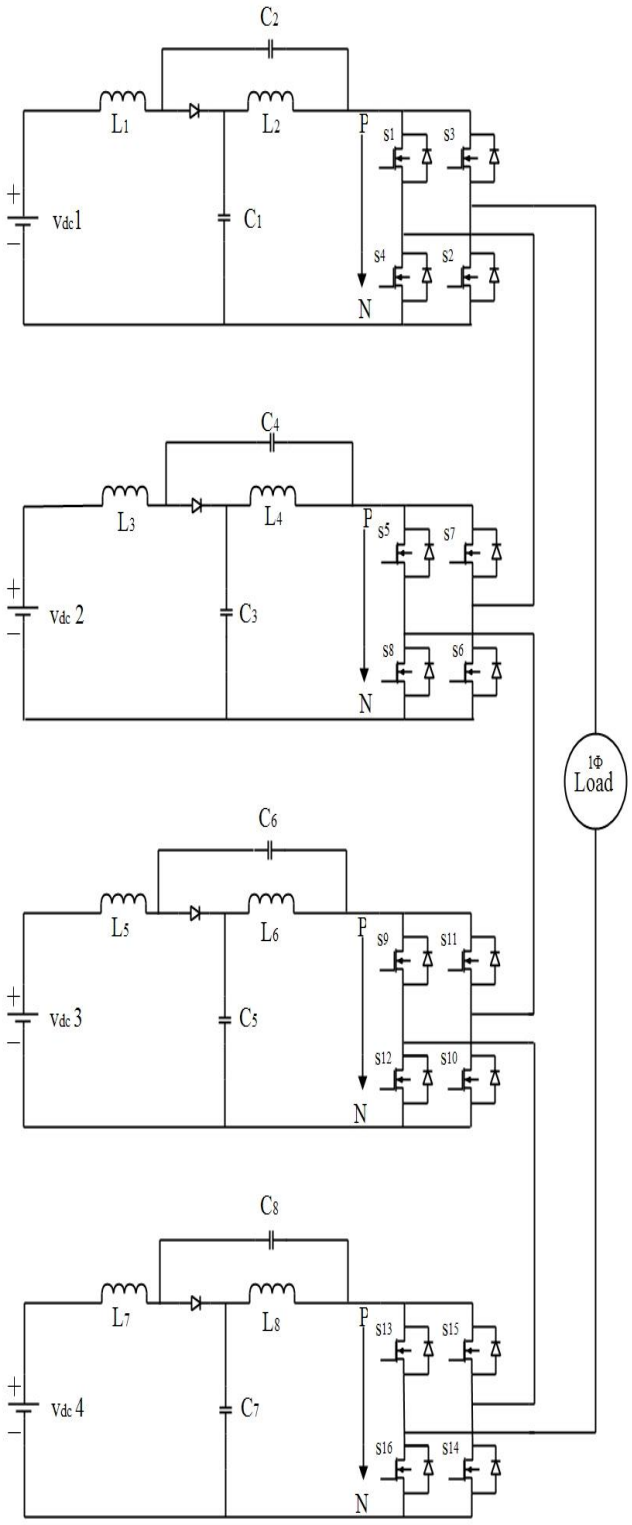

Fig.1. Topology of the 31-level QSZ-CMI.

The separate DC voltage sources with the ratio of 10:20:40:80 can be used by controlling the switching

of the cascade inverter modules, the voltage in 31-level ranges from 15 V_{pu} to -15 V_{pu} with equal step level of V_{dc} [27]. Different outputs of first bridge are +10V_{dc}, -10V_{dc}, 0; similarly second, third and fourth bridges are +20V_{dc}, -20V_{dc}, 0; +40V_{dc}, -40V_{dc}, 0 and +80V_{dc}, -80V_{dc}, 0 respectively. So switches in each H-Bridge should be controlled in such a way that the desired level in corresponding interval is obtained. Table 1 shows the control of inverter modules in the asymmetrical cascaded inverter to produce an output voltage of 31-level, the output voltage ranges from +15V_{pu} to -15V_{pu}.

Table 1
Switching patterns of the 31- level QSZ-CMI

Voltage (per unit)	Switching pattern	Voltage (per unit)	Switching pattern
15	1+2+4+8	-15	-1-2-4-8
14	2+4+8	-14	-2-4-8
13	1+4+8	-13	-1-4-8
12	4+8	-12	-4-8
11	1+2+8	-11	-1-2-8
10	2+8	-10	-2-8
9	1+8	-9	-1-8
8	8	-8	-8
7	1+2+4	-7	-1-2-4
6	2+4	-6	-2-4
5	1+4	-5	-1-4
4	4	-4	-4
3	1+2	-3	-1-2
2	2	-2	-2
1	1	-1	-1
0	0	0	0

3. Modulation technique

3.1. Step modulation operating principle

Step modulation scheme requires only one sinusoidal modulating wave which can be divided into 31 zones in magnitude and for each zone one switching pattern can be generated corresponding to output voltage level. Further, by continuously sampling the sinusoidal modulating wave, the controller select the corresponding zone and voltage level as the present output voltage. Through this scheme, switching angles of the 4 H-bridges are calculated in advance and then stored in a lookup table for digital implementation. The step modulation features all the switches operate at the fundamental frequency [19]. A 31-level stepped-voltage waveform of 4 H-bridge modules is shown in Fig. 2, where the output voltages are 8V_{pu}, 4V_{pu}, 2V_{pu} and 1V_{pu} in each bridge. The major effort of CMI is to improve the sinusoidal voltage and current waveform by series switching condition. The method of evaluating the switching angles for switches plays an important task in reducing the lower harmonic distortion of voltage and current waveform in multilevel inverter.

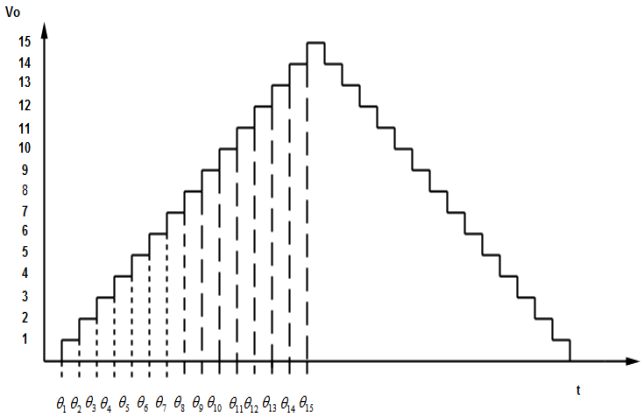

Fig. 2. Stepped voltage waveform of the 31-level QZS-CMI.

The Fourier series expansion of the step-voltage can by described in Eq. (3)

$$Vo(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4Vdc}{n\pi} \left(\sum_{p=1,2,3}^{m} (\cos(n\theta_p)) \sin(n\omega t) \right) \quad (3)$$

where n is the harmonic order, m is the maximum number of switching angles. The coefficient $4V_{dc/\pi}$ represents the peak value of the maximum fundamental voltage, from which $V_{dc} = V_{pu}$.
Modulation index is

$$M = \frac{V_1}{m \times \frac{4V_{dc}}{\pi}} \quad (4)$$

where V_1 is the peak value of the fundamental inverter output voltage, and m is the maximum number of switching angles.

THD is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave.

The THD of the output voltage is expressed as

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=3,7,....}^{\infty} V_n^{\,2}} \tag{5}$$

The voltage gain of the quasi z-source inverter is

$$\frac{V_o}{V_{dc}/2} = MB \tag{6}$$

Where V_o is the output peak phase voltage, V_{dc} is the input dc voltage, M is the modulation index, and B is the boost factor. B is determined by

$$B = \frac{1}{1 - 2\frac{T_o}{T}} \tag{7}$$

Where T0 is the shoot-through time interval over a switching cycle T, or $\left(\frac{T_0}{T} = Do\right)$ is the shoot-through duty ratio. The shoot-through time per switching cycle is made constant that also makes the boost factor constant. This condition eliminates the ripples that are associated with the output frequency by the DC inductor current and capacitor voltage.

3.2. Selective harmonics elimination

This method solves the linear and non-linear system of equation within a fraction of seconds and provides the result in range of milliseconds. The number of harmonics which can be eliminated by the CMI is (N-1) (i.e.) a 31-level inverter 30 number of harmonic order can be eliminated [28]. Here, SHE technique can effectively eliminate certain arbitrary harmonics among these 30 orders by switching the DC-link voltages of a converter on and off via the power switches at certain pre-determined points. The expression governing the SHEPWM for 31-level inverter is given in Equation (8).

$$V(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi}\begin{bmatrix} \cos(\alpha\theta_1) + \cos(\alpha\theta_2) + \cos(\alpha\theta_3) + \cos(\alpha\theta_4) \\ + \cos(\alpha\theta_5) + \cos(\alpha\theta_6) + \cos(\alpha\theta_7) + \\ \cos(\alpha\theta_8)\cos(\alpha\theta_9) + \cos(\alpha\theta_{10}) + \\ \cos(\alpha\theta_{11}) + \cos(\alpha\theta_{12}) + \cos(\alpha\theta_{13}) + \\ \cos(\alpha\theta_{14}) + \cos(\alpha\theta_{15}) \end{bmatrix} \tag{8}$$

Newton-Raphson method [29] is used to solve the non-linear equation systems using successive approximation procedure which is suitable for implementing in a computer program. The lower order harmonics are eliminated using Equation (8), which also makes the desired fundamental component constant by making other harmonic component zero

4. Loss analysis of the proposed 31 level inverter

The various loss components included in QZS are inherent resistance of the source side inductance, leakage resistance of condensers and power electronic switches. The source side inductors inherent resistance in a practical setting is of the order 0.7 Ohms. The differences in each of the source voltages lead to different current in each of the bridge. However, the average source current shared by the four sources can be given as

$$I = P/V = 450/150 = 3 \text{ A} \tag{9}$$

The current supplied by each bridge is not the same and in the case of multi-level inverter these currents are not simultaneous as well. The average current for each bridge will be 3 / 4 A = 0.75 A. This will be maximum possible source current.

The losses occurring in the inherent resistances of the inductors will be

$$= 4 * I^2R = 4 * 0.75^2 * 0.7 \text{ W} = 1.575 \text{ W} \tag{10}$$

The losses occurring in each of the capacitors can be arrived at as follows.

The different Voltages appearing across the asymmetrical sources are 10 V, 20 V, 40 V and 80V. The total voltage will be 150 V. For the purpose of calculating the losses occurring in the capacitors the average voltage existing across each capacitor can be considered as 150 /4.

$$Vc = 150/4 = 37.5 \text{ v} \tag{11}$$

The internal equivalent series resistance of an electrolytic capacitor is typically in the range of 0.13 Ohms to 1.5 Ohms. The average load current is considered as the average ripple current and the resultant losses occurring in the capacitors will be,

$$Wc = 4 * (I^2)/(R) = 4 * (0.75*0.75*1.5) = 3.375 \text{ W} \tag{12}$$

The other major component of losses is the switching losses. As for the Power electronic switches are concerned there are two different components of losses are present. The conduction losses and the switching losses. The switching losses is a function of switching frequency. Since the switching frequency is as low as the line frequency of 50 Hz, this component is negligible as compared to traditional SPWM or SVPWM based high switching frequency cases. The other loss component related to the power electronic switches are the conduction losses that occur in the power electronic switches during the ON time.

The total number of switches are 16. The number of switches engaged in each half cycle is 8. The conduction period of all the switches re not the same. A factor of 0.25 as the utilisation factor may

be considered. The typical on time voltage drop in a typical MOSFET is 2.2 V and the maximum forward current is 3 A the total losses occurring in a switch considering a maximum duty cycle of 1 will be 2.2*3 = 6.6W. The product of the ON time voltage drop and the average current through the switches is the time loss component and has been calculated as follows.

The total conduction losses will be 8 * 6.6W = 52.8W.

Thus the total losses incurred in the entire 31-level inverter accounts to be

W (inductance) + W (Capacitance) + W (switches) = 1.575 + 3.375 +52.8 W = 57.75 Watts.

The overall efficiency of the system is

P_{Input} = V * I = 150 * 3 = 450 W

P_{losses} = 57.75 W

P_{output} = 450 - 57.75 = 392.25 W

Efficiency = 87.17%

Although the efficiency is little less than 90 % it is well justified when compared to the increased losses that would occur in the load side when an inverter with lower levels are used. Thus the proposed 31 level inverter that works with the SHE PWM strategy wherein the switching losses are negligible, with improved THD of the generated source the overall efficiency of the system as a whole will be held high.

4.1. The Component count cost and reliability

As for as the component count is concerned, a comparison with the diode clamped multilevel inverter and the reduced component multilevel inverter may be considered. In case of diode clamped 31 level inverter, the total number of switches will be 2 (m -1) = 60 and besides that topology may require a large number of clamping diodes and balancing capacitors. In the case of a conventional H bridge cascaded multilevel inverter with symmetrical voltage sources the number of bridges to be used for a 31 level inverter will be 60. The proposed topology of 31 level inverter, the number of switches are only 16 due to the use of asymmetrical sources and no extra components like balancing capacitors and clamping diodes are required.

The reduced number of switches, the balancing capacitors and the clamping diodes eliminates the problem of probable frequent breakdown and even in the event of breakdown the down time is reduced. Thus the cost and maintenance of the proposed scheme is much reduced and the reliability is increased. Table 2 shows the cost comparison of the conventional with proposed method (MOSFET IRF840).

Table 2
Cost comparison

Level	No of switches		Cost of switches ($)	
	Conventional	Proposed	Conventional	Proposed
3-Level	4	4	2.17	2.17
7-Level	12	8	6.50	4.35
15-Level	28	12	15.22	6.50
31-Level	60	16	32.62	8.70

5. Results and Discussion

5.1. Simulation results

A single-phase 3-level, 7-level, 15-level and 31-level QZS-CMI system with resistive load was simulated in MATLAB / Simulink. The input voltages up to 31-level considered for simulation are 10V, 20V, 40V and 80V. The switching signals are derived from the switching subsystem. The system parameters for simulations are listed in Table 3. The proposed QZS-CMI circuit is designed without filter

Table 3
System specifications

Parameter	Value
Input DC voltage	150 V
QZS inductance	600 µH
QZS capacitance	4500 µF
Load resistance	100 Ω
Modulation index	0.8

A 3-level QZS-CMI is designed with specified parameters and the voltage source for single H-bridge is chosen as V_{dc} = 20V with step modulation - SHEPWM method. The maximum positive peak and negative peak voltage for 3-level QZS-CMI is maintained at 32.15V. Similarly, a 7-level QZS-CMI is designed as 2 H-bridges, with voltage source is in the ratio of 1:2 for 2 bridges. The maximum positive peak and negative peak voltage for 7-level QZS-CMI is maintained at 44.96V. The 2 H-bridge inverter is driven by the controller which generates the gate signal for 8 switches of the inverter. The output voltage waveform and fast fourier transform (FFT) analysis are shown in Fig. 3 and Fig. 4.

The QZS-CMI is further designed as 3 H-bridges for 15-level inverter, with voltage source in ratio of 1:2:4. The maximum positive peak and negative peak voltage for 15-level QZS-CMI is maintained at 105V.

The 31-level QZS-CMI is powered with the voltage from the separate DC voltage source; the output waveform obtained would have reduced THD

waveform. The simulation diagram of the proposed 31-level is shown in Fig. 5. 31-level QZS-CMI is designed as 4 H-bridges, with the voltage source in the ratio of 1:2:4:8. The maximum positive peak and negative peak voltage for 31-level QZS-CMI is maintained at 216.2V. The gate triggering pulse for the 4 H-bridge with 16 switches is generated by step modulation-SHEPWM method. The proposed QZS-CMI circuit is designed, output voltage waveforms and FFT analysis is shown in Fig. 6 and Fig. 7.

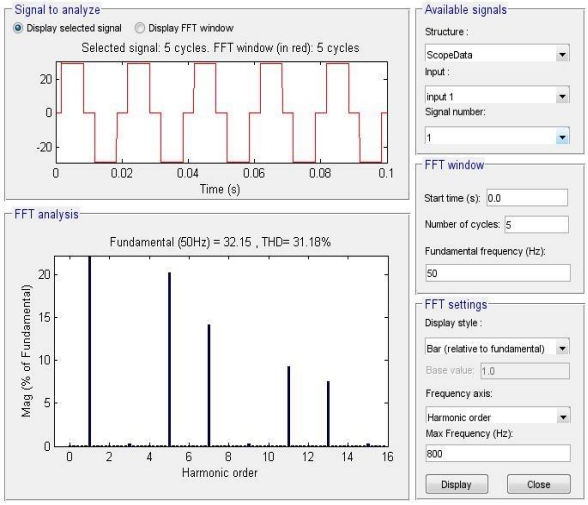

Fig. 3. FFT Analysis of 3-level for Phase Voltages

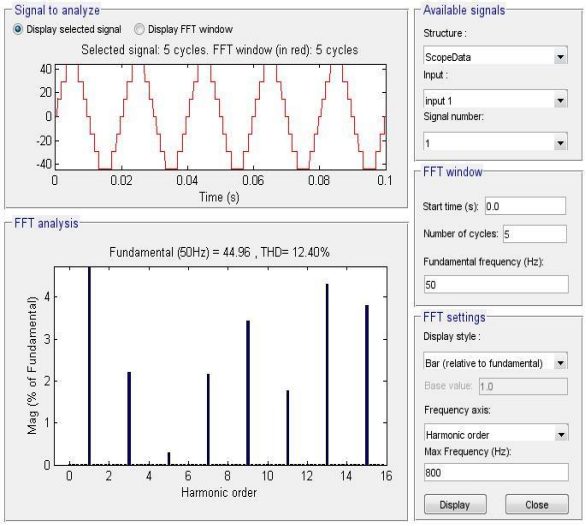

Fig. 4. FFT Analysis of 7-level for Phase Voltages

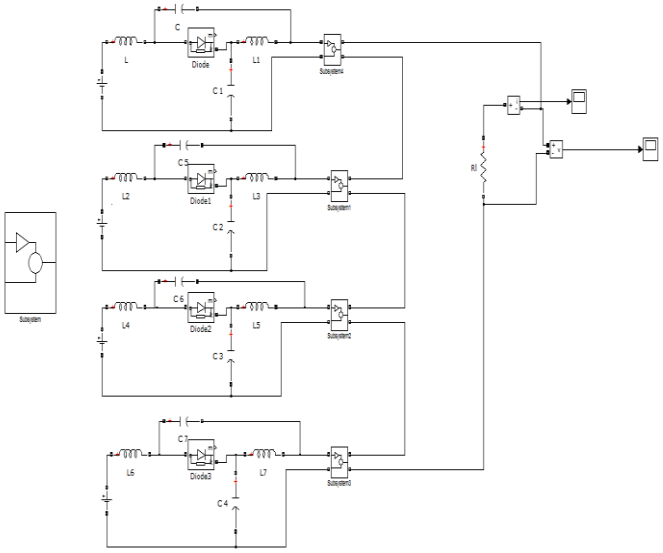

Fig. 5. Simulink of the 31-level QZS-CMI system

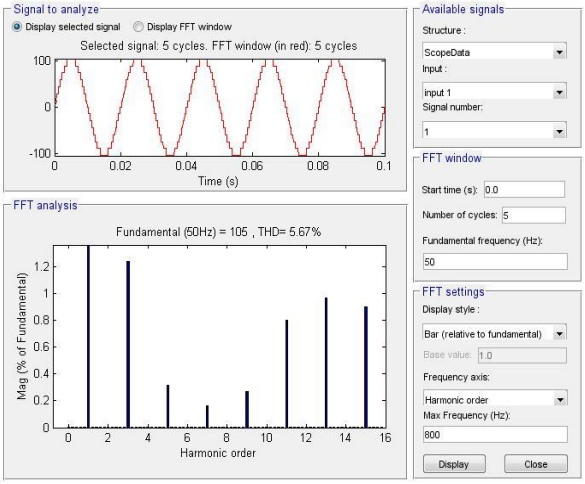

Fig. 6. FFT Analysis of 15-level for Phase Voltages

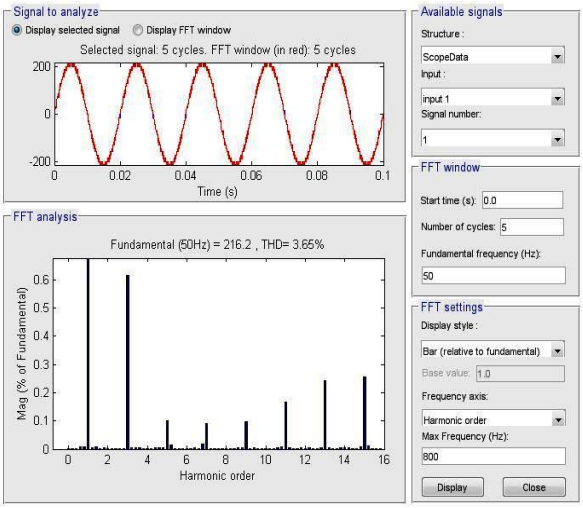

Fig. 7.FFT Analysis of 31-level for Phase Voltages

The performance is investigated through MATLAB simulation and the resulting THD is calculated and plotted for 3-level, 7-level, 15- level and 31-level. The lowest THD observed is 3.65% in 31-level QZS-CMI, which satisfy the IEEE standard 519. Since there is no filter in the simulation circuit, the input 150V DC of the 31-level inverter is stepped-up to 216.2V AC at a modulation index of 0.8, which can also be adjusted based on desired output voltage. This eliminates the need of boost converter in input side and transformer in output side. The simulation results are given in Table 4.

Table 4
Comparison of different level Voltage gain & THD (Modulation Index =0.8)

Topology	DC input voltage (V)	Output voltage (V)	THD%
3 level	20	32.18	31.18
7 level	30	44.96	12.40
15 level	70	105	5.67
31 level	150	216.2	3.65

5.2. Experimental verification

The proposed system with the operating conditions and system configuration as in the simulation are conducted in experimental setup with separate bridge as shown in Fig. 8. A modular QZS-CMI, 450*W*/150*V* prototype has been built and tested in the laboratory. The MOSFET IRF840 is selected as inverter switch; it can utilize the fast-switching low-cost and low voltage. The switches are operating at fundamental frequency and the number of switches is 16. The increased level of switching conditions may also increase the conduction losses, to avoid this situation; switches are turned on by individual driver with the transformer. The switching signals are added to the look up table and the control program developed by C language is then downloaded into the memory of ARM processor LPC 2148, using the Phillips flash tool. The initial guess value is taken from look up table for every new command of modulation index. The look up table is changed based on the DC link voltage and output current.

The output voltage waveform of 3- level, 7-level, 15-level and 31-level QZS-CMI is shown in Fig. 9, Fig.10, Fig.11 and Fig.12 respectively. The comparisons of THD, voltage gain for different level of QZS-CMI experimental results are shown in Table 5. The output voltage waveforms are taken from the Digital storage oscilloscope (DSO-Scintech 7040C). THD and voltage gain are measured using power quality analyzer (Krykard ALM35).Table 6 shows the comparision of losses for different level QZS-CMI. The graph of number of levels versus voltage gain & THD for different level is shown in Fig.13 and Fig.14.

Table 5.
Comparison of voltage gain and THD for different level of QZS-CMI (Experimental)

Topology	DC input voltage (V)	Output voltage (V)	THD%
3 level	20	30.13	32.98
7 level	30	42.51	12.50
15 level	70	107.73	5.71
31 level	150	215.10	3.68

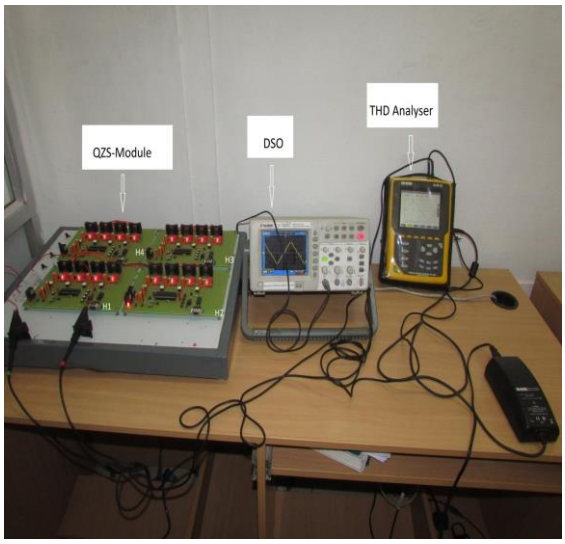

Fig. 8. Experimental Setup

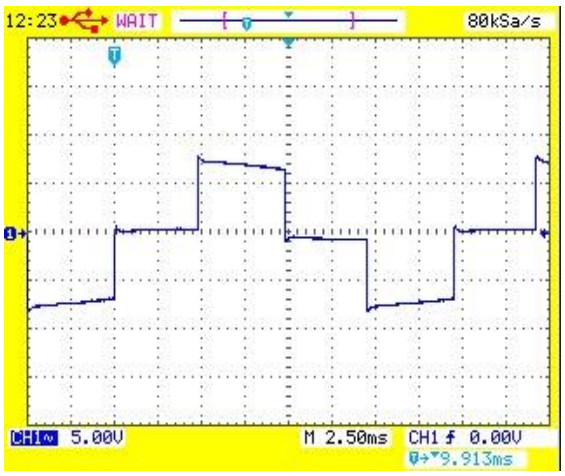

Fig. 9. Output voltage waveform of 3-level

Table 6.
Comparison of losses for different level of QZS-CMI

level	Simulation				Experimental			
	Inductor loss (W) (W_L)	Capacitor loss (W) (W_C)	Switching Loss (W) (W_S)	Total loss (W)	Inductor loss (W) (W_L)	Capacitor loss (W) (W_c)	Switching Loss (W) (W_S)	Total loss (W)
3-level	4.57	6.68	49.75	61.00	5.87	7.92	52.59	66.38
7-level	4.01	5.32	51.51	60.85	5.71	6.62	53.11	65.44
15-level	2.51	4.12	52.02	58.65	3.93	5.91	54.36	64.20
31-level	1.575	3.375	52.8	57.75	2.98	4.64	55.42	63.04

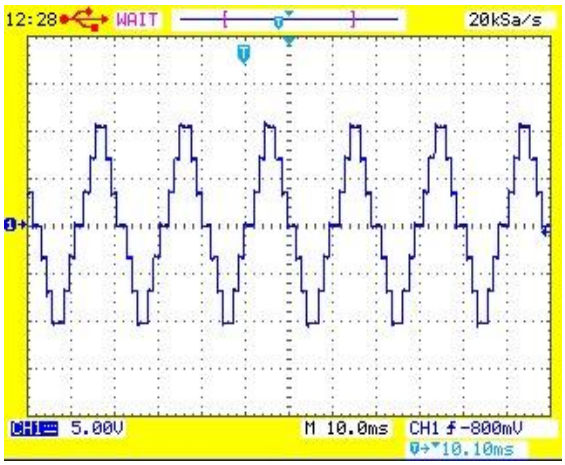

Fig. 10. Output voltage waveform of 7-level

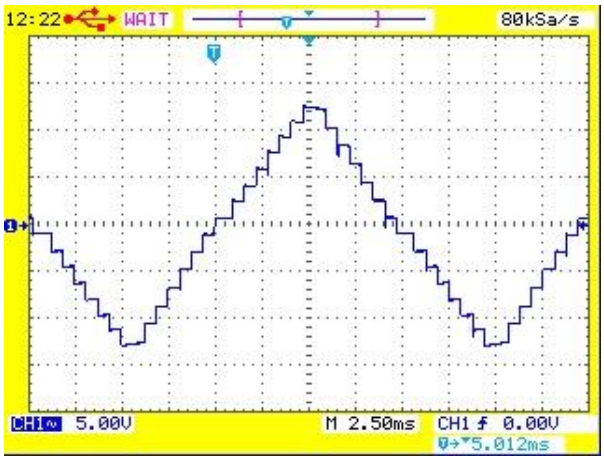

Fig. 11. Output voltage waveform of 15-level

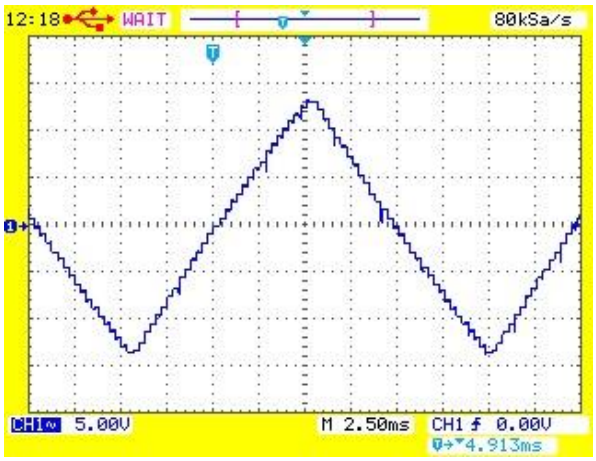

Fig. 12. Output voltage waveform of 31-level

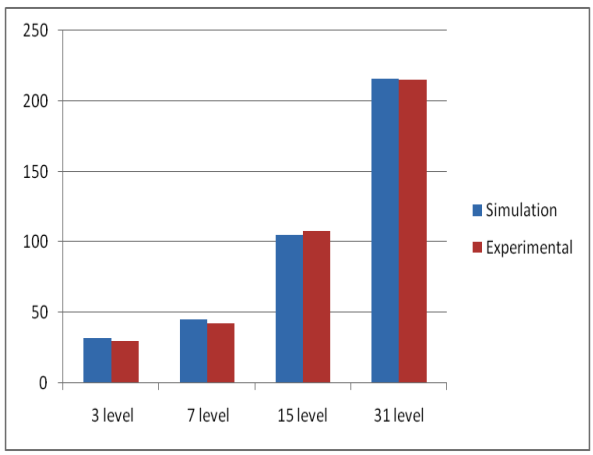

Fig.13. Comparison of voltage gain Vs Level

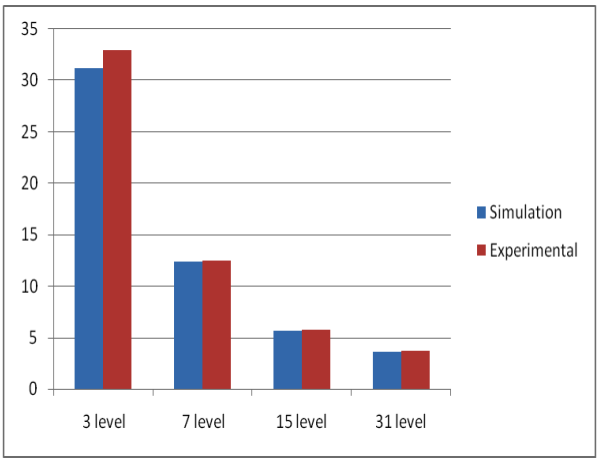

Fig.14. Comparison of THD Vs Level

The findings of this paper are,

- The hardware results are closely matched with the simulation results.
- The proposed QZS-CMI reduces the THD value to IEEE standard at higher level.
- Switches are operated at fundamental frequency hence switching stresses are minimized.
- This inverter eliminates the need for boost converter in input side and transformer in output side. Low cost processor, low voltage MOSFET is chosen. It minimizes overall system cost.
- Since it is operated with a DC source, it is well suited in PV cell and fuel cell applications.

6. Conclusion

In this paper, a comparative analysis of different levels of QSZ-CMI inverter with respect to voltage gain and THD is done. Initially the proposed work is analyzed in simulation and its results are verified through experimental setup. It is observed that THD is achieved within IEEE standard in 31-level QZS-CMI by both the simulation and hardware results. It is evident from the result that the proposed 31-level QZS-CMI topology with hybrid step and SHEPWM technique generates a high-quality output voltage waveform with reduced THD value, complexity, cost and ease of implementation. This proposed topology can also be developed for renewable energy systems, distributed generations, automotive applications and photovoltaic cells.

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