# INVESTIGATION AND IMPLEMENTATION OF SOLAR PV BASED FORWARD MICROCONVERTER

## <sup>1</sup>M.Premkumar, <sup>2</sup>Dr.T.R.Sumithira

<sup>1</sup>Assistant Professor, Department of Electrical & Electronics Engineering, KPRIET, Coimbatore, INDIA <sup>2</sup>Assistant Professor, Department of Electrical & Electronics Engineering, GCE, Salem, INDIA <sup>1</sup>mprem.me@gmail.com, <sup>2</sup>sumithra.trs@gmail.com

# <sup>3</sup>R.Sowmya

<sup>3</sup>Assistant Professor, Department of Power Engineering, GMR Institute of Technology, Rajam, INDIA <sup>3</sup>sowmyanitt@gmail.com

**Abstract** - The centralized traditional power grid leads to national power blackout resulting increase in research for alternate solutions. The solar photovoltaic is connected with module integrated converter (MIC) is the efficient way of increasing the performance in now-a-days. The modelling and analysis of the forward micro converter is done with dynamic simulation software. The Maximum Power Point Tracking (MPPT) algorithm is applied on the SEPIC converter to extract the maximum power from the panel. The objective of the proposed research is to convert the raw solar energy from the PV cell and supplied to the load with high efficiency and high power quality. The proposed converter includes low voltage stress on the semiconductor devices and simplicity of design. The switching losses are also reduced by replacing with single MOSFET in SEPIC converter. Hence the triggering components and commutation components are reduced while using a MOSFET and therefore the conduction losses are reduced. The proposed approach is analyzed and experimentally verified.

**Keywords** – Solar PV, Microconverter, MPPT, Voltage stress, SEPIC Converter

# I. INTRODUCTION

Module integrated converter are rapidly growing part of the photovoltaic (PV) system. The microinverters are modelled to convert the DC of one PV module to the AC and are designed to get maximum output power in the range of 100W to 300W [2]. The microinverters has advantage in ease of installation, maximum power point tracking (localized), and robustness to failure when compared to conventional string or central inverters shown in figure 1. Since the researchers of power electronics is seeking rapid innovation, there are many different topologies and variations being developed day by day.

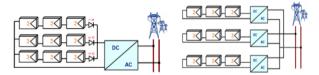


Fig. 1. Central and String Topology

Even the string inverter can give more efficiency in capturing energy, the energy obtained from the panel decreases if one of the series PV cell is kept out by shadow as shown in figure 2.

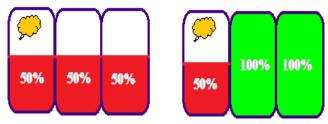


Fig. 2. Energy Harvesting

The MIC prefers "distributed MPPT" architecture which adds more cost per PV panel but efficiency is increased by 4 to 20 percent by recovering the following losses:

- PV panel mismatch losses (3.5 to 6 percent)
- Partial shading losses (5 to 25 percent)
- Simpler system design and fault tolerance (0 to 10 percent)
- Suboptimal MPPT losses (3 to 10 percent)

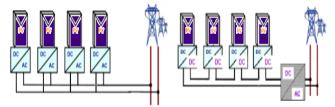


Fig. 3. Basic Module Integrated Converter Topology

So, the micro inverters topology as shown in figure 3 which sacrifices the converter efficiency but make the energy capture more efficient [4]. The microinverter outputs are connected in parallel and routed to a common ac coupling point. To keep dc wiring at relatively low voltage level of a single panel, no series or parallel dc connections are provided. Basically optimal application for specific inverter can be determined from [6] the comparison of the key parameters which is listed in table 1.

<b>Table 1. Key Parameters Comparison of Different Size</b>
Inverters

	Nominal Power	Nomin al Voltag e	Maximu m Efficien cy	Cost	Cost/W att
Microco nverter with Inverter	< 300W	< 100V	97.5%	Low	High
String Inverter	< 30kW	150V – 1000V	98%	Mediu m	Medium
Central Inverter	> 30kW	450V – 1500V	98.5%	Very High	Low

The single-phase microinverter architectures have been reviewed in [5] and the topologies are grouped into single-stage architectures and multistage architectures in figure 4. In a single stage architecture, voltage and power modulation, and output current shaping are realized in a single power stage but they have low circuit complexity and simple control. Over a wide operating range, it is not possible to achieve high performance. In multistage topology, multiple power conversion stages and each stage can perform one or more functions. The optimization is done individually at each stage, thus the overall performance is better but component requirement and control complexities are usually higher.

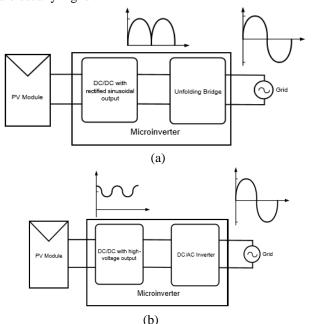


Fig. 4. (a) Microinverter using a Single-Stage Topology, (b) Multi-Stage Topology

In addition, distributed maximum power point tracking (MPPT) terminal for segmented PV arrays can be achieved

by single ended primary inductance converter (SEPIC). There are many configuration for converter [7] such as Buck, Boost, Buck-Boost, SEPIC, CUK and Fly-back and Buck and Boost configurations can decrease and increase the output voltages respectively and others can do both functions. The SEPIC converter must be operated at high switching frequency. However, high switching frequency on the device will increase the reverse recovery current of the output diode which delivers additional switching losses. The switching frequency will also increase in high electromagnetic interference (EMI) noises and additional thermal management. Also, the switch utilization factor of the SEPIC converter is lower than buck-boost converter i.e. the power-handling capabilities of MOSFET in the SEPIC converter are much lower than buck or the boost converter at the same power level. Thus, the reduction of reverse recovery loss is particularly important for the SEPIC converter.

MPPT algorithm is important to increase the efficiency of PV module and maintain the PV panel operating point at maximum power point in different environment conditions. Many MPPT techniques have been proposed in [8] are the Perturb and Observe (P&O) methods, adaptive P&O, Model Adaptive control method. reference Incremental Conductance (IC). The proposed incremental conductance method operates with variable step adapted to the actual operating conditions. Since the incremental conductance method always work around the real maximum so that a precise knowledge is not required. The leakage energy delivered by the transformer is handled with the help of decoupling circuit alone so there is no need for additional dissipative circuits [9], which will reduce power losses and improves the converter efficiency.

# **II. Circuit Topology**

The power stage elements of the proposed converter are as follows. The PV supplies a DC input of 24 V to the dc – dc converter. The SEPIC converter which gives higher or lower output voltage than the given input voltage with the help of MOSFET and energy storage elements. There are two operating modes of the converter depends on the load current flow which may be of Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). The SEPIC converter is selected based on its buck-boost capability without inversion of voltage. The storage capacitor is connected across the output and also it serves the supply the difference between the power of the PV panel and double line frequency power variation of the inverter.

#### 2.1 Continuous vs. Discontinuous Conduction Mode

The model simulation and key assumptions are documented in further section. The proposed design has small inductor current ripple in case of CCM as well as large inductor current ripple in case of DCM. The operation of the converter in CCM was suitable for the proposed model because of the ripple in the inductor current is lower and the input current is continuous. Also CCM offers higher efficiency than DCM and voltage gain is independent of the type of load whereas in DCM, voltage gain of the system is depends on the load and designed parameters such as L and switching frequency. But CCM has small switching loss produced by diode reverse recovery. Even though the size of the inductor can be reduced than CCM, the input current is pulsating. The converter can be operated in both modes by defining the power load and the input voltage but the proposed model is tested in CCM.

# 2.2 MPPT Controller Modeling

Due to the continuous change in insolation and temperature, the current-voltage (I-V) and the power-voltage (P-V) characteristics of a PV module is affected. On both I-V characteristic and P-V characteristics, knee point is defined at which the module can deliver maximum power with maximum efficiency. This knee point is called the maximum power point (MPP) of the PV module. At any environmental condition, the MPP is tracked at the module operates at its maximum efficiency. The control algorithms which tracks the MPP is implemented in conjunction with a power conditioning unit between the PV module and the electrical load.

The implementation of MPP tracking algorithm uses PV module maximum operating voltage, maximum current or power as the input variable and the algorithm generates the reference output which can be used as a control variable which helps to change the duty cycle of the proposed converter. There are many MPP tracking algorithms are exist which includes:

- 1) Perturb-and-observe (P & O) technique
- 2) Incremental conductance technique
- 3) Ripple correlation control (RCC) technique
- 4) Fractional open-circuit voltage technique
- 5) Fuzzy logic based technique
- 6) Current based peak power tracking
- 7) Parasitic capacitance technique

Due to high accuracy of tracking the MPP in continuous change in environmental conditions and less complexity, the Incremental conductance technique is used in this work. This techniques compares the incremental conductance  $(\Delta I/\Delta V)$  with the instantaneous conductance (I/V) of the PV

module and the MPP can be accurately tracked. The sum of incremental conductance and instantaneous conductance is zero at MPP, negative on the right side of MPP and positive on the left side of MPP as shown in figure 5 and the corresponding algorithm for MPP is shown in figure 6. At MPP, the algorithm keeps the previous value of the variable and the duty cycle.

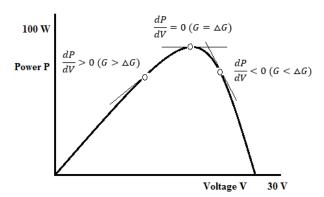


Fig. 5. P-V Characteristics of Module

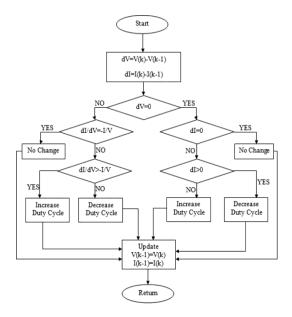


Fig. 6. Incremental Conductance Algorithm Flow Chart

# III. SYSTEM ANALYSIS

# 3.1 Modelling of SEPIC Converter

The SEPIC converter is connected with solar PV module to perform the following major functions:

- 1) Boost the lower PV voltage
- 2) Regulate the varying dc output voltage
- 3) Implement the MPP tracking of the solar panels

The SEPIC converter is selected because of its buck-boost operation without inverting the output voltage. The equations (1) to (11) are used to model and design the converter which operates in continuous current conduction mode. The output voltage is given by,

$$Vout = Vin * \frac{D}{1 - D} \tag{1}$$

Where D is duty cycle of the switching device which is given by,

$$D = \frac{Vout + Vd}{Vout + Vin + Vd} \tag{2}$$

 $V_d$  is the forward voltage drop across  $D_1$  and the maximum duty is given by,

$$Dmax = \frac{Vout + Vd}{Vout + Vin(min) + Vd}$$
 (3)

The inductance value is determined by allowing the peakpeak ripple current to be approximately 40% of the rated input current at the minimum input voltage. The ripple current ( $\Delta IL$ ) flows through the two equal value of inductors which is given by,

$$\Delta IL = Iin * 40\% = Iout * \frac{Vout}{Vin(min)} * 40\%$$
 (4)

And the two equal inductor values are determined by,

$$L1 = L2 = L = \frac{Vin(min)}{\Delta IL * Fs} * Dmax$$
 (5)

The peak value of the inductor current which ensures the saturation of the inductor is given by,

$$\Delta IL1(peak) = Iout * \frac{Vout + Vd}{Vin(min)} * \left(\frac{1 + 40\%}{2}\right)$$
 (6)

$$\Delta IL2(peak) = Iout * \left(\frac{1 + 40\%}{2}\right)$$
 (7)

The selection of the coupling capacitor (Cs) depends on the RMS current which is given by,

$$Ics(rms) = Iout * \sqrt{\frac{Vout + Vd}{Vin (min)}}$$
 (8)

The SEPIC capacitor is rated for a large RMS current which makes the converter much better for lower power applications where the RMS current through the capacitor is relatively small. The voltage rating of the coupling capacitor is greater than the maximum input voltage. The electrolytic capacitors work well for the proposed work where the size is not limited. The voltage across the coupling capacitor is given by,

$$\Delta V cs = \frac{Iout * Dmax}{Cs * Fs} \tag{9}$$

And the coupling capacitor is given by,

$$Cs = \frac{D}{R * \frac{\Delta V cs}{Vout} * Fs} \tag{10}$$

When the power switch Q1 is turned on, the inductor is charging and the output current is supplied to the load by the output capacitor. As a result, the output capacitor is subjected to large ripple current so that the selected output capacitor must withstand the maximum RMS current. The output capacitor must meet out the require RMS current, equivalent series resistor (ESR) and capacitance requirements. The value of the output capacitor (Co) is given by,

$$Co \ge \frac{Iout * Dmax}{Vripple * Fs}$$
 (11)

Where,  $F_s$  is the switching frequency;  $\Delta I_{L1}$  and  $\Delta I_{L2}$  is peak-to-peak ripple current of inductor  $L_1$  and  $L_2$  respectively;  $V_{out}$  is the output voltage;  $V_{in}$  is the input voltage from the solar PV module; R is the load resistance. The following tables gives the rating of the PV panel and SEPIC converter.

**Table 2. PV Panel Specification** 

Specifications @ G =1000W/m <sup>2</sup> and T=45°C		
Rated Power (P <sub>max</sub> )	80W	
Minimum power	75.4W	
Voltage at P <sub>max</sub> (V <sub>mpp</sub> )	19.8V	
Current at $P_{max}$ ( $I_{mpp}$ )	4.06A	
Short circuit current (I <sub>sc</sub> )	4.8A	
Open circuit voltage (Voc)	24.4V	

**Table 3. SEPIC Converter Specification** 

Parameters	Design Value
Input voltage range Vin	20-60V
Switching frequency F <sub>s</sub>	100kHz
Output voltage Vout	400V
Rated output power P <sub>max</sub>	80W
Current ripple I <sub>L1</sub>	40%
Input inductor L <sub>1</sub> and L <sub>2</sub>	22uH
Coupling capacitor C <sub>s</sub>	10uF
Output capacitor Co	100uF

#### 3.2 Operation of the Proposed Converter

Figure 7 shows a simple schematic diagram of a SEPIC converter which consists of an input capacitor ( $C_{in}$ ), output capacitor ( $C_{out}$ ), coupled inductors  $L_1$  and  $L_2$ , the coupling capacitor  $C_s$  which is charged initially to the input voltage ( $V_{in}$ ).

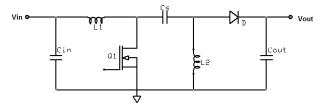


Fig. 7. Proposed SEPIC Converter

The converter is operated in CCM if the current through the inductor  $L_1$  will not reaches zero. During the steady state of the converter, the average voltage across the coupling capacitor is equal to the input voltage because the capacitor blocks the DC current so that the average current is zero which makes the inductor  $L_2$  as the source for the load current. Due to  $V_{L1}$ =- $V_{L2}$ , the two inductors are wound on the same core. Since the magnitude of the voltage is same, the effect of mutual inductance is zero. And ripple current from two inductors are same in magnitude. So, the current through the inductor  $L_2$  is same as that of load current and it is independent of the input voltage. The input voltage is given by,

$$V_{in} = V_{L1} + V_{L2} + V_{cs} \tag{12}$$

As shown in figure 8, when Q1 is off, the voltage across  $L_2$  must be equal to the output voltage since the input capacitor  $C_{in}$  is charged to the input voltage  $V_{in}$ . So that the voltage across Q1 when Q1 is off is equal to  $V_{in} + V_{out}$  and the voltage across  $L_1$  is equal to the output voltage.

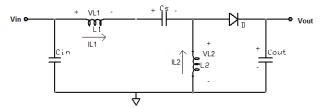


Fig. 8. Q1 in OFF State

As shown in figure 9, when Q1 is on, the capacitor  $C_s$  is charged to  $V_{in}$  and it is connected in parallel with  $L_2$ , so that the voltage across  $L_2$  is inverse of the input voltage  $-V_{in}$ . During Q1 on, the currents flowing through circuit elements are shown in Figure 10. When Q1 is on, the energy is stored in  $L_1$  from the input voltage and in  $L_2$  from the coupling capacitor  $C_s$ . The average current on the diode  $D_1$  is given by,

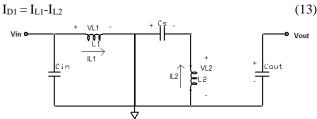


Fig. 9. Q1 in ON State

When Q1 turns off after certain time period,  $L_1$  current continues to flow through  $C_s$  and  $D_1$  and finally into the output capacitor  $C_0$  and the load. Both the capacitors get recharged so that the capacitors can deliver the load current and charge the inductor  $L_2$ , respectively, when Q1 turns on again.

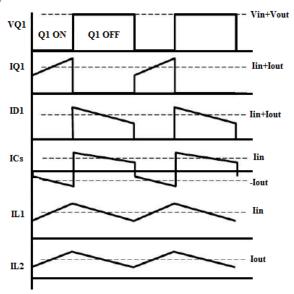


Fig. 10. SEPIC component currents during CCM

# 3.3 MATLAB/SIMULINK Simulation of SEPIC Converter

The simulation of the SEPIC converter is done with the help of MATLAB/SIMULINK. The parameters are selected as per the table given below.

Table 4. Parameters for MATLAB Simulation

Specifications @ G =1500W/m <sup>2</sup>			
Parameters	Design Value		
PV Panel Voltage	21.6 V		
Panel Voltage @P <sub>max</sub>	20.82		
Switching frequency F <sub>s</sub>	500kHz		
Converter Output voltage Vout	167V		
Rated output power P <sub>max</sub>	79.63W		
Input inductor L <sub>1</sub> and L <sub>2</sub>	22uH		
Input Capacitor	4.7uF		
Coupling capacitor C <sub>s</sub>	7uF		
Output capacitor Co	100uF		

With the above designed parameters, the Simulink model is derived and simulated. The outline of the Simulink model is shown in figure 11. The gate signal for the MOSFET is generated by employing incremental conductance algorithm which is mathematically modelled in Matlab/Simulink. The

mathematical model and its relevant embedded function of the algorithm is shown in figure 12.

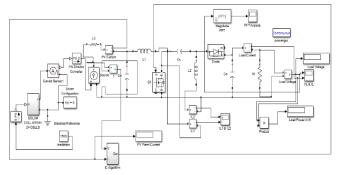


Fig. 11. MATLAB/SIMULINK Model of the Converter

First, mathematical model of the algorithm is done in the subsystem by receiving the panel voltage and current. The embedded function in figure 12 which serves constant output pulses for the MOSFET for efficient operation and delivers less switching loss.

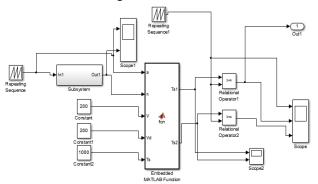


Fig. 12. MPPT Simulink Model

According to the converter parameters including inductors  $L_1$  and  $L_2$ , output capacitor, coupling capacitor, input capacitor, input voltage, output voltage, switching frequency, the converter is operated at CCM since the load is a constant load and the primary inductor current will not reach zero. The output voltage and current is regulated by using PI controllers in the inner control loop. The PI controllers are tuned using Ziegler-Nichols tuning method.

# IV. RESULTS AND DISCUSSIONS

The simulation model has been developed for 24 cell PV array, SEPIC converter, MPPT with incremental conductance algorithm using Matlab/Simulink dynamic simulation software. The simulation is done using the designed parameters which is listed in table 4 in section III. The module is designed with PV arrays and string of four modules are connected in series.

## 4.1 Effect of Changing Temperature on PV Module

The temperature effect on PV voltage for the various solar irradiation and PV characteristics for different irradiation at constant temperature are shown in figure 13-14. From figure 13, it is seen that with increase in ambient temperature, the load current of the module is increased, while the open circuit voltage is decreased. The net output power is reduced because of reduction in open circuit voltage with increasing temperature is seen in figure 14. The effect of changing irradiation on system performance is also shown in figure 13-14; where it is seen that because of the increase in load current with increase in irradiation which will increase the PV output power.

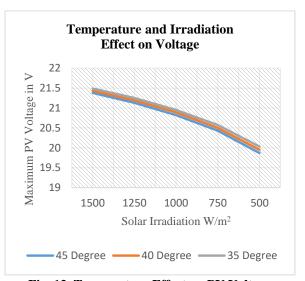


Fig. 13. Temperature Effect on PV Voltage

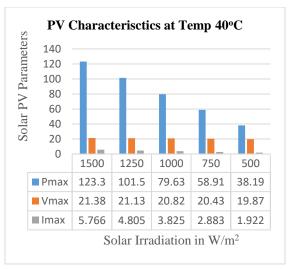


Fig. 14. PV Characteristics at Temperature 40°C

# 4.2 MATLAB/SIMULINK Simulation

The model is designed and simulated with Matlab/Simulink dynamic simulation software with the already designed variables as shown in table 4 in section III. The SEPIC converter load voltage and load current is shown in figure 15. The converter takes finite time to reach the steady state output voltage as shown in figure 15.

The performance of the MPPT algorithm is verified by changing the solar irradiation from 500W/m² to 1000W/m² at step time of 2 seconds and then to 1500W/m² at 4 seconds. The changes in the output power tracking the changes in irradiation indicates that the incremental conductance algorithm delivers good dynamic performance which gives steady state output voltage at very fast rate as shown in figure.

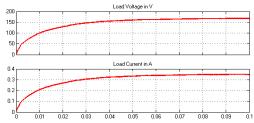


Fig. 15. Converter Load Voltage and Load Current

Before designing pulse width modulation (PWM) switching pulse, the allowed inductor ripple current,  $\Delta I_L$  need to be decided. If the allowable current is too high, which will increase the electromagnetic interference or if it is too low, results unstable PWM operation. Normally, it is advisable to select 20 to 40% of the input current as the inductor ripple current as computed in [10]. This work has simulated with the inductor ripple current as 40% of the input current. The inductor currents  $I_{L1}$  and  $I_{L2}$  is shown in figure 16.

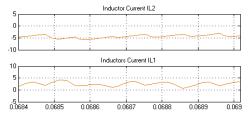


Fig. 16. Inductor currents  $I_{L1}$  and  $I_{L2}$  at 40% of Input Current

#### 4.3 Hardware Implementation

The parameters are designed as per the specific input voltage and listed in table 5. The following are the basic data's for deriving the values of other parameters.

Design Data:

Input voltage ( $V_{in}$ ): 20 - 60V, Rated Power = 80W

Output voltage (V<sub>out</sub>): 400 V Output current (I<sub>out</sub>): 0.2A Switching frequency  $F_s$ : 500 kHz and Assume  $V_d = 0.5V$ 

Table 5. Hardware Design Parameters for the Rated Power of 80W

	Rated Power of 80 W					
S. N	Parameter Computation	Designed Value	Selected Value			
1.	$Dmax = \frac{Vout + Vd}{Vin(min) + Vout + Vd}$ $Dmin = \frac{Vout + Vd}{Vout + Vin(max) + Vd}$	$D_{max} = 91.2\% \\ D_{min} = 82.4\%$	D <sub>max</sub> = 92% D <sub>min</sub> =82%			
2.	The input inductor $L_1$ ripple, $\Delta IL = lin * 40\%$ $= lout * \frac{Vout}{Vin(min)} * 40\%$ So the inductance for L1 and L2, $L1 = L2 = L = \frac{Vin(min)}{\Delta IL * Fs} * Dmax$ The peak input inductor current, $\Delta IL1(peak) = lout * \frac{Vout+Vd}{Vin(min)} * \left(1 + \frac{40\%}{2}\right)$ $\Delta IL2(peak) = lout * \left(1 + \frac{40\%}{2}\right)$	$\Delta IL = 1.6A$ $L1 = L2$ $= 22.8  uH$ $\Delta IL1(peak)$ $= 4.3  A$ $\Delta IL2(peak) = 0.99  A$	L1 = L2 = 22 uH			
3.	$\begin{split} & \text{The MOSFET peak current is:} \\ & I_{Q1} \; (peak) = I_{L1} \; (peak) + I_{L2} \; (peak) \\ & I_{Q1rms} = \\ & \textit{Iout} \sqrt{\frac{(\textit{Vin}(\textit{min}) + \textit{Vout} + \textit{Vd}) \cdot (\textit{Vout} + \textit{Vd})}{\textit{Vin} \; (\textit{min})^2}} \end{split}$ The gate drive current $I_g \; \text{of the} \; \\ & \text{IR2110 is 0.3A. The estimated} \; \\ & \text{power loss is:} \; \\ & P_{Q1} = I_{Q1 \; (rms)} * R_{DS \; (ON)} * D_{max} + \\ & (V_{in(min)} + V_{out}) \\ & * I_{Q1(peak)} * Q_g d^*F_s \; / \; I_g \end{split}$	$I_{Ql}$ (peak) = 5.29 A $I_{Qlrms}$ =4.103A $P_{Ql}$ = 0.92W	MOSFET rated drain voltage must be higher than V <sub>in</sub> +V <sub>out</sub> . IRF740n (SiHF740) is selected in this design.			
4.	SEPIC coupling capacitor selection is: $\Delta V cs = \frac{Iout * Dmax}{Cs * Fs}$ $Ics(rms) = Iout * \sqrt{\frac{Vout + Vd}{Vin (min)}}$	$\Delta V cs$ $= 0.452 V$ $Ics(rms)$ $= 0.935A$	The selected capacitor is ceramic cap and the value is Cs = 10uF			
5.	The RMS current of the output capacitor is: $I_{Cout(rms)} = I_{Cs(rms)} = 0.935A$ $Co \ge \frac{Iout * Dmax}{Vripple * Fs}$	Co ≥ 121uF	Co = 100uF The electrolytic capacitor is selected due to cost.			
6.	Output diode selection is: The reverse rated voltage of the diode should be higher than $V_{in}+V_{out}$ and at full load, the average diode current must be equal to the output current.	-	The selected diode is FR107 since it is having reverse recover voltage as 1000V and average current of 15A			

Two inductors are tightly coupled with each having same number of winding on the single core. The mutual inductance between the winding, force the ripple current to split equally between two inductors. But practically, the inductors do not have same inductance so that the ripple current will not be same. In a real coupled inductor, the inductors do not have equal inductance and the ripple currents will not be exactly equal. For the desired ripple current, the inductance is estimated to be half if there are two separate inductors. The experimental setup of the proposed converter is shown in figure 17 and the converter is tested at 40°C, 1200W/m² solar irradiation.

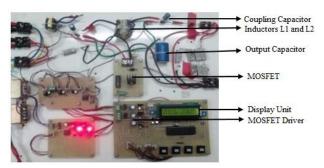


Fig. 17. Experimental Setup of Proposed Converter

The output voltage is obtained from the solar panel under variable conditions. From the observation of variable condition, the voltage from the solar panel is oscillating proportionally. However, the converter generates an output according to the desired output even though there is a variation in the input voltage. The SEPIC converter is designed to supply 80W at normal operating condition. The desired output voltage from the converter with purely resistive load is taken as 400V as shown in figure 18.

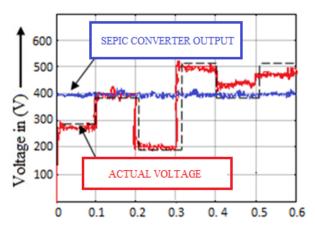


Fig. 18. Hardware Output Voltage waveform  $@1200W/m^2$ ,  $T=40^{\circ}C$ 

The output voltage and the output current of the converter are taken as a feedback with optimized gain such that the PI controller tunes and error with respect to the output also obtained. During different stages the inductor is charged and charged voltage is supplied to the voltage which is available as SEPIC output. The MOSFET is switched ON and OFF according to the desired output voltage. Charging and discharging of the inductor is shown in figure 19(a). The SEPIC output voltage at the desired level is shown in figure 19(b). The voltage across the output capacitor is shown in figure 19(c) and the net value of the capacitor voltage is 400V.

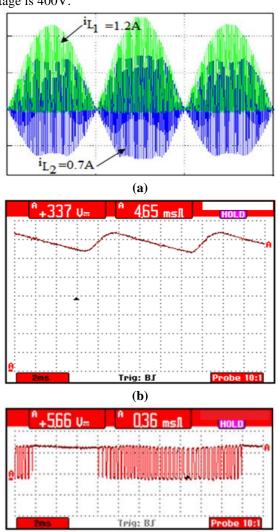


Fig. 19. Various Output Waveforms (a) Inductor Currents  $I_{L1}$  &  $I_{L2}$ , (b) SEPIC Converter Output Voltage, (C) Output Capacitor Voltage

(c)

The estimated loss of the proposed converter is shown in table 6. The efficiency of the proposed converter is acceptable and may be suitable for PV based distributed generation station.

Table 6. Estimated Loss in Converter with CCM

Type of the loss	Predicted Loss		
Switching loss	1.451		
Conduction loss (MOSFET and	1.110		
diode)			
Inductor losses	0.621		
MOSFET driver power consumption	0.245		
Controller power consumption	0.147		
Total Loss	3.574		
Efficiency at the rated power is 95.53%			

#### V. CONCLUSION

In this work, the SEPIC converter modelling in CCM has been done with incremental conductance MPPT algorithm. The Matlab/Simulink simulation results indicates that PV electric power production is highly environmental condition dependent and the maximum output power of the solar PV module can be achieved electronically by incremental conductance MPPT algorithm. The two inductors L<sub>1</sub> and L<sub>2</sub> are wound on the same core so that the same/constant voltages are applied to the inductor throughout the switching period. The switching device current rating will determine and decides the proposed SEPIC converter maximum output current. Since the power rating of the converter is low, the selected switching device SiHF740 MOSFET offers very less conduction loss and switching loss so that it will withstand peak voltage and current of the system. The proposed converter is designed and controlling is implemented with low power and low cost ATMEGA microcontroller which consumes less power and reliability of the converter also appreciable. This work briefs the modelling and implementation of one of the converter topology being used in module integrated converter today. In future, the converter control will be implemented with DSP processor or FPGA for high power rating but for the rating below 100W, ATMEGA controller may be suitable.

# REFERENCES

- [1] Baifeng Chen, Bin Gu, Lanhua Zhang, Zaka Ullah Zahid, Jih-Sheng (Jason) Lai, Zhiling Liao, and Ruixiang Hao, "High-Efficiency MOSFET Transformerless Inverter for Nonisolated Microinverter Applications", *IEEE Transactions on Power Electronics*, Volume 30, Issue 7, July 2015.
- [2] Dongbing Zhang, "AN-1484 Designing A SEPIC Converter", *Texas Instrument Application Report-SNVA168E*, May 2006–Revised April 2013.

- [3] David Meneses, Oscar Garc´ıa, Pedro Alou, Jes´us A. Oliver, Jos´e A. Cobos, "Grid-Connected Forward Microinverter with Primary-Parallel Secondary-Series Transformer", *IEEE Transactions on Power Electronics*, Volume 30, Issue 9, September 2015.
- [4] Jason Tao, Vieri Xue, "Grid-Connected Micro Solar Inverter Implement Using a C2000 MCU", Texas Instrument Application Report-SPRABTO, January 2013.
- [5] Minjie Chen, Khurram K. Afridi, David J. Perreault, "A Multilevel Energy Buffer and Voltage Modulator for Grid-Interfaced Microinverters" *IEEE Transactions on Power Electronics*, Volume 30, Issue 3, March 2015.
- [6] M.Ram kumar, I.Sayed mohammed, J.Manikanda prashath, "Simulation of SEPIC-CHMLI based Microinverter for High Step-up Voltage Conversion", International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, Issue 4, April 2014.
- [7] M.Premkumar, N.Dhanasekar, R.Dhivakar, P.Arunkumar, "Comparison of MPPT Algorithms for PV Systems based DC – DC Converter", Advances in Natural and Applied Sciences, Volume 17, Issue 9, March 2016.
- [8] M.Premkumar, R.Jeevanantham, S.Muthuvigneshkumar, "Single Phase Module Integrated Converter Topology for Microgrid Network", International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering, Volume 2, Issue 3, March 2014.
- [9] P.I. Muoka, M.E. Haque, A. Gargoom, M. Negnevitsky, "Modeling and Simulation of a SEPIC Converter based Photovoltaic System with Battery Energy Storage", 22<sup>nd</sup> Power Engineering Conference (AUPEC), Australasian Universities, November 2012.
- [10] Vuthchhay Eng, Unnat Pinsopon, Chanin Bunlaksananusorn, "Modeling of a SEPIC Converter Operating in Continuous Conduction Mode", 6<sup>th</sup> International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, (ECTI-CON 2009), June 2009.