Dynamic Performance of Three-Level Back-to-Back VSC-HVDC System Using Space Vector Modulation under Faults Conditions

S. Bouafia[(1)], A. Benaissa[(1)] , M. Bouzidi[(1,2)] , S. Barkat[(3)]

[(1)] Department of Electrical Engineering, Intelligent Control & Electrical Power Systems Laboratory (ICEPS). Djillali Liabes University, Sidi-Bel-Abbès, 22000, Algeria.
[(2)] Department of Electrical Engineering, University of Kasdi Merbah, Ouargla 30000, Algeria.
[(3)] Department of Electrical Engineering, M'sila University, M'sila 28000, Algeria.

Email: Bouafia.saber@gmail.com, aek_benaissa@yahoo.fr, bouzidi.m.28@gmail.com/bouzidi.mansour@univ-ouargla.dz, sa_barkat@yahoo.fr

Abstract: *This paper presents a comprehensive model of the Back-to-Back HVDC system based on the three-level Neutral-Point Diode Clamped (NPC) converter. The ac-side controllers are achieved in a synchronous rotating reference frame (d-q) controls direct and quadrature currents to obtain independent control of real and reactive powers. This is achieved by means of PI controllers. The voltage-balancing control of two split DC capacitors of the three-level Back-to-Back HVDC system is achieved using three-level space vector modulation (SVM) with balancing strategy based on the effective use of the redundant switching states of the inverter voltage vectors.*
The reported study results demonstrate a satisfactory response of the VSC-HVDC station operating based on the proposed SVM strategy, under various conditions of studied different normal and fault cases.

Key words*: VSC-HVDC, Back-to-Back, multilevel space vector modulation, capacitors voltages balancing, fault conditions.*

1. introduction

High Voltage Direct Current (HVDC) technology has characteristics which makes it especially attractive for certain transmission applications[1]. HVDC transmission is widely recognized as being advantageous for long-distance, bulk power delivery, asynchronous interconnections and long submarine cable crossings [2]. Two basic classes of converters are considered in HVDC technologies. There are line commutated Current Source Converters (CSC) and self-commutated Voltage Source Converters (VSC). The first group is known as the classic or conventional HVDC system. This family of the HVDC systems is a mature technology which is mainly thyristor based. It is even the technology of the choice for very high power applications (~ 1 GW) and has been successfully applied for different HVDC systems [3-4]. However, there are some disadvantages associated with the line commutated thyristor converters such as (a) requirement of reactive power supply and harmonic filters at each terminal, (b) the problem of commutation failure at inverters and (c) the problems due to adverse system interactions with weak AC system (corresponding to low Short Circuit Ratio (SCR) at the converter bus). VSC based HVDC systems are self commutated with semiconductor switches like string of IGBTs in series. The emerging technology of self-commutated Voltage Source Converter has the advantages of overcoming these problems [5-6]. The VSC based HVDC technology made a modest beginning in 1997 [6-7]. The VSC has the advantages of independent control of active power and reactive power within the feasible region in PQ diagram [8]. In addition they are capable of operating at higher frequencies, currently implemented for switching frequency of around 1800 Hz. Also there is no requirement of fast communication between the rectifier and inverter station for control purposes. The only constraint is posed by the limitations on the IGBT and GCT devices (with turn-off capability), which are used in VSC [6-9].

The requirement to meet high voltage levels, both at AC and DC sides, of an HVDC converter station is best accommodated by multilevel VSC configurations [5]. They were investigated with the requirement of quality and efficiency in high power systems. They offer many advantages such as increased power rating, minimized the harmonic effects and reduced electromagnetic interference (EMI) emission [6-7].

Recently, HVDC converter systems using full Back-to-Back multilevel NPC converters are being investigated owing to their high-voltage, high-current and staircase-like waveform capabilities [6-7-8]. Pulse width modulation (PWM) techniques are showing popularity to control multilevel inverters for multi-megawatt industrial applications [8].

Space vector modulation (SVM) is one of the most popular PWM techniques gained interest recently [14-15]. The salient features of the SVM strategy are as follows. i) It minimizes total harmonic distortion of the ac-side voltages, through utilization of all available voltage levels of the VSC. ii) It minimizes the switching losses since, over each sampling period of the SVM modulator, it uses the three adjacent switching states with minimum ON–OFF state transitions of the switching devices. iii) It enables development of a method for dc-capacitor voltage balancing without the need for auxiliary power circuits and/or offline calculations [14].

The objective of this paper is to analyze the dynamic performance of three levels VSC-HVDC System link using space vector pulse width modulation for control the both VSCs units, with balancing strategy based on the effective use of the redundant switching states of the converters voltage vectors. This paper also presented a dynamic model of a three levels VSC-based HVDC converter station to design the dc-link voltage regulator and power exchange controllers. The analysis is done by the dynamic response under different normal and fault cases.

2. three-levels VSC-HVDC system structure and mathematical model

Currently, the Back-to-Back HVDC system is considered and seen as a single device, hence the two sides support the DC link [9]. Fig.1 shows a schematic representation of a three-level VSC-based HVDC system. The system comprises two Back-to-Back connected three-level NPC converters units. The DC-link is composed of two nominally-identical capacitors. The two VSC units share the same DC-capacitors and intermediate nodes O_1 are common between VSC-1 and VSC-2. An estimate of the total switching losses of the system is modelled by resistor R_p [10].

The AC-side terminal of each converter is connected to the corresponding AC system through a series connected R and L and a three-phase transformer. For simplicity and without the loss of generality, we assume the following: i) the voltage magnitudes of both grids are the same; however, the phases can assume any values. ii) The power switches, diodes and passive components of the two VSCs are correspondingly identical [9-10].

To avoid repetitions in the formulation, the quantities of VSC-1 and AC system-1 are indexed by *k=1*, while those of VSC-2 and AC system-2 are indexed by *k=2*. In this paper, station 1 is designated and chosen as rectifier station while station 2 is designated as inverter station.

A. System mathematical model in abc Frame

Based on the simplified equivalent circuit of Fig. 1, the mathematical equations which govern dynamic behavior of the AC-side voltages are [15]

$$\begin{cases} v_{tak} = R_k i_{ak} + L_k \dfrac{di_{ak}}{dt} + v_{ask} \\ v_{tbk} = R_k i_{bk} + L_k \dfrac{di_{bk}}{dt} + v_{bsk} \\ v_{tck} = R_k i_{ck} + L_k \dfrac{di_{ck}}{dt} + v_{csk} \end{cases} \tag{1}$$

The VSCs terminal voltages defining by:

$$\begin{bmatrix} v_{tak} \\ v_{tbk} \\ v_{tck} \end{bmatrix} = \frac{1}{\sqrt{3}} m_k V_{dc} \begin{bmatrix} \sin(\theta_k) \\ \sin(\theta_k - \frac{2\pi}{3}) \\ \sin(\theta_k + \frac{2\pi}{3}) \end{bmatrix} \tag{2}$$

Where: $\theta_k = \omega_k t + \alpha_k$. m_k and α_k are, respectively, modulation index and phase-angle of the modulating waveforms of VSC-k. ω_k is the angular frequency of AC system-k [9] .

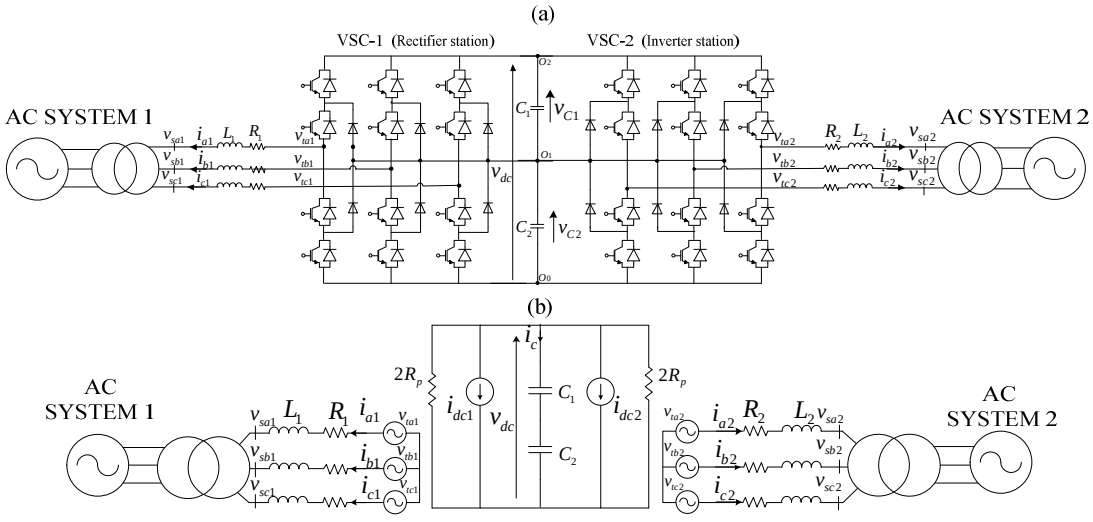

Fig. 1. (a) Three phase Back-to-Back three level NPC based VSC-HVDC system.
(b) Simplified equivalent circuit of three levels VSC-HVDC system.

For the DC-link circuit, the DC-bus voltage dynamics can be described by

$$C_{eq}\frac{dv_{dcj}}{dt} = -\frac{1}{R_p}v_{dc} - (i_{dc1} + i_{dc2}) \tag{3}$$

Where $C_{eq} = C/2$ and is the equivalent capacitor seen by each VSC. Based on the power balance equation of each VSC, we deduce :

$$i_{dck} = \frac{1}{v_{dc}}(v_{tak}i_{ak} + v_{tckb}i_{bk} + v_{tck}i_{ck}) \tag{4}$$

Substituting for v_{tak}, v_{tbk} and v_{tck} by their fundamental-frequency components from (2) in (4), we deduce

$$\begin{aligned} i_{dck} = \frac{1}{\sqrt{3}}m_k(i_{ak}\sin(\theta_k) + i_{bk}\sin(\theta_k - \frac{2\pi}{3}) \\ + i_{ck}\sin(\theta_k + \frac{2\pi}{3}) \end{aligned} \tag{5}$$

Equations (1) and (3) in conjunction with equations (2) and (5) represent a fundamental-frequency model of the HVDC system of Fig. 5.1 in the *abc* frame [9-10].

B. System model in dq Frame

The AC System-k variables are transferred to a *dq* frame by [9]

$$f_{dqk} = K_k f_{abck} \tag{6}$$

Transformation matrix K_k is

$$K_k = \frac{2}{3}\begin{bmatrix} \cos\theta_k & \cos(\theta_k - \frac{2\pi}{3}) & \cos(\theta_k + \frac{2\pi}{3}) \\ \sin\theta_k & \sin(\theta_k - \frac{2\pi}{3}) & \sin(\theta_k + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{7}$$

Where $\theta_k(t) = \int_0^t \omega_k(t)dt$.

Transforming variables of AC System-k, as given by (1) and (2), based on (6), we deduce

$$\begin{cases} v_{tdk} = R_k i_{dk} + L_k\frac{di_{dk}}{dt} - L_k\omega_k i_{qk} + v_{sdk} \\ v_{tqk} = R_k i_{qk} + L_k\frac{di_{qk}}{dt} + L_k\omega_k i_{qk} + v_{sqk} \end{cases} \tag{8}$$

In (8), i_{dk} and i_{qk} are the *d* and *q* current components of AC System-k, and v_{tdk} and v_{tqk} are given by :

$$\begin{cases} v_{tdk} = \frac{1}{\sqrt{3}}m_k V_{dc}\cos(\alpha_k) \\ v_{tqk} = \frac{1}{\sqrt{3}}m_k V_{dc}\sin(\alpha_k) \end{cases} \tag{9}$$

Where m_k and α_k are

$$\alpha_k = \tan^{-1}\left(\frac{v_{tqk}}{v_{tdk}}\right) \qquad m_k = \frac{\sqrt{3}\sqrt{v_{tdk}^2 + v_{tqk}^2}}{V_{dc}} \tag{10}$$

Substituting for i_{abck} from (6) in (5), we deduce

$$i_{dck} = \frac{3}{2\sqrt{3}}m_k(i_{qk}\sin\alpha_k + i_{dk}\cos\alpha_k) \tag{11}$$

Substituting for i_{dck} from (11) in (3) yields

$$\begin{aligned} C_{eq}\frac{dV_{dc}}{dt} = -\frac{v_{dc}}{R_p} - \frac{3}{2}m_1(i_{q1}\sin\alpha_1 + i_{d1}\cos\alpha_1) \\ -\frac{3}{2}m_2(i_{q2}\sin\alpha_2 + i_{d2}\cos\alpha_2) \end{aligned} \tag{12}$$

Equations (8) and (12) represent a *dq* model of the HVDC system that is used for design of the DC- and AC-side controllers [9-10].

3. Controllers structure for VSC-HVDC

The controls of a VSC-HVDC system is basically the control of the transfer of energy with independent control of active and reactive power and also keep the DC link voltage at the desired level to support the required active and reactive power commands [10-11-12].

C. AC-side current control

Modulation index and phase angle of the modulating waveform are the control parameters of each VSC unite of Fig. 5.1. *d* and *q* components of the terminal voltage of VSCs units, based on (5.22), are decoupled through the following change of variables [10]

$$\begin{cases} v_{tdk} = u_{dk} - L_k\omega_k i_{qk} + v_{sdk} \\ v_{tqk} = u_{qk} - L_k\omega_k i_{dk} + v_{sqk} \end{cases} \tag{13}$$

u_{dk} and u_{qk} are new control signals that are generated by two independent PI-controllers .

The *d*-axis PI-controller is defined by

$$u_{dk} = K_{ipk}e_{dk} + K_{iik}\int_0^t e_{dk}dt \tag{14}$$

Where $e_{dk} = i_{drefk} - i_{dk}$

The *q*-axis current controller is designed in a similar manner.

D. DC-Bus Voltage Control

To control v_{dc}, we use (12). Multiplying both sides of (12) by ($C_{eq}v_{dc}$) yields: [10]

$$\begin{aligned} \frac{d(\frac{1}{2}C_{eq}v_{dc}^2)}{dt} = -\frac{v_{dc}^2}{R_p} - \frac{3}{2\sqrt{3}}v_{dc}m_1(i_{q1}\sin\alpha_1 + i_{d1}\cos\alpha_1) \\ -\frac{3}{2\sqrt{3}}v_{dc}m_2(i_{q2}\sin\alpha_2 + i_{d2}\cos\alpha_2) \end{aligned} \tag{15}$$

Substituting for v_{tdk} and v_{tdk} from (9), into (15), we obtain

$$\begin{aligned} \frac{d(\frac{1}{2}C_{eq}v_{dc}^2)}{dt} = -\frac{V_{dc}^2}{R_p} - \frac{3}{2}(v_{td1}i_{d1} + v_{tq1}i_{q1}) \\ -\frac{3}{2}(v_{td2}i_{d2} + v_{tq2}i_{q2}) \end{aligned} \tag{16}$$

The left side of (16) is the rate of energy variations in v_{dc}^2/R_p is the power dissipation in R_p. Terms $3/2(v_{td1}i_{d1}+v_{tq1}i_{q1})$ and $3/2(v_{td1}i_{d1}+v_{tq1}i_{q1})$ in (16) represent the instantaneous outgoing powers at the AC-side terminals of VSC-1 and VSC-2, respectively.

$$\frac{3}{2}(v_{td1}i_{d1} + v_{tq1}i_{q1}) = \frac{3}{2}v_{sd1}i_{d1} \tag{17}$$

If the total instantaneous power of the interface reactors are neglected, then $3/2(v_{td1}i_{d1}+v_{tq1}i_{q1})=3/2v_{sd1}i_{d1}$. Real and reactive power components delivered to each AC system are given by

$$P_2 = -P_1 \approx \frac{3}{2} v_{sd} i_{Pxref} \quad , \quad Q_k = -\frac{3}{2} v_{sd} i_{qrefk} \tag{18}$$

Thus, (16) is reduced to a Single-Input Single-Output (SISO) system described by (19)

$$\frac{d(\frac{1}{2}C_{eq}v_{dc}^2)}{dt} = -\frac{V_{dc}^2}{R_p} - \frac{3}{2}v_{sd1}i_{d1} - \frac{3}{2}v_{sd2}i_{d2} \tag{19}$$

Assuming $v_{sd} = v_{sd1} = v_{sd2}$, we have

$$\frac{d(\frac{1}{2}C_{eq}v_{dc}^2)}{dt} = -\frac{V_{dc}^2}{R_p} - \frac{3}{2}v_{sd}(i_{d1} - i_{d2}) \tag{20}$$

We define the d-axis current references i_{dref1} and i_{dref2}, as

$$\begin{cases} i_{dref1} = -i_{Pxref} + i_{Vcref} \\ i_{dref2} = i_{Pxref} + i_{Vcref} \end{cases} \tag{21}$$

Where i_{Pxref} is the current command corresponding to the desired power exchange between AC System-1 and AC System-2. A positive i_{Pxref} means a positive power flow command from AC System-1 to AC System-2. i_{Vcref} commands the small real current drawn from the both AC systems to compensate for the losses represented by R_p, and, thus, to regulate the DC-bus voltage. i_{Vcref} must be determined by a PI-controller for zero steady-state error. Thus, a DC-bus voltage controller is suggested as [10-15]

$$i_{vcref}(s) = \frac{K_{vp}s + K_{vi}}{s} e_v(s) \tag{23}$$

Where: $e_v = v_{dcref}^2 - v_{dc}^2$

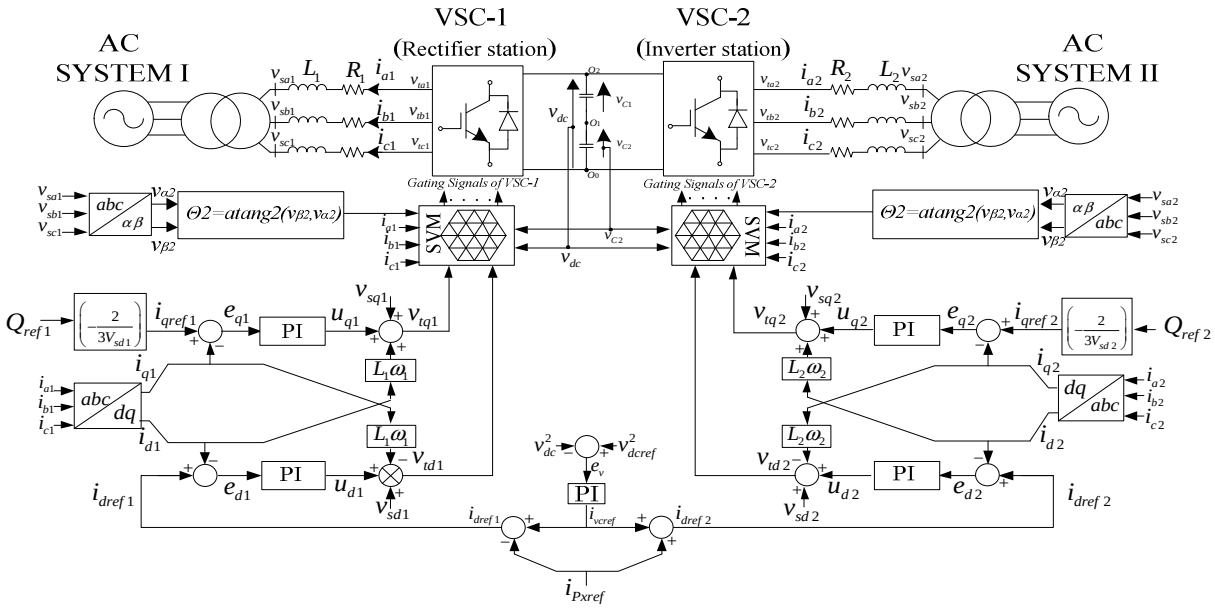

Fig. 2. Control structure of the three levels VSC-HVDC system

4. Three-Level Space Vector Modulation

A three-level converter differs from a conventional two-level converter in that it is capable of producing three different levels of output phase voltage, With three possible output states for each of the three phases, there are a total of 27 (3^3) possible switch combinations. The result of plotting each of the output voltages in a $\alpha\beta$ reference frame is shown in Fig. 3.

Fig. 4 shows that the 27 switch combinations result in a total of 19 unique voltage vectors since some of the combinations produce the same voltage vector. These different combinations relate to different ways of connecting the VSCs to the DC bus that result in the same voltage being applied to AC systems. Projection of the vectors on a $\alpha\beta$ coordinates forms a two-layer hexagon centered at the origin of the $\alpha\beta$ plane. Zero voltage vectors are located at the origin of the plane. The switching states are illustrated by 0, 1 and 2 which denote corresponding switching states. Any sampling instant the tip of the voltage vector is located in a triangle formed by three switching vectors nearest to the voltage vector (Fig. 3). The nearest three vectors are chosen by determining the triangle within the vector space in which the desired voltage vector resides.

The required on duration of each of the vectors is determined by Equations (24). These specify that the demand vector, v_{ref}, is the geometric sum of the chosen three vectors (v_1, v_2, v_3) multiplied by their on-durations (d_1, d_2, d_3) and that their on- durations must fill the complete cycle.

$$\begin{cases} v_1 d_1 + v_2 d_2 + v_3 d_3 = v_{ref} T \\ d_1 + d_2 + d_3 = T \\ v_{ref} = |v_{ref}| e^{j\theta}, \theta = \angle v_{ref} \end{cases} \tag{24}$$

The next step is to identify the appropriate redundant switching states and generate the switching pattern to control voltages of the capacitors. This requires knowledge of phase currents and impacts of different switching states on dc-side intermediate branch currents and consequently capacitor voltages [14-15-16].

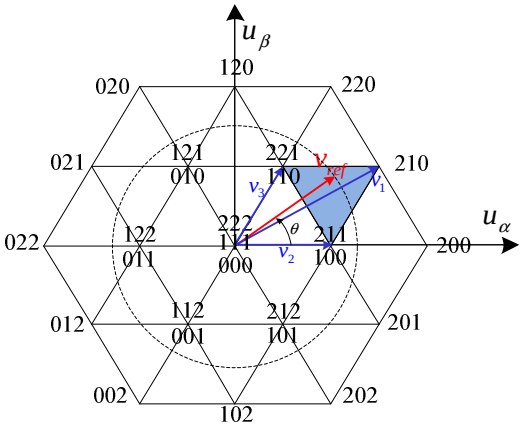

Fig. 3. Space vector diagrams of three-level converter.

5. DC-capacitor voltages balancing strategy

In a three-phase three-level VSC converter, the total energy E of DC-link capacitors is:

$$E = \frac{C}{2}(v_{C1}^2 + v_{C2}^2) \tag{25}$$

When all capacitor voltages are balanced, the total energy E reaches its minimum of $E_{\min} = Cv_{dc}^2/4$, [7-8]. This condition is called the minimum energy property which can be used as the basic principle for dc-capacitor voltage balancing and control. The adopted control method should minimize the quadratic cost function J associated with voltage deviation of the DC-capacitors [17]. The cost function is defined as follows:

$$J = \frac{C}{2}\left(\Delta v_{C1}^2 + \Delta v_{C2}^2\right) \tag{26}$$

Where: $\Delta v_{Cj} = v_{Cj} - \frac{v_{dc}}{2}, \quad j = 1,2$

Based on proper selection of redundant switching states of both VSC units, J can be minimized, if capacitor voltages are maintained at voltage reference values of $v_{dc}/2$. The mathematical condition to minimize J is:

$$\Delta v_{C_2}(\bar{i}_{x1}(k) + \bar{i}_{x2}(k)) \geq 0 \tag{27}$$

Where Δv_{C2} is the voltage drift at sampling period k. Currents components $x = 1,2,3$ are computed for different combinations of adjacent redundant switching states over a sampling period and the best combination which maximize (27) is selected [17-18].

6. simulation analysis and results

To evaluate the performance of the overall HVDC system of Fig. 1 with the parameters presented in table 1 [10], including power and control subsystems, under various dynamic operating scenarios, and the proposed SVM technique with DC-capacitor voltage-balancing strategy, a numeric simulations were carried out using the presented models implemented in MATLAB™/SIMULINK software. The system was simulated during 2.0 s.

Simulation Parameters

Parameters of the Study System	Value
Each DCC nominal power	110 MW
Each AC system nominal voltage	138 kV
Nominal Frequencies f_1	60 Hz
Nominal Frequencies f_2	50 Hz
Each transformer voltage ratio	138 / 30 kV
R_1 and R_2	40 mΩ
L_1 and L_2	6 mH
Nominal net DC voltage	30 kV
Resistance R_p	1.8 KΩ
VSC-1 sampling frequency	2520 Hz
VSC-2 sampling frequency	2520 Hz
DC-link Capacitor C_1 ,C_2	2000 µF

A. *Real and reactive power control*

Initially, the system is in a standby mode of operation and v_{dcref} is set to 30 kV. Both VSCs units operate at unity power factor. At t = 0.07 s up to 0.7 s, P_{ref2} is changed as a step corresponding to a power change from 0 to 10 Mw, from AC system-1 to AC System-2. At t = 0.7 s, P_{ref2} is ramped from 10 Mw to -10 Mw; this change corresponds to a power flow reversal from 10 Mw to -10 Mw, from AC system-2 to AC system-1.

at t = 0.5 s, reactive power demands of AC systems 1 are changed from 0 to -5 *Mvar* and from 0 to -3 *Mvar* for AC System-2.

Fig. 2.a shows the DC voltage response, we can observe that the DC-bus voltage is maintained close to its reference with good approximation, stability and without overshoot, it is important also to note that the application of the proposed redundant vectors based three-level SVM control maintains capacitors voltages (shows in fig 2.b) balanced to their references of $v_{dc}/2$.

Figs. 2.d and 2.g shows dynamic response of the system under various steps changes in real and reactive power demands of the HVDC system. We can show that real and reactive power of AC system 1 and AC system 2 after a short overshooting are regulated at the corresponding references, and are well decoupled from each other.

B. *Control system performance during faults*

Short-circuit faults in the grid are likely the most severe disturbance for the VSC- HVDC link. The resulting voltage dips at the converter terminals will severely hamper the ability of the link to transfer power. This may even lead to tripping of the link [3].

At 1.2 s, a single-phase-to-ground fault (Unbalance Fault) is made in phase *a* at the rectifier side, which drops the AC bus voltage on the faulted phase to ground during the time interval 1.2 s to 1.3 s. As shown in Fig 4.c, the voltages at inverter side (shown in Fig 4.f) are not affected by the unbalanced voltage at the rectifier side. The voltage in the faulted phase *a* at rectifier side is dropped to 100 V. during the fault and the other two phases have maximum value is about 18 kV during the fault. At inverter side the phase currents in the faulted phase *a* is increased about 300A. from 500 A to 800 A. in this case. The corresponding active power at inverter side is reduced during the fault, but the reactive power at inverter side does not change. The DC side voltage is well controlled except for the transient caused by the fault.

A three-phase-to-ground fault (balanced Fault) is applied at rectifier side at 1.6 s and is cleared at 5 cycles after the fault. The AC voltage at inverter side is maintained to 15 kV except small oscillations during the fault. The AC voltage at rectifier side is decreased to 1kV during the fault and recovers fast and successfully to the reference voltage after clearing the fault. The real power flow is reduced to very low value during the fault. The DC voltage during the fault has some oscillations at the beginning of the fault and at clearing the fault, and its maximum transient value is about 3.03 kV. So the operation of the VSC-HVDC is as expected. On the other hand, the phase currents at inverter side decrease to low values to reduce the power flow. The phase currents at rectifier side increase from 200 A to 350 A, and have overcurrent transient at the beginning of the fault.

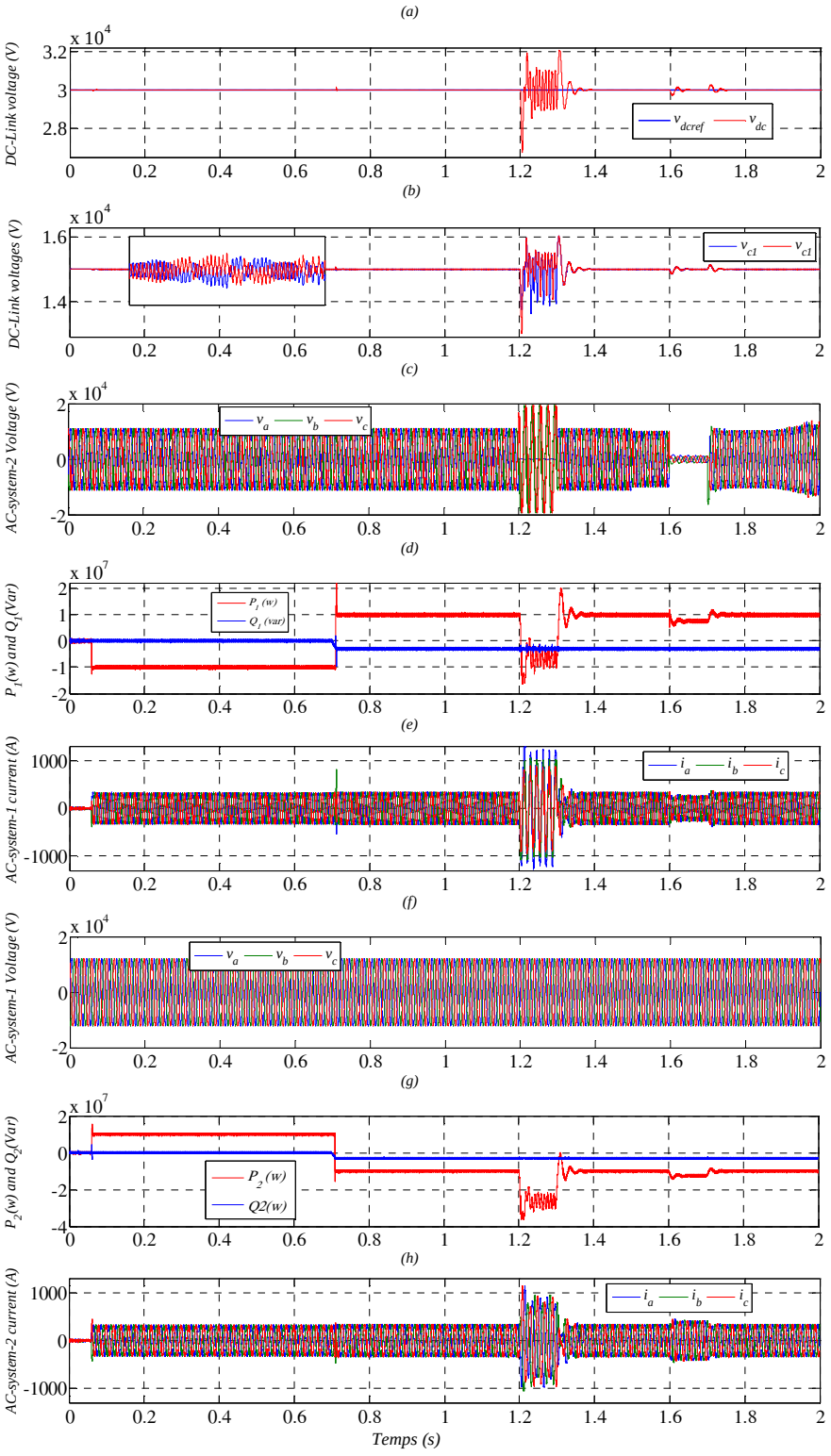

Fig. 4. - Dynamic response of VSC-HVDC system to a step changes in active/reactive power demands and system performance under faults condition

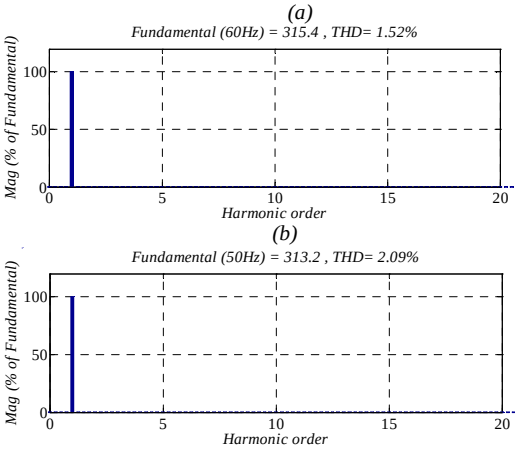

Fig 5. - Harmonic spectrum of line current
(a) for 60Hz AC-system-1 side
(b) for 50Hz AC-system-2 side

Fig 5.a and 5.b demonstrate that the distortion in supply current with lower THD level is obtained using proposed space vector modulation method.

7. Conclusion

In this paper we have presented the analysis and simulation of three levels Back-to-Back VSC-HVDC system using space vector modulation not only under normal operating conditions but also under balanced and unbalanced faults condition. The capability of the voltage-balancing SVM strategy, performance of the designed controllers, and also the overall performance of the HVDC system are investigated based on time-domain simulation studies, in the MATLAB™/SIMULINK environment. The studies conclude that the DC voltage balancing strategy prevents the voltage drift phenomenon of the DC-link capacitors of the HVDC system, even for the worst case scenario.

References

[1] Flourentzou, N. , Agelidis, V.G. , Demetriades, G.D. *"VSC-Based HVDC Power Transmission Systems: An Overview"* IEEE Trans. on Power Electronics, Vol.24 , Issue: 3, March 2009, pp. 592 – 602 .

[2] M. Bahrman and B. Johnson, *"The ABCs of HVDC transmission technology"*IEEE Power Energy Mag., vol. 5, no. 2, pp. 1057–1069, Mar.–Apr. 2007.

[3] J. Arrillaga, Y.H. Liu, N.R. Watson, "*Flexible Power Transmission. The HVDC Options*", J. Wiley and Sons Ltd., 2007.

[4] V. G. Agelidis, D. Demetriades, and N. Flourentzou, "*Recent advances in high-voltage direct-current power transmission systems*" in Proc. IEEE Int. Conf. Ind. Technol., pp. 206–213. Dec. 2006.

[5] A. Nabae, I. Takahashi, and H. Akagi, *"A new neutral point clamped PWM inverter"*, IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

[6] Yushu Zhang, GP Adam, TC Lim, SJ Finney and BW Williams, *"Voltage Source Converter in High Voltage Applications: Multilevel versus Two-level Converters"*, IET AC/DC Conference, 2010.

[7] J. Rodriguez, J. Lai, and F. Z. Peng, "*Multilevel inverters: A survey of topologies, controls, and applications*", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[8] Minyuan Guan, Zheng Xu , *"Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions"* , IEEE Trans. on Power Electronics, Vol.27 , Issue: 12 ,pp. 4858 – 4867, Dec. 2012.

[9] Saeedifard, M. , Iravani, R. *"Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System"*, IEEE Trans. on Power Delivery, Vol.25 , Issue: 4 , pp. 2903 – 2912, Oct. 2010 .

[10] B. Parkhideh,S. Bhattacharya *"A Practical Approach to Controlling the Back-to-Back Voltage Source Converter System"*, Industrial Electronics, 34th Annual Conference of IEEE, 10-13 Nov. 2008, pp. 514 - 519 , Orlando, FL,USA.

[11] M. Chavesa, E.Margatoa ,J. Fernando, F. Pintoa, J. Santanaa, *"HVDC transmission systems: Bipolar Back-to-Back diode clamped multilevel converter with fast optimum-predictive control and capacitor balancing strategy "*, Electric Power Systems Research 81 2011, pp. 1436–1445.

[12] J. Glasdam, J. Hjerrild, L.H. Kocewiak, C.L. Bak, "*Review on multi-level voltage source converter based HVDC technologies for grid connection of large offshore wind farms"*, Power System Technology (POWERCON), IEEE International Conference, Oct. 30 2012-Nov. 2 2012 pp.1-6, Auckland,USA.

[13] A. Tyagi,K.R. Padiyar, *"Dynamic analysis and simulation of a VSC based Back-to-Back HVDC link"*, Power Electronics, IICPE, 19-21 Dec. 2006. pp 232 – 238, Chennai, india.

[14] M, Saeedifard,R. Iravani, R., Pou, J. *"A space vector modulation strategy for a Back-to-Back five-level HVDC converter system"*, IEEE Trans. Ind. Electron., 2009, 56, pp. 452–466.

[15] M.Bouzidi, A.Benaissa, S.Bakat, A.Djerioui, "Application of Backstepping to the Virtual Flux Oriented Control for Three- Phase Shunt Active Power Filter", *Journal of Electrical Engineering*. Vol. 13 . Edi. 4 , pp. 308-315, 2013 .

[16] N. Kimura, A. Kouno, T. Morizan, and K. Taniguchi, "*Suppression of harmonics of multi-level converter applied for Back-to-Back HVDC link"*, in Proc. Power Convers. Conf., Apr. 2002, vol. 3, pp. 1132–1137.

[17] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, *"Voltage balancing control of diode-clamped multilevel converters with passive front-ends"*, IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1751‑1758, Jul. 2008.

[18] H.A. Hotait, A.M. Massoud, S.J. Finney, B.W. Williams, *"Capacitor Voltage Balancing Using Redundant States of Space Vector Modulation for Five-Level Diode Clamped Inverters"*, IET Power Electronics, vol. 3 n. 2, May 2010, pp. 292–313.