HIGH GAIN NON ISOLATED DC-DC STEP UP CONVERTERS INTEGRATED WITH ACTIVE AND PASSIVE SWITCHED INDUCTOR NETWORKS

M. Al MAMUN **Mehedi Azad SHAWON**
Department of Electrical and Electronic Engineering, Southeast University, Dhaka-1208, Bangladesh
mamuniut09@gmail.com mashawon@seu.ac.bd

Golam SAROWAR **Md. Ashraful HOQUE**
Department of Electrical and Electronic Engineering, Islamic University of Technology (IUT), Gazipur, Bangladesh
asim@iut-dhaka.edu mahoque@iut-dhaka.edu

Abstract: *High gain dc-dc step up converters have been used in renewable energy systems, for example, photovoltaic grid connected system and fuel cell power plant to step up the low level dc voltage to a high level dc bus voltage. If the conventional boost converter is to meet this demand, it should be operated at an extreme duty cycle (duty cycle closes to unity), which will cause electromagnetic interference, reverse recovery problem and conduction loss at the power switches. This paper proposes a class of non-isolated dc-dc step up converters which provide very high voltage gain at a small duty cycle (duty cycle < 0.5). Firstly, the converter topologies are derived based on active switched inductor network and combination of active and passive switched inductor networks; secondly, the modes of operation of proposed active switched inductor converter and combined active and passive switched inductor converter are illustrated; thirdly, the performance of the proposed converters are analyzed mathematically in details and compared with conventional boost converter. Finally, the analysis is verified by simulation results.*

Key words: *Step up converter, Non isolated converter, High gain, DC-DC converter, Switched inductor network, Duty cycle*

1. Introduction

The demand for energy is increasing with the development of society. The use of fossil fuels (coal, oil, gas etc.) to meet this growing demand has affected the environment adversely by causing environmental pollution and greenhouse effect. Moreover, the storage of fossil fuels in the earth is decreasing day by day due to its increased usage. Hence, the necessity of new, clean and renewable energy has emerged greatly to replace the traditional fossil fuel energy. Power generation by photovoltaic (PV) and fuel cell systems have shown good signs of future success as they have been applied on a broad scale [1]-[6].

However, the output voltages of PV and fuel cells range between 20 V to 40 V which is very low. A typical fuel cell power plant [7] is depicted in Fig. 1. To maintain the line voltage of 220 V in a single phase system, the grid-connected inverter needs the dc bus voltage at 380 V which is approximately 20 times the fuel cell output voltage. Thus, a dc-dc step up converter with a very high voltage gain is needed to boost the outputs of PV and fuel cells. To accomplish this, the conventional boost converter must operate at extreme duty cycle (duty cycle closes to unity) which leads to electromagnetic interference, reverse recovery problem, high conduction loss at the switches etc.

Different isolated and non-isolated topologies have been developed to obtain high gain at low duty cycle. Isolated converters involve transformer where the turns ratio of the transformer is adjusted to so that a high gain is obtained [8]-[12]. However, a large turn ratio leads to a large leakage inductance which causes high voltage spike across the switches [13]-[15]. Besides, isolated converters becomes costly due to its multi-stage AC/DC/AC conversion and isolated sensors and controllers.

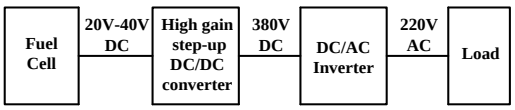


Fig. 1. Fuel cell power plant with different power stages

The existing non-isolated converters are normally of coupled inductor type and non-coupled type. The coupled inductor converters adjust the output voltage gain by controlling the turns ratio of the coupled inductor which is similar to the isolated converters [16]-[19]. Thus, the leakage inductance and, as a consequence, the voltage spike across the switches do exist prominently. The non-coupled inductor converters can minimize this issue by removing the magnetic components with a comparatively high voltage gain [20]-[23]. High voltage gain is also achieved in cascade converter but it offers large and

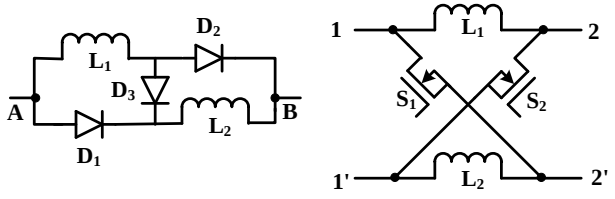
complex circuitry. The transformer less converter in [24] can provide a high voltage gain with reduced voltage stress across the switches. However, the gain is not that much high to achieve 20V/380V conversion.

Researchers have developed different switched inductor and switched capacitor networks to increase the voltage level [24]. Series and parallel connections of these networks make it possible to obtain higher voltage gain. However, the voltage gain is still lower to meet the demand of high voltage gain. Moreover, the circuitry becomes complex and expensive.

This paper presents a novel class of high gain non-isolated dc-dc step up converters integrated with active and passive switched inductor networks. Proposed converters offer very high voltage gain at a small duty cycle i.e. duty cycle < 0.5 which reduces the electromagnetic interference, reverse recovery problem and conduction loss of the switches. Moreover, a single control signal is used for all the switches which reduces the circuit operation complexity. The operating principle and the steady state analysis of the proposed converters are presented in details for equal inductances. Finally, the simulation results by PSIM 9.0 are provided to verify the analysis.

2. Topological derivation of proposed converters

Fig. 2 shows the active switched inductor (A-SL) and passive switched inductor (P-SL) networks presented in [23]-[24].



(a) (b)

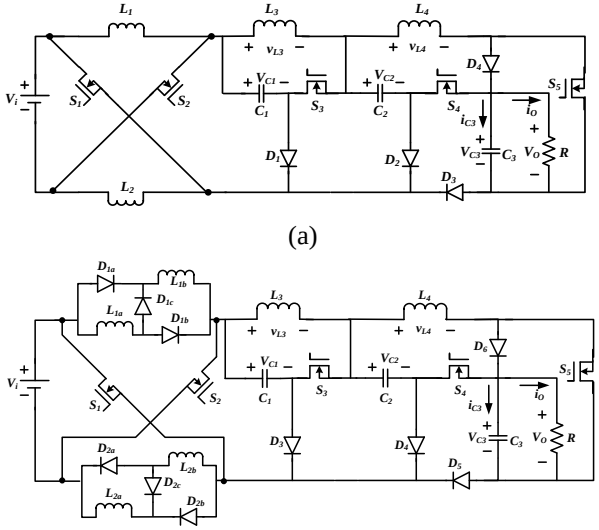
Fig. 2. Switched inductor networks (a) passive switched inductor network (b) active switched inductor network

The passive switched inductor (P-SL) network consists of two inductors L_1, L_2 and three diodes D_1, D_2 and D_3. When the voltage difference across the terminals A and B (V_{AB}) is positive, D_1 and D_2 become forward biased, and D_3 becomes reverse biased. As a result, inductors L_1 and L_2 are in parallel connection. When the voltage difference across the terminals A and B (V_{AB}) is negative, D_1 and D_2 become reverse biased, and D_3 becomes forward biased. This put the inductors L_1 and L_2 in series connection.

The active switched inductor (A-SL) network consists of two inductors L_1, L_2 and two switches S_1, S_2. Both of the switches operate simultaneously. When the switches S_1 and S_2 are turned on, inductors L_1 and L_2 become parallel connected. When they are turned off, inductors L_1 and L_2 become series connected across the input terminals 1-1' of the two port network if a load is connected across the terminals 2-2'.

The proposed converters derived from [25] are obtained by applying the above A-SL and P-SL networks. The proposed converters are shown in Fig. 3.

The inductors in the P-SL and A-SL networks are of equal inductance. Power switches share the same switching signals which makes the control easy. When all the switches are turned on simultaneously, the inductors in the P-SL and A-SL networks operate in parallel connection and are charged by the power source, and when all the switches are turned off simultaneously, inductors operate in series connection and are discharged to load.



(a)

(b)

Fig. 3. Proposed converters (a) proposed converter with A-SL network (b) proposed converter combined with P-SL and A-SL networks

3. Operations of proposed converters

A. Operation of proposed converter with A-SL network

The proposed converter with A-SL network in Fig. 3(a) involves four inductors (L_1, L_2, L_3 and L_4), three capacitors (C_1, C_2 and C_3), four diodes (D_1, D_2, D_3 and D_4) and five high frequency controlled switches (S_1, S_2, S_3, S_4 and S_5). MOSFETs are used as the high frequency controlled switches and these are operated based on a single duty cycle. V_i represents the low dc input voltage from PV source or fuel cell. The resistive load is connected across the capacitor C_3. The equivalent circuit in CCM operation is shown in Fig. 4.

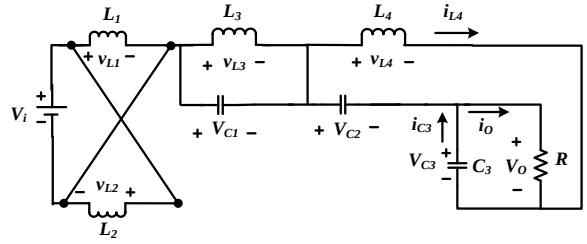
Mode 1 [$0 - DT_S$]: All the five switches are

turned on during this time interval. The equivalent circuit is shown in Fig. 4(a). Inductors L_1 and L_2 are energized in parallel by the supply voltage V_i. Also, L_3 and L_4 are energized during this period. Capacitors C_1, C_2 and C_3 are discharged. All the diodes D_1, D_2, D_3 and D_4 are reverse biased. The load is supplied by the capacitor C_3. As L_1 and L_2 are in parallel connection, $v_{L1} = v_{L2}$. The voltages across the inductors L_1, L_2, L_3 and L_4 are expressed as:

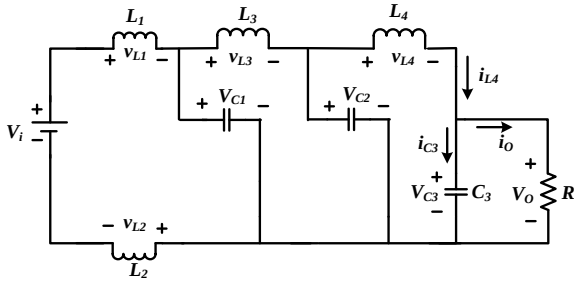
$$v_{L1} = v_{L2} = V_i,\ v_{L3} = V_{C1},\ v_{L4} = V_{C2} + V_{C3} \quad (1)$$

Mode 2 [$DT_S - T_S$]: All the four switches are turned off during this time interval. The equivalent circuit is shown in Fig. 4(b). Inductors L_1 and L_2 are discharged in series. Also, L_3 and L_4 are discharged. Capacitors C_1, C_2 and C_3 are charged by the inductors. All the diodes D_1, D_2, D_3 and D_4 are forward biased. The load is supplied by the inductor L_4. As an identical current flows through L_1 and L_2, $v_{L1} = v_{L2}$. The voltages across the inductors are expressed as:

$$v_{L1} = \frac{V_i - V_{C1}}{2},\ v_{L3} = V_{C1} - V_{C2},\ v_{L4} = V_{C2} - V_{C3} \quad (2)$$



(a)



(b)

Fig. 4. Equivalent circuit of proposed converter with A-SL network in CCM (a) when all the switches are on (b) when all the switches are off

The volt-second balance of v_{L1} is given by,

$$V_i\, DT_S = -\left[\frac{V_i - V_{C1}}{2}\right](1 - D)T_S$$

Or,

$$V_{C1} = \frac{V_i\,(1+D)}{1-D} \quad (3)$$

Similarly, volt-second balance of v_{L3} is given by,

$$V_{C1}\, DT_S = -\,(V_{C1} - V_{C2})\,(1 - D)T_S$$

Or,

$$V_{C2} = \frac{V_{C1}}{1-D} = \frac{V_i\,(1+D)}{(1-D)^2} \quad (4)$$

Similarly, volt-second balance of v_{L4} is given by,

$$(V_{C2} + V_{C3})\, DT_S = -\,(V_{C2} - V_{C3})\,(1 - D)T_S$$

Or,

$$V_{C3} = \frac{V_{C2}}{1-2D} = \frac{V_i\,(1+D)}{(1-D)^2(1-2D)} = V_O \quad (5)$$

Therefore, the voltage gain in Continuous Conduction Mode is:

$$G_{CCM} = \frac{(1+D)}{(1-D)^2(1-2D)} \quad (6)$$

Voltage stress across the diodes are found as:

$$\begin{cases} V_{D1} = V_i + V_{C1} \\ V_{D2} = V_i + V_{C1} + V_{C2} \\ V_{D3} = V_i + V_{C1} + V_{C2} + V_{C3} \\ V_{D4} = V_{C3} \end{cases} \quad (7)$$

Voltage stress across the switches are found as:

$$\begin{cases} V_{S1} = V_{S2} = \frac{V_i + V_{C1}}{2} \\ V_{S3} = V_{C2} \\ V_{S4} = V_{S5} = V_{C3} \end{cases} \quad (8)$$

The equivalent circuit in DCM is shown in Fig. 5 and the analysis is given below.

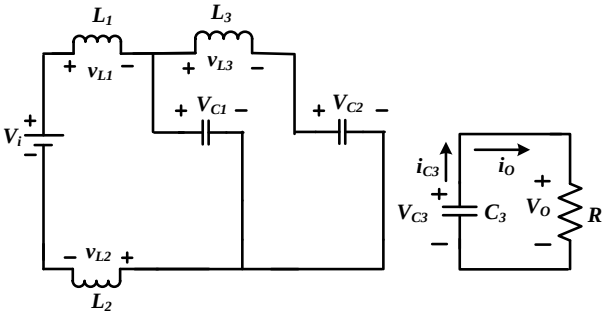


Fig. 5. Equivalent circuit of proposed converter with A-SL network in DCM

Mode 1 [$0 - DT_S$]: This mode is similar to Mode 1 in CCM operation. During this time, the peak current i_{L4P} through the inductor L_4 derived from Fig. 6 is:

$$i_{L4P} = \frac{V_{C2} + V_{C3}}{L_4}\, DT_S \quad (9)$$

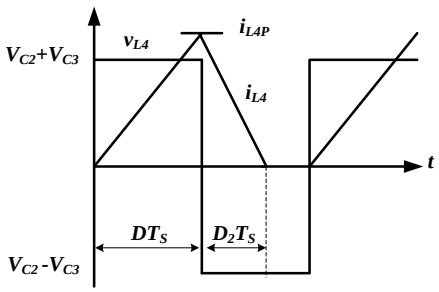


Fig. 6. v_{L4} versus i_{L4} in DCM

Mode 2 [$DT_S - (DT_S + D_2T_S)$]: This mode is similar to Mode 2 in CCM operation. During this time, the inductor current i_{L4} is decreased to zero. The peak current through the inductor L_4 can be derived from Fig. 6 as:

$$i_{L4P} = \frac{V_{C3} - V_{C2}}{L_4}\, D_2T_S \quad (10)$$

Mode 3 [$(DT_S + D_2T_S) - T_S$]: During this time interval, the equivalent circuit is shown in Fig. 5 when the load is supplied by the capacitor C_3. Combining (9) and (10), D_2 can be expressed as:

$$D_2 = \left[\frac{V_i(1+D)+V_O(1-D)^2}{V_O(1-D)^2 - V_i(1+D)}\right] D \quad (11)$$

The average current through the diode D_4 is equal to the average load current, therefore:

$$\frac{\frac{1}{2} \times D_2 T_S \times i_{L4P}}{T_S} = I_O = \frac{V_O}{R}$$

Or,

$$V_O = \frac{D2^2 V_{C2}}{D2^2 - 2\tau} \quad (12)$$

where $\tau = \frac{L_4}{RT_S}$ = time constant of L_4. Now, if $V_{C2} = \frac{V_i(1+D)}{(1-D)^2}$ is put in (12), then D_2 is deduced as:

$$D_2 = \sqrt{\frac{2\tau V_O (1-D)^2}{V_O(1-D)^2 - V_i(1+D)}} \quad (13)$$

Again, the volt-second balance of v_{L4} is given by,

$(V_{C2} + V_{C3})\, DT_S = -(V_{C2} - V_{C3})\, D_2 T_S$

Or,

$$\frac{V_{C3}}{V_i} = \frac{(D + D_2)(1 + D)}{(D_2 - D)(1 - D)^2}$$

Thus, the voltage gain in DCM is:

$$G_{DCM} = \frac{V_{C3}}{V_i} = \frac{(D+D_2)(1+D)}{(D_2 - D)(1-D)^2} \quad (14)$$

The boundary condition arises when i_{L4} decreased to zero at T_S. At boundary condition, $D_2 = (1 - D)$. Now, if we put $V_{C2} = V_{C3}(1 - 2D)$, then the time constant of L_4 at boundary condition derived from equation (13) is given by,

$$\tau_B = D\,(1 - D)^2 \quad (15)$$

The relationship between τ_B and D is shown in Fig. 7. When $\tau > \tau_B$, the converter operates in CCM and when $\tau < \tau_B$, the converter operates in DCM.

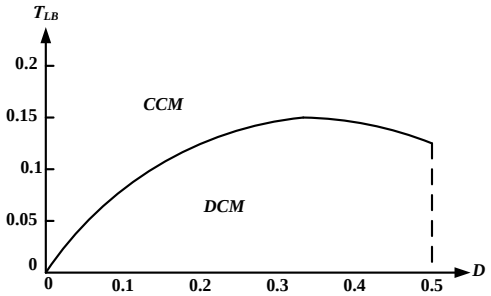


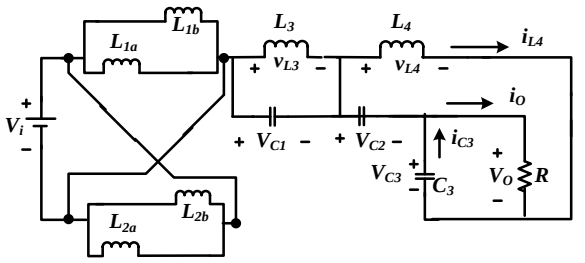
Fig. 7. Boundary condition of the converter

B. Operation of proposed converter combined with P-SL and A-SL network

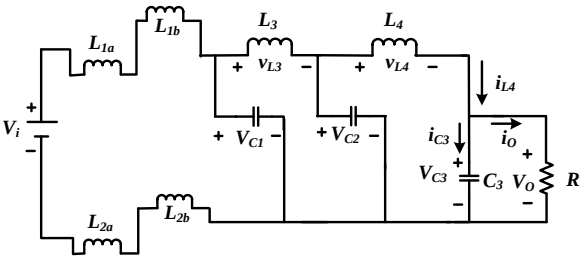
The proposed converter in Fig. 3(b) involves six inductors (L_{1a}, L_{1b}, L_{2a}, L_{2b}, L_3 and L_4), three capacitors (C_1, C_2 and C_3), ten diodes (D_{1a}, D_{1b}, D_{1c}, D_{2a}, D_{2b}, D_{2c}, D_3, D_4, D_5 and D_6) and five high frequency controlled switches (S_1, S_2, S_3, S_4 and S_5). The operation in CCM is shown in Fig. 8.

Mode 1 [$0 - DT_S$]: All the four switches are turned on during this time interval. The equivalent circuit is shown in Fig. 8(a). Inductors L_{1a}, L_{1b}, L_{2a} and L_{2b} are energized in parallel by the supply voltage V_i. Also, L_3 and L_4 are energized. Diodes D_{1a}, D_{1b}, D_{2a} and D_{2b} are forward biased and the rest of the diodes are reverse biased. The load is supplied by the capacitor C_3. As L_{1a}, L_{1b}, L_{2a} and L_{2b} are in parallel connection, $v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b}$. Now, if it is assumed that $v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b} = v_{L1}$, then the voltages across the inductors L_{1a}, L_{1b}, L_{2a}, L_{2b}, L_3 and L_4 are expressed as:

$$\begin{cases} v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b} = v_{L1} = V_i \\ v_{L3} = V_{C1} \\ v_{L4} = V_{C2} + V_{C3} \end{cases} \quad (16)$$



(a)



(b)

Fig. 8. Equivalent circuit in CCM of proposed converter combined with A-SL and P-SL networks (a) when all the switches are on (b) when all the switches are off

Mode 2 [DT_S - T_S]: During this time interval, all the switches are off. The equivalent circuit is shown in Fig. 8(b). The diodes D_{1a}, D_{1b}, D_{2a} and D_{2b} are reverse biased and rest of the diodes are forward biased. Inductors L_{1a}, L_{1b}, L_{2a} and L_{2b} are discharged in series and energize capacitors C_1, C_2 and C_3. Also, the inductors L_3 and L_4 are discharged to C_2 and C_3. The load is supplied by the inductor L_4. Due to identical current flows through L_{1a}, L_{1b}, L_{2a} and L_{2b}, $v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b}$. Now, if it is assumed that $v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b} = v_{L1}$, then the voltages across the inductors L_{1a}, L_{1b}, L_{2a}, L_{2b}, L_3 and L_4 are expressed as:

$$\begin{cases} v_{L1a} = v_{L1b} = v_{L2a} = v_{L2b} = v_{L1} = \frac{V_i - V_{C1}}{4} \\ v_{L3} = V_{C1} - V_{C2} \\ v_{L4} = V_{C2} - V_{C3} \end{cases} \quad (17)$$

The volt-second balance of v_{L1} is given by,

$$V_i\, DT_S = -\left[\frac{V_i - V_{C1}}{4}\right](1 - D)T_S$$

Or,

$$V_{C1} = \frac{V_i(1+3D)}{1-D} \quad (18)$$

Similarly, volt-second balance of v_{L3} is given by,

$$V_{C1}\,DT_S = -(V_{C1} - V_{C2})\,(1-D)T_S$$

Or,

$$V_{C2} = \frac{V_{C1}}{1-D} = \frac{V_i\,(1+3D)}{(1-D)^2} \quad (19)$$

Similarly, volt-second balance of v_{L4} is given by,

$$(V_{C2} + V_{C3})\,DT_S = -(V_{C2} - V_{C3})\,(1-D)T_S$$

Or,

$$V_{C3} = \frac{V_{C2}}{1-2D} = \frac{V_i\,(1+3D)}{(1-D)^2(1-2D)} = V_O \quad (20)$$

Thus, the voltage gain in continuous conduction mode is,

$$G_{CCM} = \frac{(1+3D)}{(1-D)^2(1-2D)} \quad (21)$$

Voltage stress across the diodes are found as:

$$\begin{cases} V_{D1c} = V_{D2c} = V_i \\ V_{D3} = V_i + V_{C1} \\ V_{D4} = V_i + V_{C1} + V_{C2} \\ V_{D5} = V_i + V_{C1} + V_{C2} + V_{C3} \end{cases} \quad (22)$$

Voltage stress across the switches are found as:

$$\begin{cases} V_{S1} = V_{S2} = \frac{V_i + V_{C1}}{2} \\ V_{S3} = V_{C2} \\ V_{S4} = V_{S5} = V_{C3} \\ V_{D1a} = V_{D1b} = V_{D2a} = V_{D2b} = \frac{V_{C1} - V_i}{4} \end{cases} \quad (23)$$

The equivalent circuit in DCM is given in Fig. 9. The analysis of DCM is similar to that of the analysis of DCM of the proposed converter with A-SL network.

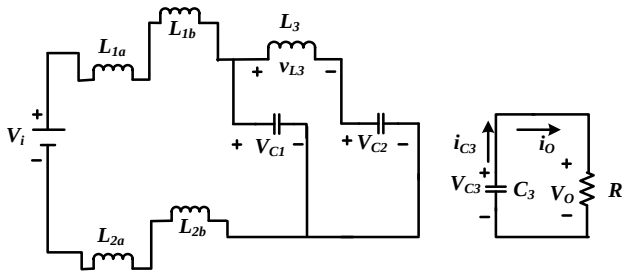


Fig. 9. Equivalent circuit of proposed converter combined with A-SL and P-SL network in DCM

If $V_{C2} = \frac{V_i\,(1+3D)}{(1-D)^2}$ is put in (12), then D_2 is deduced as:

$$D_2 = \sqrt{\frac{2\tau V_O\,(1-D)^2}{V_O\,(1-D)^2 - V_i\,(1+3D)}} \quad (24)$$

Again, the volt-second balance of v_{L4} is given by,

$$(V_{C2} + V_{C3})\,DT_S = -(V_{C2} - V_{C3})\,D_2T_S$$

Or,

$$\frac{V_{C3}}{V_i} = \frac{(D + D_2)(1+3D)}{(D_2 - D)\,(1-D)^2}$$

Therefore, the voltage gain in DCM is:

$$G_{DCM} = \frac{V_{C3}}{V_i} = \frac{(D+D_2)(1+3D)}{(D_2-D)\,(1-D)^2} \quad (25)$$

Boundary condition of this proposed converter is also similar to that of the A-SL converter. If we put $D_2 = 1 - D$ and $V_{C2} = V_{C3}(1-2D)$, then the time constant of L_4 at boundary condition derived from equation (24) is given by,

$$\tau_B = D\,(1-D)^2 \quad (26)$$

Thus, it is observed that the time constant is equal to the time constant of the proposed converter with A-SL network.

4. Analysis of the proposed converters

Table 1

Utilized components and parameters of the proposed converters and the conventional boost converter

	A-SL Converter	Combined A-SL and P-SL converter	Conventional Boost Converter
Voltage gain in CCM	$\frac{(1+D)}{(1-D)^2(1-2D)}$	$\frac{(1+3D)}{(1-D)^2(1-2D)}$	$\frac{1}{1-D}$
Duty cycle range	$0 < D < 0.5$	$0 < D < 0.5$	$0 < D < 1$
No. of Diode	4	10	1
No. of Capacitor	3	3	1
No. of Inductor	5	7	1
Maximum voltage stress across switches	$\frac{V_i\,(1+D)}{(1-D)^2(1-2D)}$ across S_4 and S_5	$\frac{V_i\,(1+3D)}{(1-D)^2(1-2D)}$ across S_4 and S_5	$\frac{1}{1-D}$
Maximum voltage stress across diodes	$V_i + \frac{V_i\,(1+D)}{1-D} + \frac{V_i\,(1+D)}{(1-D)^2} + \frac{V_i\,(1+D)}{(1-D)^2(1-2D)}$ across the diode D_3	$V_i + \frac{V_i\,(1+3D)}{1-D} + \frac{V_i\,(1+3D)}{(1-D)^2} + \frac{V_i\,(1+3D)}{(1-D)^2(1-2D)}$ across the diode D_5	$\frac{1}{1-D}$
Inductor Time constant at boundary condition	$D\,(1-D)^2$	$D\,(1-D)^2$	$D\,(1-D)/2$

The analysis of the proposed converters is performed based on voltage gain, voltage stress across the switches and diodes, inductor time constant at boundary condition and the number of passive elements. Table 1 shows the comparison between the proposed converters and the conventional boost converter.

From Table 1 it is observed that in CCM the voltage gains of the proposed converters are much higher than that of the conventional boost converter and among the three converters combined A-SL and P-SL converter gives the highest voltage gain. Inductor time constants at boundary condition in the proposed converters are identical and lower than that

of the conventional one for a certain value of duty cycle. This makes the size of the inductor smaller. Moreover, the electromagnetic interference and the conduction loss at the switches in the proposed converters are reduced due to smaller duty cycle.

However, the voltage stress across the diodes and switches in the proposed converters are higher than that of the conventional boost converter. The combined A-SL and P-SL converter suffers the highest voltage stresses across the diode D_5 and switches S_4 and S_5. Hence, the voltage ratings of these components should be higher than the other components. Moreover, the proposed converters involve more components. Therefore, if the required voltage gain is not that much high, then the proposed A-SL converter is preferred to the combined A-SL and P-SL converter because it involves lower number of components. But if an extremely high voltage gain is required, then the combined A-SL and P-SL converter is preferred to the A-SL converter.

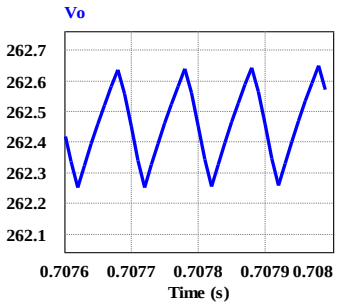
5. Simulation results

Table 2
Parameters

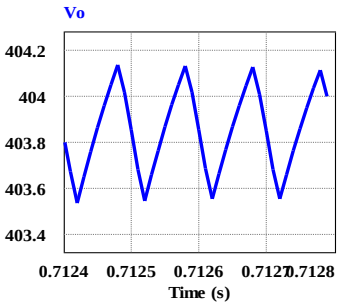
Parameters	Value
Input voltage (V_i)	20 V
Switching Frequency (f_S)	10 kHz
Inductors in A-SL and P-SL networks	1 mH
Inductor (L_3)	3 mH
Inductor (L_4)	5 mH
Capacitor (C_1)	1000 µF
Capacitor (C_2)	1000 µF
Capacitor (C_3)	1000 µF
Load across C_3	100 Ω
Duty Cycle (D)	0.369

The proposed converters are designed and implemented by using PSIM 9.0. The circuit parameters taken for the simulation are tabulated in Table 2. Mathematical calculations of the output voltages are done from (5) and (20), and these are found to be 262.46 V and 403.95 V. The simulation gives the values of output voltages very near to the calculated values with a negligible ripple content which is within prescribed tolerable limit [26]. The ripple content is controlled by controlling the value of $\boldsymbol{C_3}$. The output voltages are shown in Fig. 9.

In both of the converters maximum voltage stress occurs across the switches S_4 and S_5 and are found from (8) and (23). These are found as 262.46 V in A-SL converter and 403.95 V in combined A-SL and P-SL converter respectively. The simulation shows the values very near to the calculated values which are shown in Fig. 10.

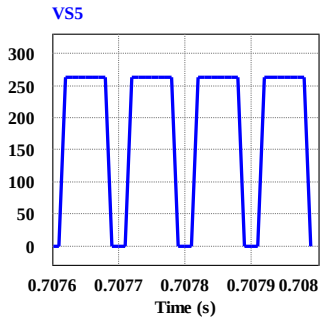


(a)

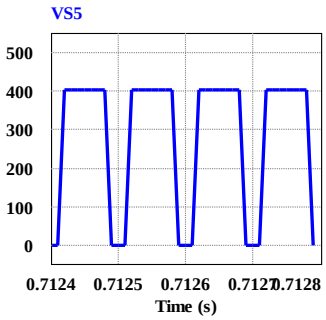


(b)

Fig. 9. Output voltages of proposed (a) A-SL converter (b) Combined A-SL and P-SL converter for same duty cycle



(a)

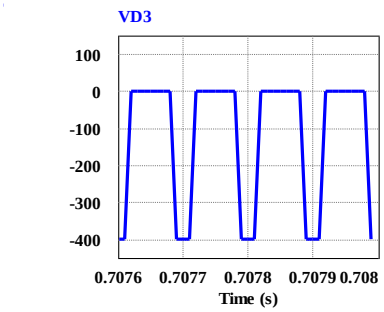


(b)

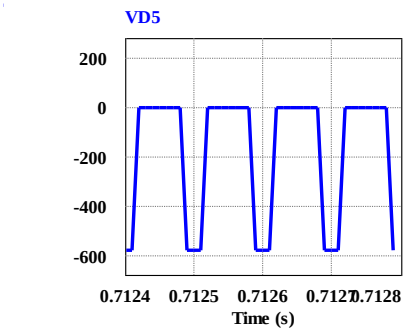
Fig. 10. Voltage across switch S_5 of (a) A-SL converter (b) Combined A-SP and P-SL converter

The maximum voltage stress across the diodes appear across D_3 and D_5 in A-SL converter and combined A-SL and P-SL converter respectively. (7) and (22) give the voltage across D_3 as 394.62 V and

voltage across D_5 as 596.57 V respectively. Calculated values are very near to the simulated values and are shown in Fig. 11.



(a)



(b)

Fig. 11. Voltage across (a) D_3 in A-SL converter (b) D_5 in combined A-SL and P-SL converter

6. Conclusion

This paper has presented a class of very high gain dc-dc step up converters based on active and passive switched inductor networks. The novel characteristics of the proposed converters are as following:

a) The proposed converters can achieve a very high voltage gain with a small duty cycle i.e. duty cycle less than 0.5 which is nearly impossible for conventional boost converter.

b) Lower inductor time constant at boundary condition which make the size of inductor smaller.

c) The electromagnetic interference problem depending upon the rate of change of current through the switch, and conduction loss of the switch are reduced due to smaller duty cycle.

d) The current stress of the inductors and voltage stress of the switches are reduced by the use of passive switched inductor networks and active switched inductor network respectively.

e) The control complexity is reduced greatly as a single control signal is used for all switches.

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