ANALYSIS OF HARMONIC MINIMIZATION FOR INTERLEAVED SYNCHRONOUS BUCK CONVERTER USING VCPFC

R.Thangam [1] S.P.Joy Vasantha Rani [2]

[1]Assistant Professor, Department of Electrical Engineering, Saveetha School of Engineering, Thandalam, Chennai

[2]Assistant Professor, Department of Electronics Engineering, Madras Institute of Technology, Chrompet

thangamr.mit@gmail.com [1]

jovinadekson@gmail.com

ABSTRACT

In this work power factor improvement and harmonic minimization for the interleaved synchronous buck converter connected through nonlinear load is proposed. The interleaved converter supplied with 240V and reaches 12V as output. The converter output always connected with nonlinearloads, causes less power factor with more harmonics. Active PLL with voltage controlled power factor controller is designed to reduce harmonics and to rise the power factor.The VCPFC controller designed using MATLAB Simulink .Controller output waveforms are examined and analyzed with other controller performances. The converter is rated with 2mA,1mH,and 1000µF values. The chopper is tested for different resistive loads and inductive loads.

Keywords: Interleaved buck converter (IBC), voltage mode control, voltage controlled power factor correction (VCPFC), Total harmonic distortion(THD), Electromagnetic interference(EMI), Phase locked loop(PLL), Unity power factor(UPF).

I.INTRODUCTION

To maintain high power quality is most important factor for all electronic devices. Providing high quality power through PFC controller in primary section power electronic chopper achieves higher efficiency. Complete study of CCB PFC controller [1] were discussed.

Rapid improvement of semiconductor products, increasing applications of power electronic products like commercial, residential purpose. Hence the power electronic products causes a reduction in power angle and increase in harmonics. To reduce this active PFC correction is important.[2]

Distributed parallel converters doesn't require centralized control and more tolerant for converter cell faults. It requires less connections inside each cell faults. If any interleaving cell fault occurs it doesn't affect the main converter work. The remaining cell will work automatically among themselves[3]. UPF rectifier provides total minimized harmonic distortion. forward converter uses single conversion stage.

Ripple in the supply current are completely reduced using buck interleaved converter. Hence this procedure more advantageous. Interleaved Converter contains two shunt connected buck converters that operates in 180˚ phase shift [4].

To obtain UPF, In SMPS ,numerous control methods are implemented.Analog controllers are implemented to get UPF at low cost [5].Analog controller uses hysteresis control technique has increased dynamic response ,greater stability to achieve increased PF and low harmonics.[6]

To Design analog controllers is costly and also implementation is difficult. Hence instead of hysteresis controller current controllers frequency based controllers were used for PFC design. The total system implemented in single chip with very low cost[10] with external multiplier included.

To remove the use of external multiplier, nonlinear control and one cycle control [11-12] were established. Digital controllers are replace all analog controllers because computational ability is improved with esteem to its Analog parts [13-14].

Digital,Analog and mixed controllers are appliedto control interleaved step down converter to produce a controlled input current,output voltagesame phase with input voltage obtaining improved PF and very less THD [15]. To decrease the ripple current produced by the power diode rectifier to achieve UPF nearer to unity and regulate the DC voltage. The scheme rectifier

connected to the PFC Buck Converter it compensates the ripple current produced by the diode. [16].

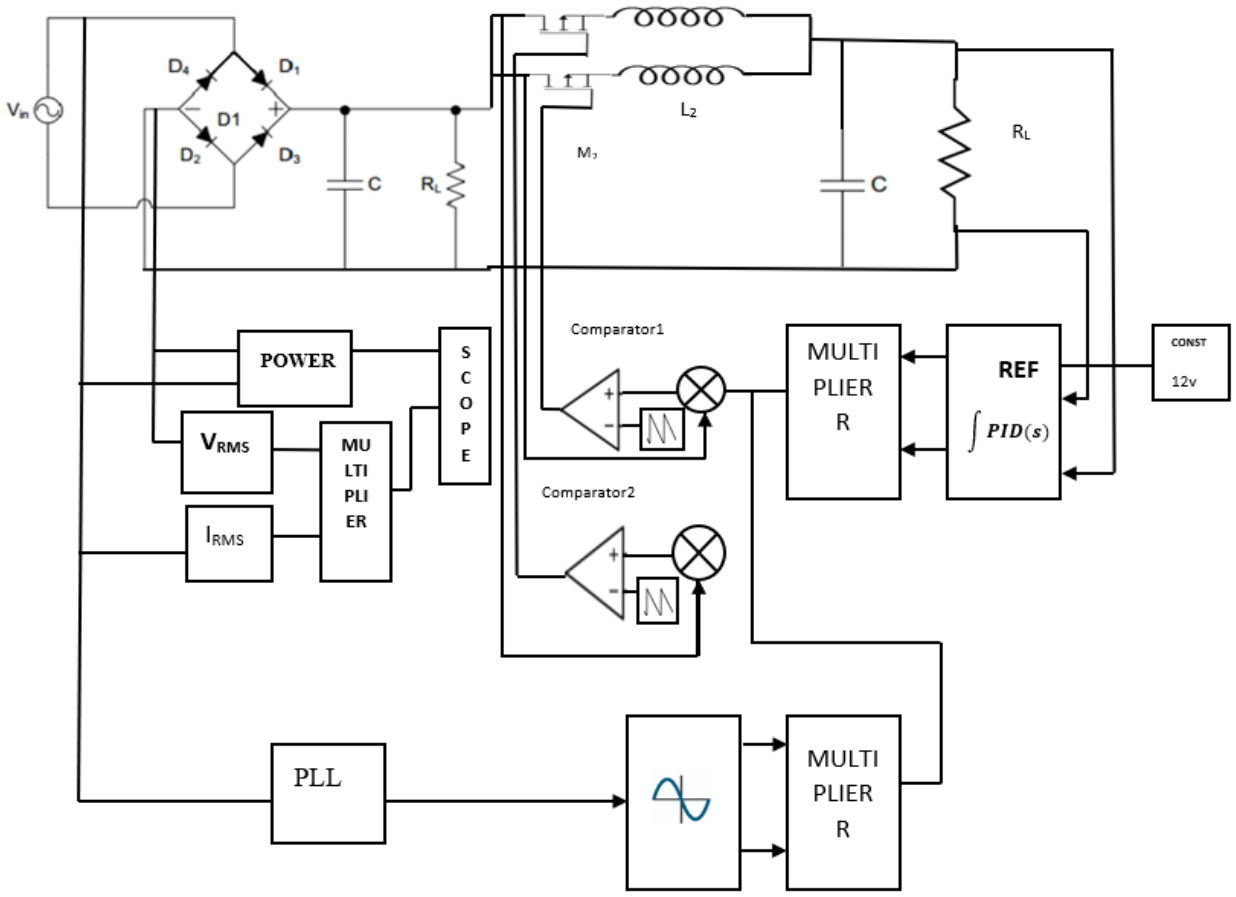


Fig.1 Two phase IBCcontrolled by PLL

The diode rectifier ripples are formed then the ripples areminimized by capacitor. During this period, the main current is highly pulsating. This initiates to the decrease in power factor value and harmonics distortion existing in main current. This involves the use of PFCis important for power electronic devices[18].
The Interleaved Converter is executed using digital PSM controller. Digital controller uses Pulse skipping technique for to produce the pulses. Mathematical designing of Interleaved Converter and stability study of converter was discussed[19].

The proposed Digital pulse skipping controller supports to attain a controlled output voltage against all harmonics and disturbances in load. The Simulink model coversto the design control circuit without and with PFCimprovement circuit modelled using MATLAB/Simulink. It has been observed from the outputTHD of input current wasminimized effectively and the phase angle between voltage and current also reduced[20].

The subsequent section gives the details of basic concepts of IBC ,design specifications of IBC, mathematical modelling of IBC,controller design with PLL for VCPFC, MATLAB simulink design of converter with PFC . Last section gives conclusions

II Interleaved Buck converter:

IBCconsists of twofold buck converters are parallely connected. it is controlled by controller provided in the closed loop. Each MOSFET operated with different phases reduced by phase shift interleaving operation. To decrease the

inductance size and reduce the effect of ripples present in input current,Vo,Io. Hence circulating current in two parallel paths. Transient considerations are taken into account during switch on period and switch off period of rectifiers.Two phase IBCconsists of two inductors are parallely connected inductance value. The storage capacity of inductance is now doubled. It provides the equal output power as compared with the basic converter. Controller Pulses are applied to each switch with 180˚phase shift.

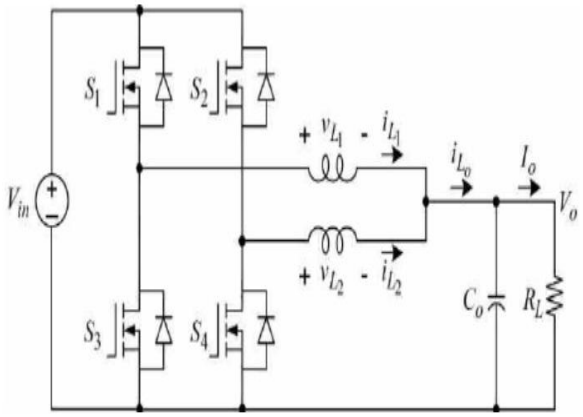


Fig.2Basic Interleaved buck converter

III.DESIGN SPECIFICATIONS OF TWO PHASE IBC

Table 1 shows the design specifications of buck converter with settling time values.

Table1: Design Specifications

V_{in}=24V	L=1mH
V_{out}=12V	C=1000F
P_o=72W	I_o=0.06A
D=0.5	R=200Ω
Irms=0.6A	V_{rms}=16.8V
P.F=0.9	T_s=0.4s

IV MODELLING OF IBC

To obtain the stability of converter both output side and input side harmonics of current should be minimized. Considering the actual voltage, input voltage and duty ratio the equation becomes

A. Design of converter

$$\frac{V_a}{V_i} = \frac{D}{D+\Delta} \qquad (1)$$

$$\Delta = D\left(\frac{V_i}{V_a} - 1\right) \qquad (2)$$

$$\overline{I_0} = \frac{V_i T_i}{2L} D\Delta \qquad (3)$$

Now substitute equation (2) in (3)

$$\overline{I_0} = \frac{V_i T_i}{2L} D\left(D\frac{V_i}{V_0} - 1\right) \qquad (4)$$

Taking small signal values for D to d and I_0 to i_0

$$\overline{I_0} = \frac{V_i T_i}{2L} D^2\left(\frac{V_i}{V_a^2} - 1\right) \qquad (5)$$

$$\widehat{i_0} = \frac{\partial \overline{I_a}}{\partial D}\hat{d} + \frac{\partial \overline{I_a}}{\partial V_a}\widehat{v_a} \qquad (6)$$

$$\cong \frac{V_i T_i}{2L}\ 2D\left(\frac{V_i}{V_0} - 1\right)\hat{d} + \frac{V_s T_S}{2L} D^2\left(-\frac{V_i}{V_a^2}\right)\widehat{V_a}$$

$$\widehat{i_0} \cong \frac{2I_0}{D}\hat{d} - \frac{D+\Delta}{R}\widehat{v_0} \qquad (7)$$

B.Inductor selection

When the chopping frequency is increased heat is produced in the inductor which is due to saturation, residual flux and hysteresis is imbalanced. Hence the proposed interleaving buck converter producesharmonics controller output. This can be overcome by properly selecting the coil with increased air gap.

The inductance value L_I derived as follows

$$V_{LI} = L_I \frac{di}{dt} = L_I\left(\frac{\Delta I_{LI}}{(1-D)T}\right) \qquad (8)$$

$$L_I = \frac{V_{OUT}\,(1-D)}{f_{SW} \cdot \Delta I_{LI}} \qquad (9)$$

Where $f_{sw}$is the switching frequency of the converter. Assuming 30% of ripple value allowed

$$I_{PK} = I_{OUT} + \frac{\Delta I_L}{2} \qquad (10)$$

Where Δ is the 30% of allowed ripple value.

I_{pk}=100A

Inductor must sustain the peak current up to 100A.

B. Capacitor selection

The output capacitor filters inductor current ripples and delivers the stable output voltage

$$\Delta I_{Cout} = \left(\frac{V_{out}}{n.f_{SW}}\right)\left(1 - \frac{D}{L}\right) \quad (11)$$

$$C_{out} = \frac{(1-D)V_{out}}{\Delta V_{Cout}.\ 8L\ .n.f_{sw}} \quad (12)$$

V DIGITAL CONTROLLER DESIGN WITH PLL

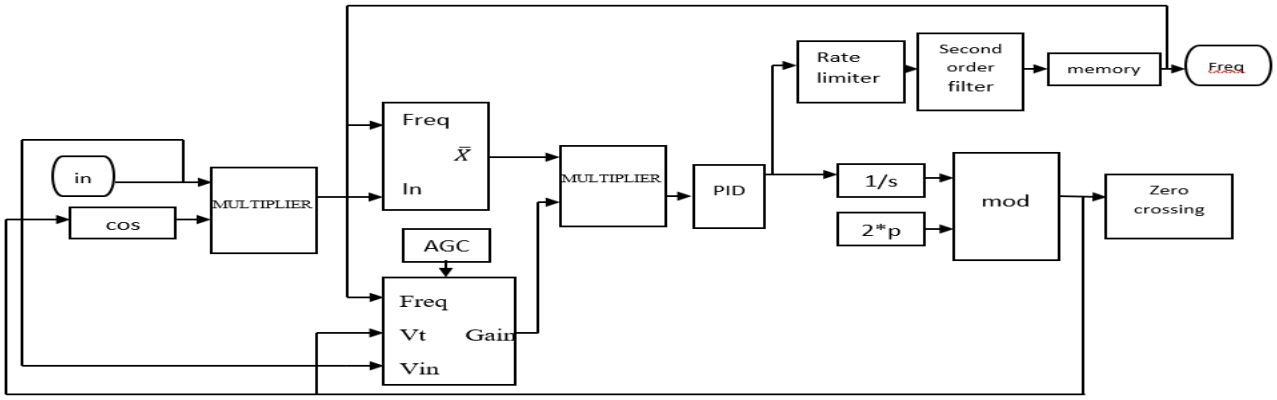


Fig.3 PLL block for PFC controller

The digital control is used for generation of pulses by controlling both output voltage and input voltage. Feedback control is applied to get regulated output voltage. The sampled voltage error is supplied to the Digital compensator. The output of this digital compensator is multiplied with sine template and then compared with sensed inductor current signals. The current error is treated in the digital compensator part and the resulting valuesare compared with the carrier signal in the digital PWM block which gives pulses to the switches.

A.Design of PLL

Phase Locked Loop (PLL) system is used to match a fixed frequency sinusoidal signal. When the Automatic Gain Control is allowed, the input (phase error) of the PLL regulator is mounted according to the input magnitude.

For better performance, set controller

controller gains [Kp Ki Kd] = [180 3200 1] and check the Automatic Gain Control parameter to enable.

Input : Normalized input signal (pu)

Output 1: practical frequency (Hz) = w/(2pi)

Output 2: sawtooth w.t varying between 0 to 2*pi, matched on the zerocrossing (rising) of the basic of input signal.

i)Automatic gain control:

Compute the fundamental value of input 3 through a running window of one full cycle of fundamental frequency given by first input. The reference value is required for the calculation is given to the second input. The two outputs return respectively the magnitude and phase fundamental values are same.The basic cycle of simulation, the output value is held constant as mentioned by the input parameters. To calculate total value of second input over a running gap of one full cycle of frequency signal given by first input.

For the first rotation of basic frequency,output maintained to the value stated in the starting input (DC component) parameter.The Minimum frequency parameter is used to limit the buffer part of the Variable Time Delay block used under the mask of the block.

ii)Multiplier block design

$$I_{muo} = \frac{k_m\ I_{ac}\ (V_{comp}\ -1)}{V_{ff}^2} \quad (13)$$

Where,

Imuo-Multiplier output current

Iac-Multiplier input current

Vff-Feed forward voltage

Vcomp- Comparator output voltage

Vff=1.4

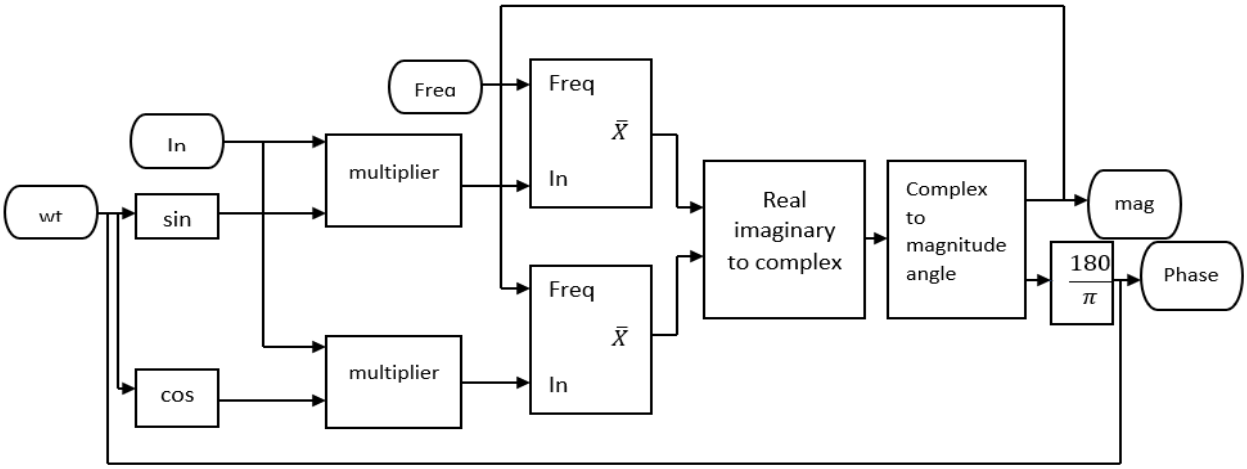


Fig.4 Automatic gain control in PLL

$$V_{o(PK)}=\frac{P_{in}}{2\pi fr\, C_O V_O} \quad (14)$$

Where, $f_r=1.84V_{ac}$

The digital regulator is designed in the two steps discussed here.

Step1:Mathematical design of controller the line voltage and the input voltage

$$v_s = Vs\, sin\theta \quad (15)$$

$$v_1 = Vs\,|sin\theta| \quad (16)$$

$$\theta = 2\pi fLtL \quad (17)$$

θ is the line phase angle

voltage transfer ratio of PFC is required to vary the angle θ in half period.

The voltage transfer value

$$T_{vv}(\theta) = \frac{Vo(\theta)}{Vs(\theta)|sin(\theta)|} \quad (18)$$

Where $f_s >> f_L$

Where *Vo* is the local average direct current output voltage from power factor converter, WhereT_{VV} is line period the buck topology can not provide high voltage transfer ratio.

To achieve higher power factor

$$i_1 = Is|sin\theta| \quad (19)$$

$$P_i = v_1 i_1 = V_S I_S \sin^2\theta \quad (20)$$

And output powerbecomes

$$P_o = \overline{v_o} i_0 \quad (21)$$

Assume Pi=Po, the output current *io* gives,

$$i_o = \frac{Vs\ Is\ \sin^2\theta}{\overline{v_o}} \quad (22)$$

For one full period two half cycles are the outputs,

$$i_o = 2I_O \sin^2\theta = I_O(1 - cos2\theta) \quad (23)$$

For better Power factor correction output current is required for a unity power factor as a function of the angle θ.

Two requirements for PFC

a)T_{vv}must be varied for one full cycle or half value period.

b)The output current also varied simultaneously over the half value period .

$$u(t) = K_p\left[e(t) + \frac{1}{Tiv}\int_{v0}^{t} e(t)dt + Td\frac{de(t)}{dt}\right] \quad (24)$$

The *Td*,*Ti*and*Kp*constant values are obtained by based on errors tuninig respectively.PID controller's Laplace transform is given by

The parameters are tuned properly for digital controller and adapt the buck converter to achieve the best behaviour of system. The Kp,Ti and T values are found by using Nichols tuninig and ruth array technique.

$$U(s) = K_p \left(1 + \frac{1}{Tiv} + Tds\right) V(s) \qquad (25)$$

PLL controller modelling and IBC modelling established in this work.The digital controller is used to regulate the output voltage in fixed value. The PLL will lock the input frequency ,Hence input voltage and current values inphase. The obtained value applied to multiplier block. Closed loop transfer functions are derived for discontinuous conduction mode. UPF and low THD nearly achieved.

VI MATLAB SIMULINK MODEL FOR IBC

Interleaved buck converter without VCPFC

MATLABSimulink is used for implementing the interleaved synchronous buck converter circuit. The fig.5 shows the interleaved step down converter without power factor correction. Without power factor correction circuit the power factor values is 0.5 and Total harmonic values also very highvalue reaches approximately unity and low THD obtained. This low THD limit is with in the IEEE Interleaved buck converter PLL with VCPFC

MATLABSimulink is used to implement the IBC circuit with PLL based VCPFC controller. PF 519 bounds.The Vo is controlled to a fixed value by the controller and input voltage and current in phase.

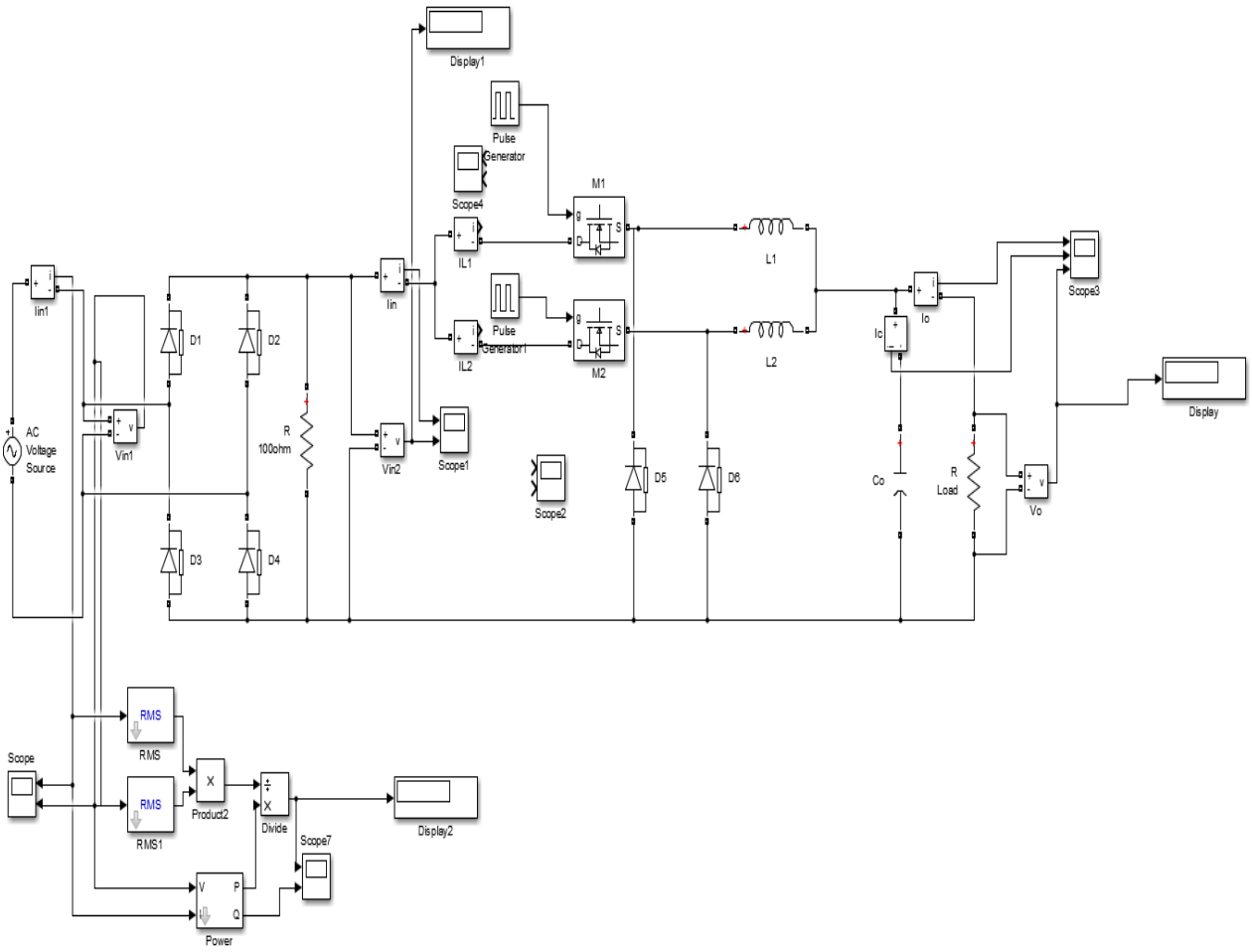


Fig.5 Interleaved buck converter without pfc

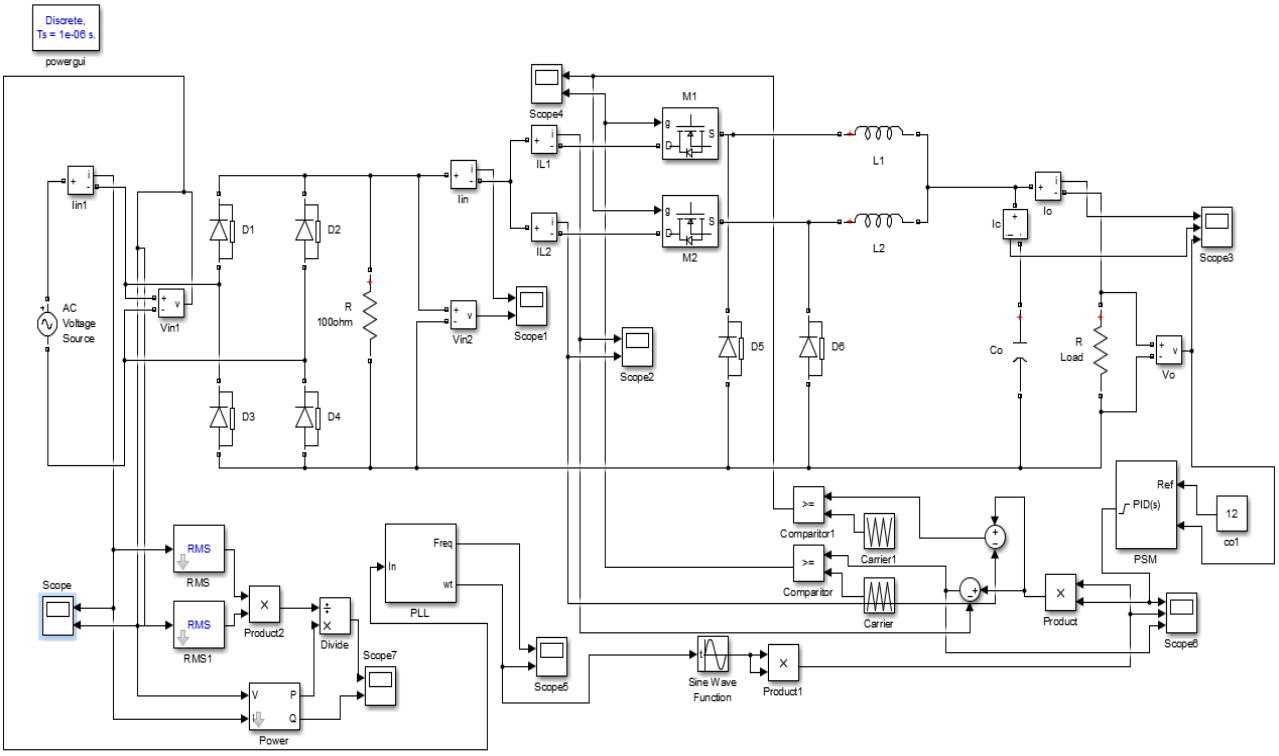


Fig.6 Interleaved synchronous buck converter with PLL controlled VCPF

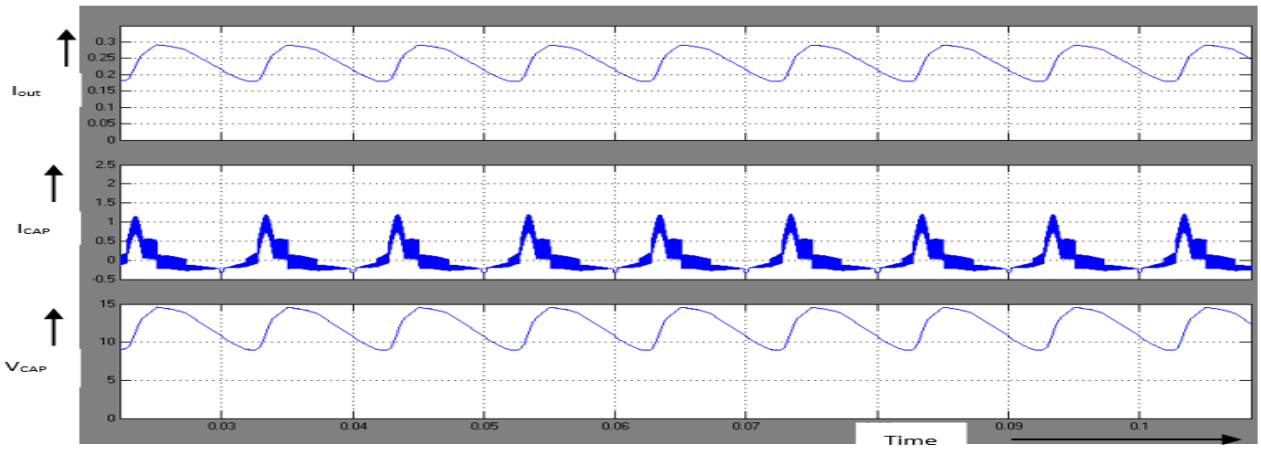
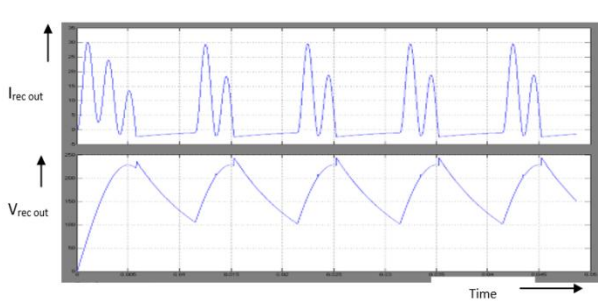


Fig. 7 a)Converter output current ,capacitor current and output voltage



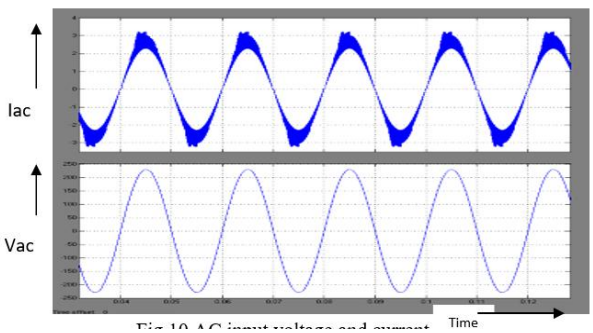
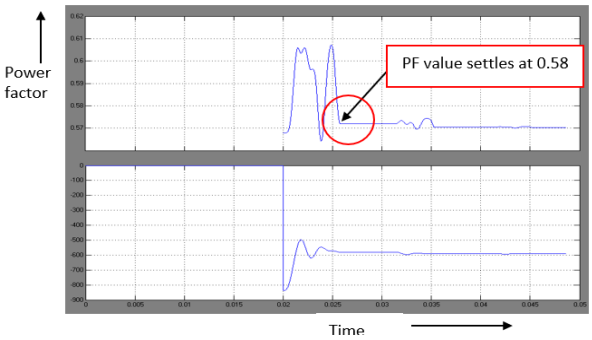


Fig. 7b)Interleaved synchronous buck converter with VCPFC output c)Rectified output



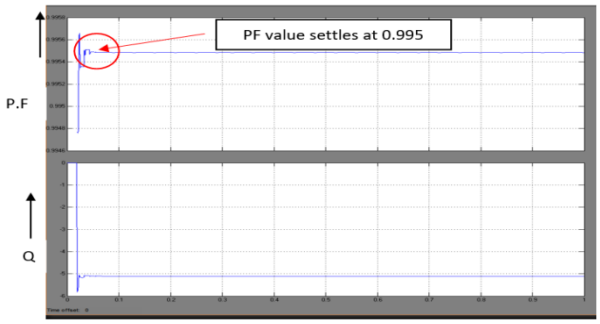


Fig 8a)Interleaved synchronous buck converter without pfc controller b)Interleaved synchronous buck converter with pfc output

Table:I PLL based interleaved buck for the Resistive load with Vin=230V

Load value(Ω)	50	100	150	200	250	300
Vout(V)	12.6	12.5	12.3	12.2	12.1	12.05
Io(A)	0.25	0.125	0.08	0.07	0.05	0.04
Power factor	0.995	0.997	0.9981	0.998	0.9983	0.9985

Table:II PLL based interleaved buck for the inductive resistive loadwith Vin=230V,L=150x10^{-3}H

Load value(Ω)	50	100	150	200	250	300
Vout(V)	12.6	12.5	12.4	12.3	12.1	12.1
Io(A)	0.25	0.12	0.07	0.06	0.05	0.04
Power factor	0.995	0.997	0.998	0.998	0.998	0.9984

Table:III Performance comparison with other papers

Parameters	This work	[25]	This work	[1]	This work	[4]
V_{in}(V)	260	260	230	230	120	120
V_o(V)	80	80	80	80	56	56
L(H)	150 µ	150 µ	400	400	975	975
C(F)	1000 µ	990 µ	1000	1.5	110	110
LOAD in watts	2m, 200Ω	100	2m, 200Ω	90	1000	1000
Controller	Interleaving approach with PLL with VCPFC	Improved constant on time controller	Interleaving approach with PLL with VCPFC	CCB PFC Controller	Interleaving approach with PLL with VCPFC	Nonlinear ripple feedback controller
Power factor	0.96	0.93	0.935	0.92	0.94	-

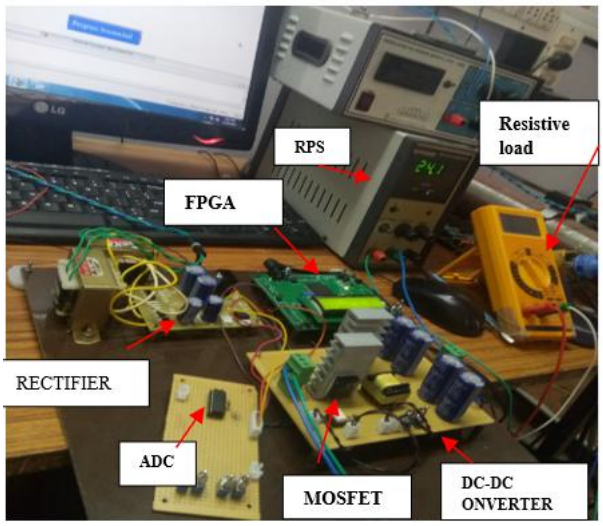


Fig. 9 Hardware set up of closed loop PLLbased VCPFC controller for buck converter with Resistive load

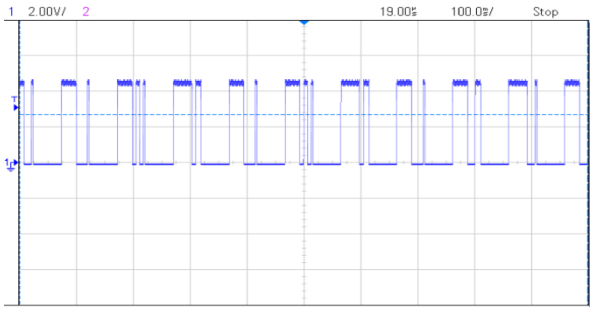


Fig. 10 VCPFC controller output

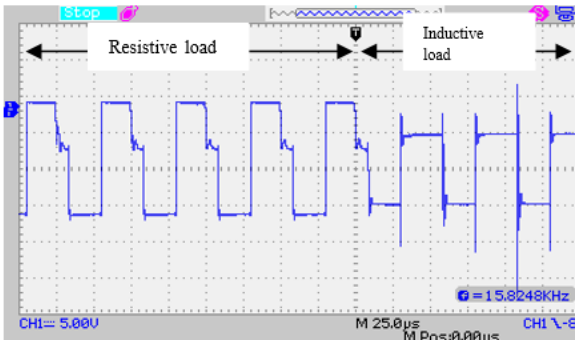


Fig.11 VCPFC controllert output for resitive and inductive load

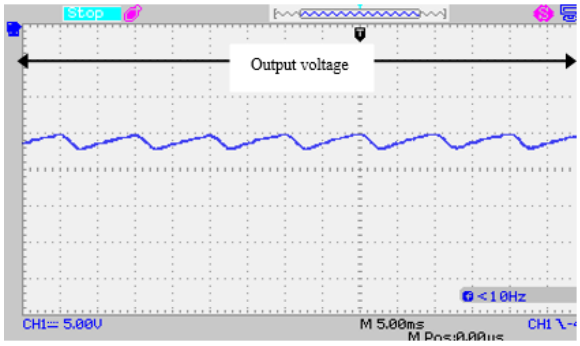


Fig.12 closed loop output voltage PLL controlled VCPFC

CONCLUSION

Voltage controlled PFC buck converter designed and analyzed.This analysis focused to improve power factor at input side. The conventional design without PLL canot achieve the power factor above 0.95.The complete design PLL based VCPFC achieves 0.998 P.F .This design procedure implemented in matlab simulink for both with PFC and without PFC .Simulink results cbtained for both induvtive and resistive loads with input voltage 240V,2mA.This PLL based VCPFC buck converter maintain the voltageapproximately 12V and P.F 0.998 across the load range 25% to 80%.

REFERENCE

1. Laszlo Huber,Liu Gang, and Milan M. Jovanovic, “Design-Oriented Analysis and Performance Evaluation of Buck PFC Front End”IEEETransactions on power electronics, vol. 25, no. 1, January 2010.
2. Jing-Teng Lin and Kai-yuHu,Chien-Hung Tsai, “Digital Multiphase Buck Converter withCurrent Balance/Phase Shedding Control”IEEE Transactions on power electronics, 2015.
3. David J. Perreault, and John G. Kassakian,“Distributed Interleaving ofParalleled Power Converters”IEEETransactionson circuits and systems—I: Fundamentaltheory and applications, vol. 44, NO. 8, August 1997.
4. Yen-Wu Lo and Roger J. King, “High Performance Ripple Feedback forthe Buck Unity-Power-Factor Rectifier”IEEE Transactions on power electronics, vol. 10, no. 2, March 1995.
5. G.RevanSidda, Mohammed Mustafa, Mohammed Saleem,Power Factor Correction Techniquein Photovoltaic Grid Connected Inverter by usingBoost Converter”International Journal of Engineering Trends and Technology (IJETT) – Volume 13, Number 1, Jul 2014.
6. L.Rossetto,G.Spiazzi,P.Tenti, “Control techniques for power factor correctionconverters”
7. Leopoldo Rossetto, Giorgio Spiazzi, PaoloTenti, Bruno Fabiano, and Carmelo Licitra, “Fast-Response High-Quality Rectifier with Sliding Mode Control” IEEE transactions on power electronics, vol. 9, no. 2, march 1994
8. Antonio Leon-Masich,Hugo Valderrama-Blavi, “A High-Voltage SiC-Based Boost

PFCfor LED Applications" IEEE transactions on power electronics, vol. 31, no. 2, February 2016.
9. A. Cid-Pastor n, L.Martinez-Salamero,A.ElAroudi,"Synthesisofloss-freeresistorsbasedonsliding-modecontroland itsapplicationsinpowerprocessing" Control EngineeringPractice21(2013)689–699.
10. Freddy Flores-Bahamonde, Hugo Valderrama-Blavi,"Control of a three-phase AC/DC VIENNA converterbased on the sliding mode loss-free resistor approach"IET Power Electron., 2014, Vol. 7, Iss. 5, pp. 1073–1082.
11. Adria Marcos-Pastor, Enric Vidal-Idiarte, "Loss-Free Resistor-Based Power Factor CorrectionUsing a Semi-Bridgeless Boost Rectifierin Sliding-Mode Control"IEEE transactions on power electronics, vol. 30, no. 10, October 2015.
12. Reham Haroun, Abdelali El Aroudi, "Impedance Matching in Photovoltaic SystemsUsing Cascaded Boost Converters andSliding-Mode Control"IEEE transactions on power electronics, vol. 30, no. 6, June 2015.
13. PHILIP C. TODD, "UC3854 Controlled Power Factor Correction Circuit Design"
14. Dragan MaksimoviC,Yungtaek Jang, "Nonlinear-Carrier Control forHigh-Power-Factor Boost Rectifiers"IEEE transactions on power electronics, vol. 1 i , no. 4, July 1996.
15. Keyue M. Smedley,Slobodan Cuk, "One-Cycle Control of Switching Converters"IEEE transactions on power electronics, vol. 10, no. 6, November 1995.
16. Haiping Xu, Xuhui Wen, ErminQiao, "High Power Interleaved Boost Converter in Fuel Cell Hybrid Electric Vehicle"0-7803-8987-5/05,2005 IEEE.
17. Brad Bryant,Marian K., "Modelling the Closed-Current Loop of PWM BoostDC–DC Converters Operating in CCM With PeakCurrent-Mode Control"IEEE transactions on circuits and systems—i: regular papers, vol. 52, no. 11, November 2005.
18. Wei Ma, Mingyu Wang, "Stabilizing the Average-Current-Mode-ControlledBoost PFC Converter viaWashout-Filter-Aided Method"IEEE transactions on circuits and systems—ii: express briefs, vol. 58, no. 9, September 2011.
19. SaubhikMaulik, Prof. Pradip Kumar Saha,"Power Factor Correction By Interleaved Boost Converter Using PI Controller"Int. Journal of Engineering Research and Applications,Vol. 3, Issue 5, Sep-Oct 2013, pp.918-922.
20. Simone Buso, Paolo,"MattavelliSimple Digital Control Improving DynamicPerformance of Power Factor Preregulators"IEEE transactions on power electronics, vol. 13, no. 5, September 1998.