Dual Boost High Performances control strategy on a Power Factor Correction (PFC) implementation by using a 24 bit custom floating point library.

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Abstract – *This work explores the feasibility of implementing IEEE 754 standard compliant, 24 bit floating point unit on reconfigurable computing systems.*
The floating point unit generation approach outlined in this paper allows the creation of a vast collection of floating point routines. The developed library has been tested by means a proposed Power Factor Correction (PFC) dual boost scheme.
It is based on an optimized power sharing where the active filtering approach is used to increase the current quality and at the same time to reduce the switching losses.
Both the simulation and experimental results show that the proposed strategy for PFC achieves near unity power factor and a not negligible switching losses reduction. Furthermore these results show the today's FPGA devices are well suited for this operation also by using a low cost device.

Key words: *FPGA, floating point numbers, PFC.*

1. Introduction

Over the last years, with the growing enhancements in functionality that have occurred in FPGA devices, reconfigurable computing has proven itself to be a viable alternative to microprocessor-based implementation for a variety of compute-intense algorithms [1].
Floating point arithmetic is essentially equivalent to arithmetic in scientific notation to a particular base or radix [2].
This standard defines [3] [4] four formats for floating-point numbers, two of which are commonly used, single and double precision numbers.
A generic number can be represented in the form:

$$N = (-1)^s 2^e f \qquad (1)$$

$$\text{with: } f = \sum_{k=0}^{n-1} a(k)2^{-k} \;;\; M = 1.f \qquad (2)$$

$$\text{with: } EXP = e + BIAS$$

In general the exponent is biased by $(2^{N-1})-1$, where N is the number of bits used for the exponent field.
In this paper has been considered the implementation of a short floating point 24 bit math library. In this case [5] [6] a generic number is stored in a 24 bit width word.
A reduced floating point representation is particularly useful when the FPGA [7] device is not sufficiently capable to implement the single or double precision standard.
In the following is briefly reported the analytical formulation used for the implementation of the four basic arithmetic operations between two or more given numbers.
Using a 24 bit floating point (*sfloat24*) arithmetic the loss of precision respect to the use of standard single precision number is not particularly significant in ordinary numerical computational tasks. The significant limitation is due only by the reduced range representation as well known in the literature.
Obviously this approach is not new in the nowadays available calculus units, for example DSP and/or microcontrollers system may use a 24 bit floating point arithmetic. In the field of FPGA this approach becomes important in order to exploit their well known features.
In particular is described the implementation of the comparison operators between two o more numbers.
The comparison operators are useful to implement a current hysteresis technique widely used in the proposed control scheme.
Furthermore in modern power converters for electrical drives the switching losses minimization is one of the main objectives of the design process. The importance of this problem arises when either high power or high performances are required.
The switching losses, in fact, increase both when the DC bus voltage or the collector current increase (high power application) and when high switching frequencies are required (high performances). Since the simple reduction of the switching frequency decreases the converter output quality (i.e. a quality decreases of both the output voltages and currents) a reduction of the switching losses can be achieved by reducing the voltage (multilevel or hybrid multilevel converters) [8],[9] or by reducing the switch current (parallel connection) [10]. Another important aspect is that to comply to the recent international standards, such as IEC-1000-3-2 and IEEE-519.
The interleaving configuration of the converters reduces the line current harmonics and increases the efficiency.

The active filtering approaches, widely depicted in this paper can be considered as an evolution of the interleaving techniques applied when two or more converters are connected in parallel.

2. Basic Arithmetic Operators formulation

Given the following numbers:

- $N_A = (-1)^{S_A} 2^{eA} \cdot 1.f_A$ where the value of eA in the exponent bit field is just represented with $EXP_A = eA + BIAS$ and the mantissa as $M_A = 1.f_A$
- $N_B = (-1)^{S_B} 2^{eB} \cdot 1.f_B$ where the value of eB in the exponent bit field is just represented with $EXP_B = eB + BIAS$ and the mantissa as $M_B = 1.f_B$

It is possible to define on the basis of the following expressions the four basic arithmetic operators.
The sum and/or difference between two numbers can be expressed as:

$$R = N_A \pm N_B \tag{3}$$

$$R = (-1)^{S_A} 2^{eA} \cdot 1.f_A \pm (-1)^{S_B} 2^{eB} \cdot 1.f_B \tag{4}$$

The product can be expressed as [11]:

$$R = N_A \cdot N_B \tag{5}$$

$$R = S_R \cdot 2^{eA+eB} \cdot 1.f_A \cdot 1.f_B \tag{6}$$

where:

$$S_R = S_A \; XOR \; S_B \tag{7}$$

$$EXP_R = eA + eB + BIAS \tag{8}$$

$$M_R = 1.f_A \cdot 1.f_B \tag{9}$$

and R is the result returned by the sum and or difference operators.
Given a number in the usual, already showed form the reciprocal is equal to [12]:

$$R = \frac{1}{(-1)^S 2^e 1.f} \tag{10}$$

If the fractional part of the mantissa f is null the result is immediately given by:

$$R = (-1)^S \cdot 2^{-e} \tag{11}$$

with $EXP_R = -e + BIAS$.
Nevertheless the division between numbers can be defined as the product of the first number and the reciprocal of the second number.

3. Comparison Operators

In this section will be discuss the comparison between two given numbers N_A and N_B. The sign of each number is given by the MSB. The absolute value of a number is the union of the exponent and the fractional part of mantissa fields respectively.
A XOR operation between the sign bit of both the numbers is executed in order to evaluate if the numbers have the same signs ($XOR = 0$) or different ones ($XOR = 1$).
If the sign bit of N_A is equal to '1', S_A=1, and (S_A *XOR* S_B)=1, therefore S_B=0, then results $N_A<N_B$ or $N_A \leq N_B$.
If the sign bit of N_A is equal to '0', S_A=0, and (S_A *XOR* S_B)=1, therefore S_B=0, then results $N_A>N_B$ or $N_A \geq N_B$.
If the numbers have the same sign the comparison is executed by evaluating the absolute value of both the numbers. If the MSB of both the numbers are zero the comparison operation gives the following results:

Comparison between absolute values	N_A *greater than* N_B	N_A *less than* N_B
$\|N_A\|>\|N_B\|$ or $\|N_A\|\geq\|N_B\|$	1	0
$\|N_A\|<\|N_B\|$ or $\|N_A\|\leq\|N_B\|$	0	1

If the MSB of both the numbers are equal to one the comparison operation gives the following results:

Comparison between absolute values	N_A *greater Than* N_B	N_A *less than* N_B
$\|N_A\|>\|N_B\|$ or $\|N_A\|\geq\|N_B\|$	0	1
$\|N_A\|<\|N_B\|$ or $\|N_A\|\leq\|N_B\|$	1	0

It is evident that the comparison between two numbers is given by the logical flags "greater than" and "less than" respectively. The comparison operator between two numbers is useful to build a hysteresis current controller widely used in the following to implement the described control strategy.

4. Dual Boost High Performances Power Factor Correction (PFC) System

This system is generally used in low power applications, such as single phase residential applications, where a bidirectional power flow is not required.
The proposed PFC is shown in fig. 1 and it is based on a dual boost circuit where the first one (switch T_{b1} and choke L_{b1}) is used as *main PFC* circuit and where the second one (switch T_{b2} and choke L_{b2}) is used to perform an active filtering. The purpose of the active filtering performed by the second boost circuit is to increase the quality of the line current and at the same time to reduce the PFC total switching losses.

A. Proposed PFC modelling and controlling

With reference to fig.1, by considering the PFC working in continuous conduction mode, the following voltage equations are worked out [13]:

$$\begin{cases} v_b = L_{b1}\dfrac{d}{dt}i_{b1} + R_1 i_{b1} + f_{b1}v_d \\ v_b = L_{b2}\dfrac{d}{dt}i_{p2} + R_2 i_{b2} + f_{b2}v_d \\ i_{PFC} = i_{b1} + i_{b2} \end{cases} \quad (12)$$

where:

$$v_b(t) = \left|V_b \sin(\omega t)\right|$$

$$f_{b1} = \begin{cases} 0 & if \quad T_{b1} = 1 \quad (switch\ on) \\ 1 & if \quad T_{b1} = 0 \quad (switch\ off) \end{cases} \quad (13)$$

$$f_{b2} = \begin{cases} 0 & if \quad T_{b2} = 1 \quad (switch\ on) \\ 1 & if \quad T_{b2} = 0 \quad (switch\ off) \end{cases} \quad (14)$$

the source main voltage and PFC commutation functions respectively represent. In particular, the (12) can be written as follows:

$$\begin{aligned} f_{b1} = 0 \quad &\rightarrow \quad \frac{d}{dt}i_{b1}(t) = \frac{v_b(t)}{L_{b1}} \\ f_{b1} = 1 \quad &\rightarrow \quad \frac{d}{dt}i_{b1}(t) = \frac{v_b(t) - v_d(t)}{L_{b1}} \end{aligned} \quad (15)$$

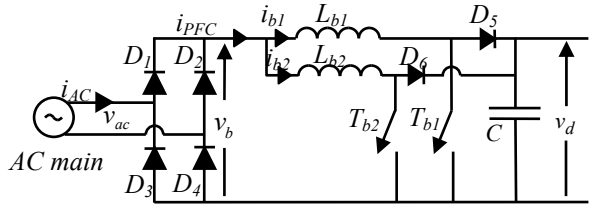

Fig.1. Proposed dual boost PFC circuit.

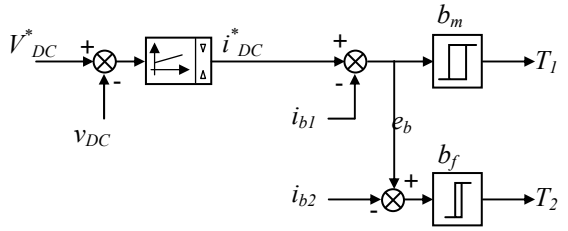

Fig. 2. Control scheme of the proposed dual boost converter.

$$\begin{aligned} f_{b2} = 0 \quad &\rightarrow \quad \frac{d}{dt}i_{b2}(t) = \frac{v_b(t)}{L_{b2}} \\ f_{b2} = 1 \quad &\rightarrow \quad \frac{d}{dt}i_{b2}(t) = \frac{v_b(t) - v_d(t)}{L_{b2}} \end{aligned} \quad (16)$$

where:

$$i_{b1} \geq 0 \quad i_{b2} \geq 0 \quad (17)$$

because of the unidirectional AC/DC diode rectifier of fig.1. Therefore, the control of the PFC currents i_{b1} and i_{b2} can be achieved only if the following condition occurs:

$$v_d(t) > v_b(t) \quad (18)$$

In particular if the (18) is satisfied it is possible to control the derivative of the total PFC current i_{PFC}

$$\frac{d}{dt}i_{PFC} = \frac{d}{dt}i_{b1} + \frac{d}{dt}i_{b2} \quad (19)$$

As described above, by using (15) and (16) the control of the PFC currents i_{b1} and i_{b2} can be achieved and, in particular, it is possible to track the desired value of both the PFC reference currents evaluated by using the control scheme of fig.2. In this control scheme the magnitude of the desired PFC current is determined by using a PI regulator [14] which input is the difference between the reference and actual output voltage. In order to obtain an unity power factor, the argument of the total PFC current is determined by using the argument of the line voltage. Once the desired total PFC current is achieved, two current controls has to be performed for both the PFC circuits. The *main PFC* is modulated with an hysteresis control by imposing the total PFC current. A large hysteresis band b_m allows to achieve low switching frequency. The *filtering PFC* reference current is, instead, the difference between and the actual value of i_{b1}. An hysteresis control is also performed, but using a small hysteresis band b_f. By using this approach the *main PFC* is used to transfer the desired power to the load while the *filtering PFC* is controlled in order to increase the total PFC current quality.

B. Dual Boost PFC Efficiency

The main goal of the proposed dual boost PFC and of the above described control algorithm is to introduce improvements in terms of power losses reduction thanks to an Active Filtering (AF) approach.

The use of the active filtering for the switching losses reduction is based on simple analysis of the linearized switching characteristic of a power device. The total switching losses can be expressed by [15]:

$$P_t = fV_{dc}I_{load}d \quad (20)$$

where f the switching frequency, I_{load} the device collector current, V_{dc} the DC bus voltage and d the turn-on and turn-off time coefficient respectively represent. By using the (20) it is easy to show that if the required load power is splitted on two different

switches, operating with different switching frequency and with different currents, the total efficiency is greatly improved with respect to the case in which a single device is used. In particular in the proposed approach the *main PFC* (switch T_{b1}) works with high current and low switching frequency while the *filtering PFC* (switch T_{b2}) works with low current and high switching frequency.

5. Dual Boost PFC Simulation

In order to perform a digital implementation of the control scheme shown in fig.2, an FPGA based architecture has been chosen. The proposed control scheme has been deeply tested in simulation for a preliminary validation. In particular, a complete simulation of both the power electronics system and of the control code has been performed by using the Matlab® Simulink® and the Altera DSP Builder®.
It has to underline that the use of the Altera® DSP Builder® allows to preliminary simulate the algorithm and then to program directly the FPGA starting from the Simulink® code. Obviously this approach is effective only if all the control components, included the digital and analog I/O, are properly simulated. Therefore the first simulation step is the reproduction of all the analog signals and their quantization process.
In fig. 3 the Simulink® signals conditioning and A/D conversion code are shown.

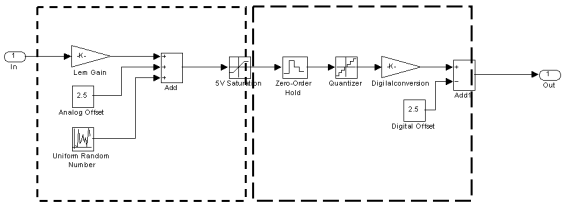

Fig. 3. Simulink® signal conditioning and A/D conversion.

The former is composed by a gain block, which takes into account the current transducer constant (*Lem Gain*), and an offset equal to 2.5V used to allow an A/D conversion of both positive and negative quantities. A random number generator is also included to simulate the noise related to the signal conditioning circuit.
The A/D conversion simulation code starts with a 5V saturation and a zero-order hold block is used to simulate the A/D converter Sample and Hold. According to the used 10 bit A/D converter datasheet, a conversion time of 2.5 μs has been chosen. A quantizer block simulates the A/D quantization error, Q_e, evaluated by using the following well-known relation:

$$Q_e = \frac{V_{ref}}{2^{conversion\_bits}} = \frac{5}{1024} = 0.0049 \qquad (21)$$

where V_{ref} is the A/D reference voltage.
Therefore, the digital conversion gain and the following offset transform the quantized signal into a *sfloat 24* bit data bit format. The basic casting operators are based on the conversion of an integer number to the corresponding 24 bit floating point number and vice versa.

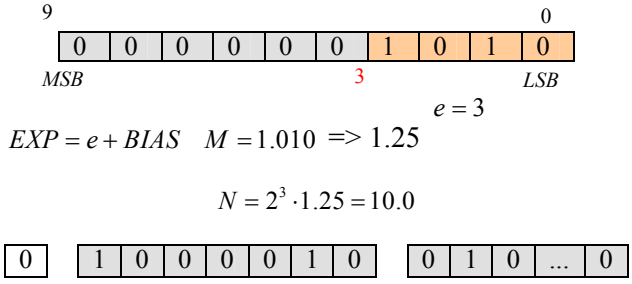

Fig. 4. Example of a 10 bit unsigned integer number conversion in the corresponding 24 bit floating point number.

Once the A/D conversion block has been tested, the FPGA control algorithm can be included in the Simulink® simulation. The implemented algorithm for the generic power converter switch is:

$$if \quad x_{(n)} = x_{(n-1)} \qquad \begin{cases} i_{(n)} < i^*_{(n)} + b \\ i_{(n)} > i^*_{(n)} + b \end{cases} \qquad (22)$$

$$if \quad x_{(n)} = 0 \qquad (i_{(n)} > i^*_{(n)} + b) \qquad (23)$$

$$if \quad x_{(n)} = 1 \qquad (i_{(n)} < i^*_{(n)} - b) \qquad (24)$$

where:

- x hysteresis output (i.e. switch command);
- i actual current;
- i^* reference current;
- b hysteresis band;

and where with the subscript n the generic n^{th} A/D conversion is denoted.

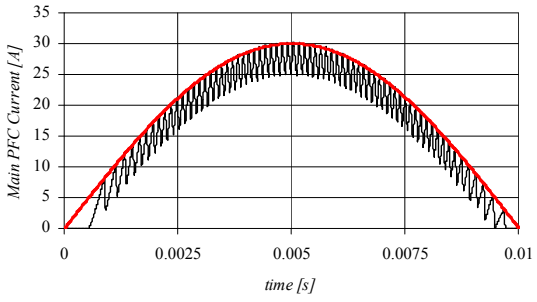

Fig.5. Simulation results: main PFC current.

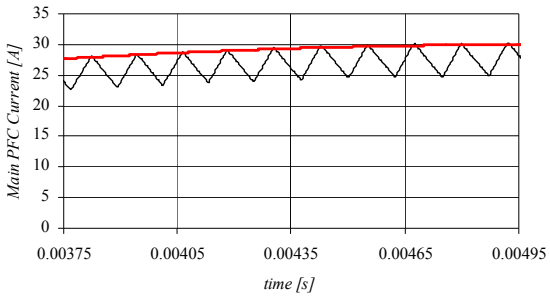

Fig. 6. Main PFC current detail.

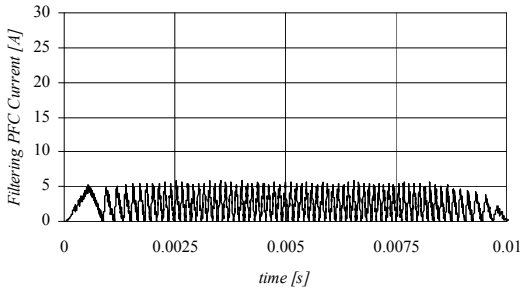

Fig.7. Simulation results: filtering PFC current detail.

Table I. System parameters.

Main PFC inductor:	3.6 *mH*
Filtering PFC inductor:	0.6 *mH*
Output filter Capacitor:	1100 µF
DC load:	200 *Ω*

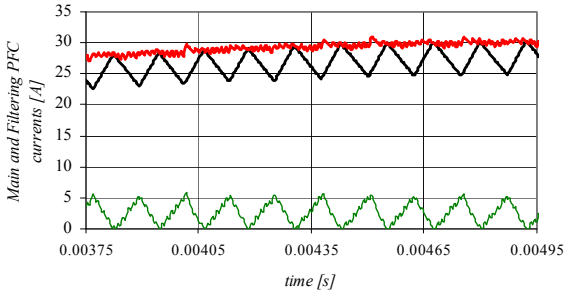

Fig.8. Detail of main and filtering PFC currents.

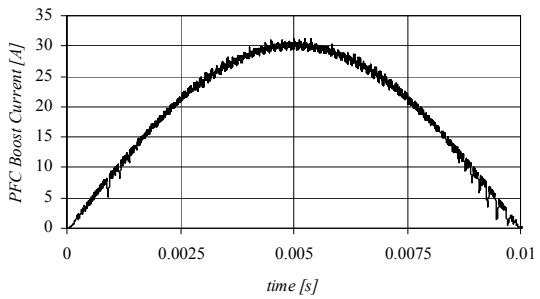

Fig.9. Simulation results: total PFC current.

By means of equations (15)-(16), in fact, is possible to control the derivative of both the *main* and *filtering* PFC currents but it is not possible to compensate negative errors of the *main* PFC current. Thus, to avoid that the quantity e_{ip1} becomes negative the lower value of the main PFC hysteresis band has been set to zero. In fig. 7 the *filtering PFC* current obtained with an hysteresis band of 1 A is reported. As it is possible to see the amplitude of this current is 5A which is the amplitude of the main PFC current hysteresis band. The effect of the filtering current come clear in fig. 8 where a detail of main and filtering current is plotted. In fig 9 the total PFC current is shown. In this last graph a not negligible reduction of the current ripple is achieved.

6. Experimental Results

In the implemented control strategy the sensed currents are the main PFC current, the filtering PFC current and optionally, only in order to validate the tests, the AC line current is sensed. To perform the experimental tests is strictly necessary to acquire the AC line voltage or the boost voltage in order to generate the *modulo sine* function needed for "building" the reference current at input of the adopted feeding algorithm. To keep the output voltage to a desired value is also necessary to acquire also the output DC voltage.
In order to sense the currents the LEM® LA25 NP Hall effect current transducers have been used and to sense the voltages the LEM® LV25 P Hall effect voltage transducers have been used.
The used Hall effect transducers used in the experimental layout, have the following main characteristics:

- the current transducers have a range of the output voltage is 0 to 7.5V for the sensed input current range 0 to 25A [K_{LEMI}=3.3226].
- in the case of voltage transducers the output voltage range is 0 to 4V for the applied input voltage range 0 to 500V [K_{LEMV}=125].

The reference current can be generated by scaling the absolute value of the AC line voltage multiplying by a factor in order to obtain the desired current reference. Another way to do this is to build a hardware zero voltage detect circuit based on a discrete IC National Semiconductor® LM139/LM339, or equivalent. This circuit generates a positive voltage when the sensed voltage is positive and a null voltage, depending by the adopted circuital configuration. In this case the *modulo sine* reference math function is generated by using the well know *CORDIC* theory, this approach is very efficient respect to look up table approach, a sine or cosine function is generated with a few and flexible code instructions [16].
In the following table is reported the total logic elements used by the control strategy in both the

above mentioned techniques of reference current direct generation.

Table II. Dual Boost Active Filter with direct Current reference [FPGA device occupation].

Typology of synchronization with the AC mains	Total logic elements
AC Voltage acquisition squared with LM 339 with generation of sine function by using the CORDIC theory.	3999/5980 [67%]
AC Voltage acquisition generation of sine function by using a scaling voltage technique.	3468/5980 [58%]

It is possible by means the custom *sfloat24* math library to implement also the full control scheme of the proposed dual boost PFC by adding the code of the PI regulator in order to achieve a desired output voltage of the whole power system. In this case the above mentioned FPGA device is not suitable to implement the full control strategy because the limited capacity in terms of logic elements. This problem could be solved by using the Altera® EP1C12Q240C6 FPGA.

Table III. Dual Boost Active Filter with PI regulator [FPGA device occupation].

Typology of synchronization with the AC mains	Total logic elements
AC Voltage acquisition squared with LM 339 with generation of sine function by using the CORDIC theory.	6342/12060 [52.6%]
AC Voltage acquisition generation of sine function by using a scaling voltage technique.	6133/12060 [50.8%]

In the table III is reported the total logic elements used by the full control strategy in the case when the reference current is generated by a PI regulator.
The performance of the proposed dual boost PFC has been experimentally investigated by using the 200 W prototype, where the control unit is the Altera® Cyclone® I FPGA while the power electronic circuits have been based on the Power Mosfet IR® SPP11N60S5 and on the IR® diode 30EPH06. Unfortunately the Cyclone® I EP1C6Q240C6/ EP1C12Q240C6 evaluation boards have not provided of an analog to digital (A/D) unit section, therefore, in order to acquire the analog signals proportional to sensed voltages and main PFC and filtering PFC currents, an analog to digital board based on 10 bit National Semiconductor® AD1061CN A/D converters has built up and connected to used FPGA device. As previously described this A/D converter, by the evaluation of the quantizer error and by its high speed, is widely suited for the proposed experimental layout, from it's datasheet this A/D converter executes a conversion in only 2 µS, the main task time execution of the control algorithm has been set to 2.5 µS. The A/D converters mounted on Altera® Cyclone I FPGA evaluation board can acquire only positive voltages until 5V, therefore additional analog circuits are needed in order to fit the voltage of built sensing system to the acceptable voltage value for the A/D circuitry of the used control unit. In order to acquire AC electrical signal the built additional analog conditioning signal system perform also a shift to positive voltages.
The *main PFC* choke and the *filtering PFC* choke are equal to 3.6 *mH* and 0.6 *mH* respectively. The FPGA used in the experimental setup implements the following functions: to execute the control algorithm, and in particular perform a quasi-analog current control; service of the A/D converter; shutdown the PFC in the case of overcurrent or overvoltage.
The handshaking of the A/D converters with the used FPGA device has been implemented by writing the following code, its obviously has been written taking in count the technical specifications as reported in the datasheet.

```
Ad_process : process(aux_adwr_net, ad_main_int_net)
  begin
   if(aux_adwr_net<='0' and ad_main_int_net<='0') then
     ad_main_rd_net<=aux_adwr_net;
     ad_main_value_net<=ad_main_input_net after 50ns;
   end if;
end process ad_process;
```

This code fragment, for example, manage a single A/D converter, for the management of a multiple A/D conversion the code is the same except to add other few variables.
In the case of the management of four A/D conversions: AC mains voltage; DC output voltage; Main PFC Current and Filtering PFC current the written VHDL code occupies only 18 logic elements of a generic used FPGA device.
The obtained experimental results are reported in figs. 10 and 11. In fig. 10 the AC line current, the *main PFC* current (i_{b1}) and the *filtering PFC* current (i_{b2}) respectively are shown. In this test the *main PFC* hysteresis band (b_m) is 0.5A while the *filtering PFC* hysteresis band (b_f) is set to 0.15A. This test validates the proposed active filtering approach; in particular it shows that the *filtering PFC* current (fig. 10c) allows to compensate the not negligible ripple of the *main PFC* current (fig. 10b). In particular the average value of both the *main* and *filtering PFC* switching frequency is 4kHz and 23kHz respectively. Fig. 11 shows the oscilloscope screenshot of the test performed with hysteresis band (b_m) of 0.25A.
Several tests has been performed with different values of both the hysteresis bands b_f and b_m in order to evaluate their effect on the system efficiency.

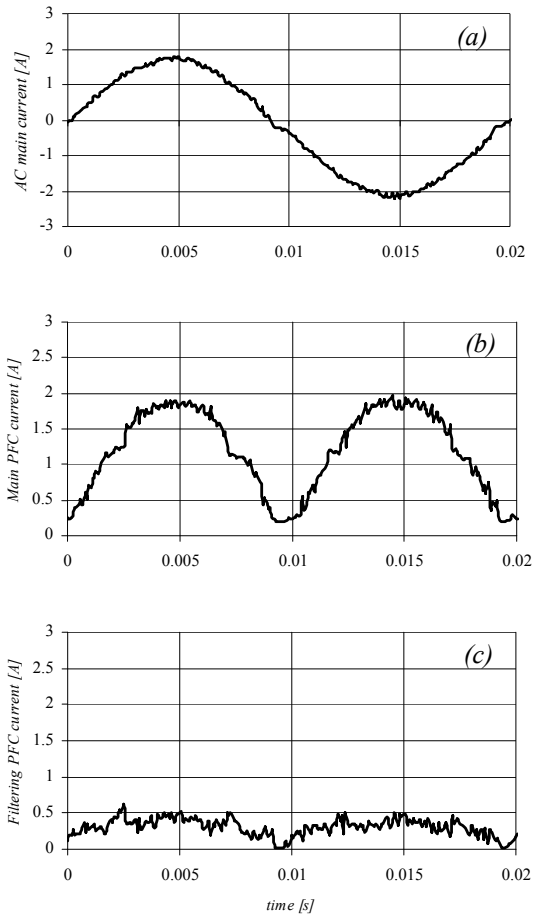

Fig. 10. AC main current (a), main PFC current (b), filtering PFC current (c) obtained with a main hysteresis band of 0.5A.

In particular the switching losses *vs.* the current ripple of the proposed dual boost PFC is compared with the one of a classical single boost PFC.
When the tested circuit working in single boost mode (the *filtering PFC* is disabled) the power switch temperature reaches 80.3°C while the temperature of the same switch, working in dual boost mode and at the same operating condition (current ripple, current amplitude and DC bus voltage) is 57.4°C.
The temperature difference is determined by the switching losses reduction achieved by using the proposed dual boost circuit. In particular a total losses reduction of 17% (*main* and *filtering* switching and conduction losses) has been evaluated by using the calibrated heat sink method. This method consists in the experimental determination of a thermal calibration curve that allows to evaluate the total device/converter losses (switching and conduction losses) simply by reading the component temperature.
To determine this thermal calibration curve, by using a low power source, several DC currents have been injected in the power device and, for each test current, after the system reached the thermal equilibrium, the device temperature, the power device terminal voltage V_c and the injected current I_c have been measured.

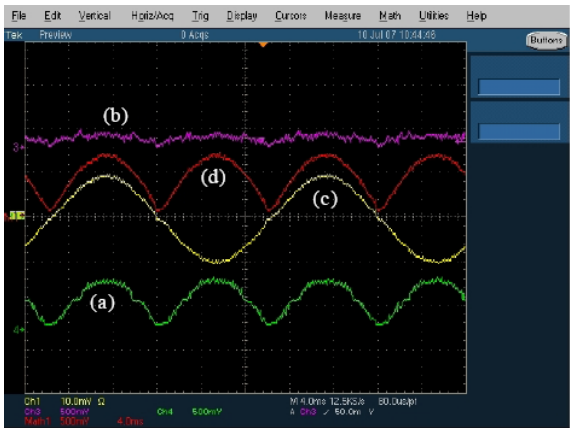

Fig. 11. Oscilloscope screenshot of main PFC current (a); filtering PFC current (b); AC line current (c); total boost PFC current (d).

At the steady state the dissipated power:

$$P_d = V_C I_C$$

is stored and plotted as function of the device temperature in order to determine the thermal calibration curve.
In the Fig. 12 the above described thermal calibration curve is shown.
Moreover, by using this method it is also possible to determine the device conduction losses as function of the device collector current, which is reported in fig. 13. It is possible to see that, by means of the proposed approach, a 45% reduction of the device losses is achieved.

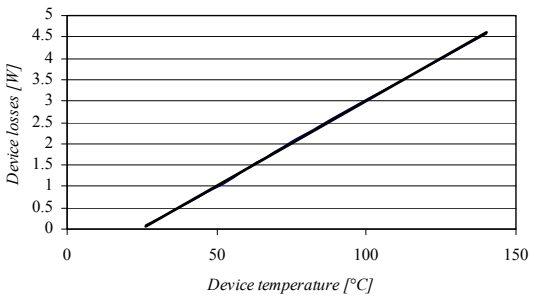

Fig. 12. Device thermal characteristic.

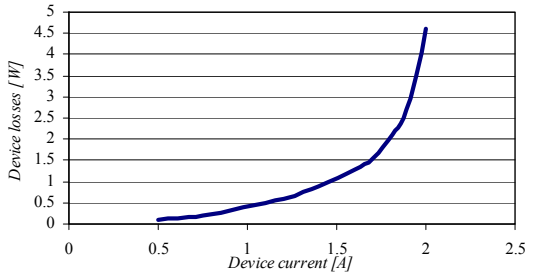

Fig. 13. Device conduction losses.

7. Conclusion

In this paper a 24 bit floating point math library has been implemented and tested. With this math library a novel dual boost PFC circuit is proposed and tested.

The simulation and experimental results confirm the validity of the proposed approach to implement real number operations on the FPGA devices.

By using the proposed power sharing control algorithm, based on active filtering approach, both a reduction of switching losses (45%) and of the total device losses (17%) is achieved. Because the speed of a classical DSP is not suitable to implement the proposed quasi-analog current control a FPGA has been used to control a 200 W prototype converter.

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