CASCADED AND HYBRID MULTILEVEL INVERTERS WITH REDUCED NUMBER OF SWITCHES FOR INDUCTION MOTOR

M. MURUGESAN
Faculty of Electrical and Electronics Engineering,
V.S.B Engineering College, Karur.

G. ASOKKUMAR
Faculty of Electrical and Electronics Engineering
Annai Mathammal Sheela Engineering College, Namakkal

.

K. RAMANI
Faculty of Electrical and Electronics Engineering,
K.S.Rangasamy College of Technology, Tiruchengode, Namakkal.

Abstract- In this paper, a modified hybrid multilevel inverter is introduced which employs bypass diode technique with H-bridge inverter topology. It aims to reduce number of controlled switches. The proposed inverter consists of a H-bridge and 3 unit cells. Each unit cell requires a serially connected voltage source and switch with a parallel diode. In a conventional multilevel inverter, presence of high number of switches increase the harmonics, switching losses, cost and total harmonics distortion. This proposed topology achieves fifteen level with only seven number of switches. It dramatically reduces complexity of control circuit, cost and low order harmonics and thus effectively reduces total harmonics distortion.

Keywords- Cascaded and Hybrid multilevel inverter, H-bridge multilevel inverter, THD, PWM, IGBT, SDCS.

1. Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and MW power level. For a medium voltage grid, it is troublesome to connect one power semiconductor switch directly [1-2]. High power and medium voltage inverter has recently become a research focus so far as known there are many problems in conventional two level inverter in the high power application. Multilevel inverters have been gained more attention for high power application, which can operate at high switching frequencies while producing lower order harmonic components [3-4].

A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for a high power application. There are several topologies available such as neutral point or diode clamped inverter, flying capacitor based multilevel inverter, cascaded H-bridge multilevel inverter and hybrid H-bridge multilevel inverter [3].

The main disadvantage still exists in diode clamped multilevel inverter topology, which restricts the use of it to the high power range of operation. In flying capacitor multilevel inverter large numbers of capacitors are needed. The first topology introduced is the series H-bridge design [5-6], in which several configurations have been obtained. This topology consists of series power conversion cells which form the cascaded H- bridge multilevel inverter and power levels will be scaled easily. An apparent disadvantage of this topology is large number of isolated voltage required to supply each cell. The proposed topology for multilevel inverter has a high number of steps associated with a low number of power switches. In addition for producing all the levels (odd and even) at the output voltage, a procedure for calculating required DC voltage source is proposed .In this topology Pulse width modulation technique is employed.

2. Cascaded Multilevel Inverter

The general structure of cascaded multilevel inverter for single phase consists of three voltage sources as shown in fig. 1. Each voltage source V_{s1}, V_{s2} and V_{s3} is connected in cascade with other sources via a special H-bridge circuit. Each H-bridge consists of four active switching elements in order to make the output voltage source in positive or negative polarity or simply zero volts depending on the switching condition of the switches. A conventional multilevel power inverter topology employs multiple/link voltage of equal magnitudes. It

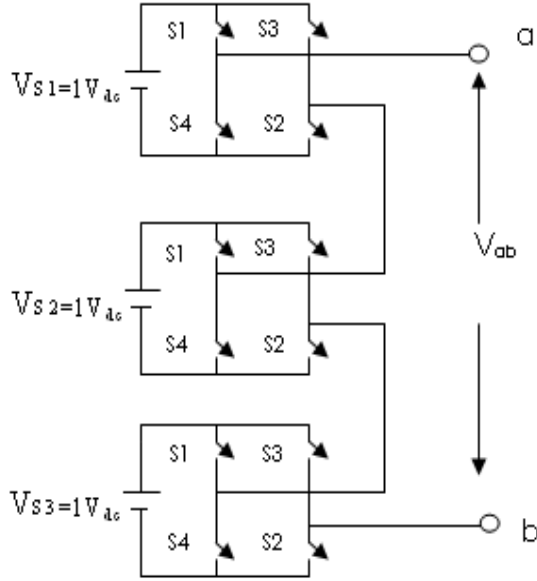is fairly easy to generalize the number of distinct levels [7-11].

Fig .1.Topology for Cascaded H-bridge Multilevel Inverter

The number of sources S or H-bridges and the associated number output level can be written as follows

$$N_{level} = 2S+1 \qquad (1)$$

For example if S=3, the output wave form has 7 levels (±3, ±2, ±1 and 0).The voltage on each stage can be calculated by using the equation below,

$$V_{si} = 1V_{dc} \ (i=1, 2, 3\ldots\ldots) \qquad (2)$$

The number of switches used in this topology is expressed as,

$$N_{switch} = 4S \qquad (3)$$

The advantages of cascaded multilevel inverter are modularized layout of series H-bridges and packaging. This will enable the manufacturing process to be done more quickly and cheaply. Drawbacks of this topology are requirement of a separate DC source for each of the H-bridges and involvement of high number of semiconductor switches.

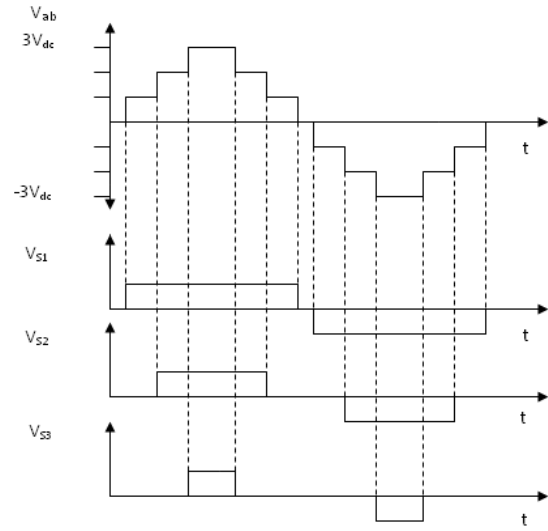Fig. 2 shows the output voltage waveform of a seven level cascaded inverter with three separate DC sources.

Fig. 2. Typical output waveform for cascaded multilevel inverter

3. Hybrid Multilevel Inverter

The general structure of hybrid multilevel inverter for single phase is shown in fig. 3. Each of the separate voltage source V_{s1}, V_{s2}, V_{s3} is connected in cascade with other sources via a special H-bridge circuit associated with it. Each of the circuit consists of four active switching elements which produce the output voltage to be either in positive or negative or zero volts, depending on the switching condition of switches in the circuit. A conventional multilevel power inverter topology employs multiple/link voltage of equal magnitudes. It is fairly easy to generalize the number of distinct levels [12-14].
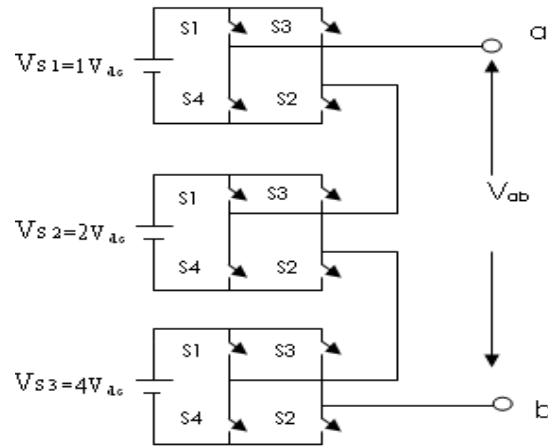

Fig. 3. Topology for Hybrid H-bridge Multilevel Inverter

The number of sources S or H-bridges and the associated number output level can be written as follows

$$N_{level} = 2^{s+1} - 1 \qquad (4)$$

For example if S=3, the output wave form has 15 levels (±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0). The voltage on each stage can be calculated by using the equation below,

$$V_{si} = 2^{s-1}.V_{dc} \ (i=1, 2, 3............) \qquad (5)$$

The number of switches used in this topology is expressed as,

$$N_{switch} = 4 \ S \qquad (6)$$

The advantages of hybrid multilevel inverter are series H-bridges of modularized layout, generation of fifteen level output voltage and fabrication. This will enable the manufacturing process to be done more quickly and cheaply. The draw back of this topology is that it needs a separate DC source for each of the H-bridges and involves same number of semiconductor switches as in cascaded H-bridge inverter. Fig. 4 shows the output voltage waveform of a fifteen level hybrid H-bridge inverter with three separate DC sources.
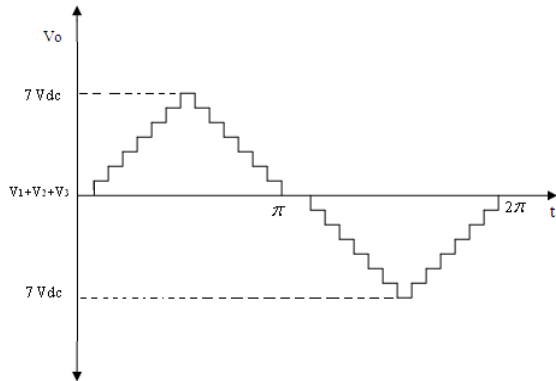

Fig. 4. Typical output waveform for hybrid multilevel inverter

4. Modified Cascaded Multilevel Inverter

The general structure of proposed cascaded multilevel inverter is shown in fig.5. Each voltage source (V_{s1}, V_{s2}, and V_{s3}) is connected in cascade with other sources via a special circuit associated with it. Each stage of the circuit consists of only one active switching element and one bypass diode that can make the output voltage source only in positive polarity with several levels. Initial operation is to turning on of S_1 (when $S_2,S_3...S_n$ turned off) for output voltage level of $+1V_S$. To get an output of $+2V_S$ turning on of S_2 (when $S_3...S_n$ turned off) is done sequentially. Also consequently turning on of S_n^{th} switches will produce nV_S level of output voltage. Only one H-bridge is connected to get both positive and negative polarity. The main advantage of modified cascaded multilevel inverter is seven number of levels with only seven number of switches. For the number of DC sources S or stages, number of output level can be written as follows

$$N_{level} = 2S+1 \qquad (7)$$

For example if S=3, the output wave form has seven levels (±3, ±2, ±1 and 0) which is shown in the Fig. 6 and voltage on each stage can be calculated by using the equation

$$V_i = 1V_s \qquad (i=1, 2, 3...n) \qquad (8)$$

The number of switches used in this topology is expressed as
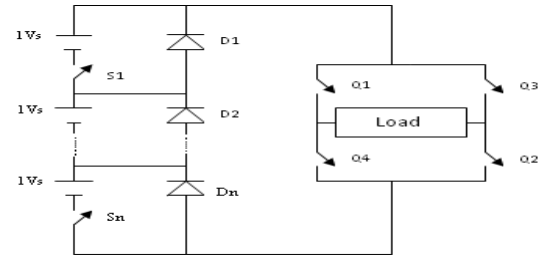
$$N_{switch} = S + 4 \qquad (9)$$

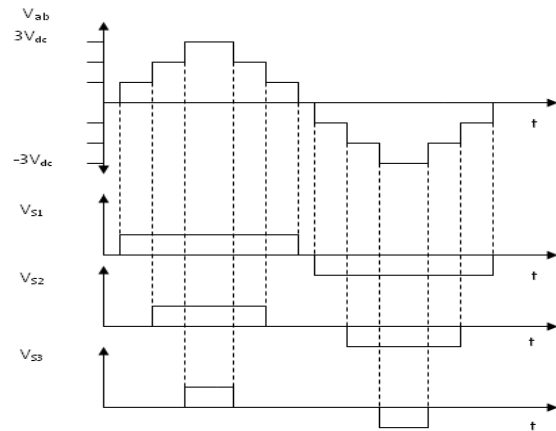Fig. 5. Topology for modified cascaded multilevel inverter

Fig. 6. Typical output waveform for modified cascaded multilevel inverter

5. Modified Hybrid Multilevel Inverter

The general structure of proposed hybrid multilevel inverter is shown in fig. 7. The structure is very much similar to modified cascaded inverter except amplitude of DC voltage sources in unit cells.

The operation is started with turning on of S1 (when S2 and S3 turned off) and the output voltage is +1V_S correspondingly, To go to next level output +2V_S only S2 is operated where S1 and S3 are kept in turned off condition. Similarly for sequent steps turning on of suitable switches at particular intervals can be achieved, Table.1 shows the operation clearly.

The main advantage of modified hybrid multilevel inverter is fifteen levels with existence of only seven switches and three DC sources. The number of DC sources S or stages and the associated number output level can be calculated by using the equation below,

$$N_{level} = 2^{s+1}-1 \qquad (10)$$

For an example if S=3, the output wave form has fifteen levels (±7, ±6, ±5, ±4, ±3, ±2, ±1 and 0). Voltage on each stage can be calculated by using the equation as given,
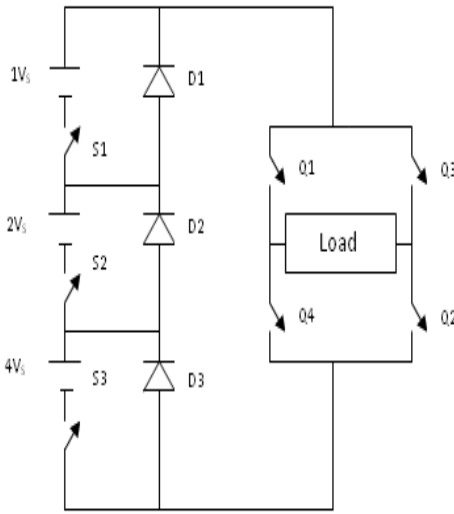
$$V=2^{s-1}.V_{dc} \qquad (11)$$

Fig. 7. Topology for modified hybrid multilevel inverter

The number of switches used in this topology is given by the equation

$$N_{switch}=S+4 \qquad (12)$$

Table 1
Basic Operation of Hybrid Multilevel Inverter

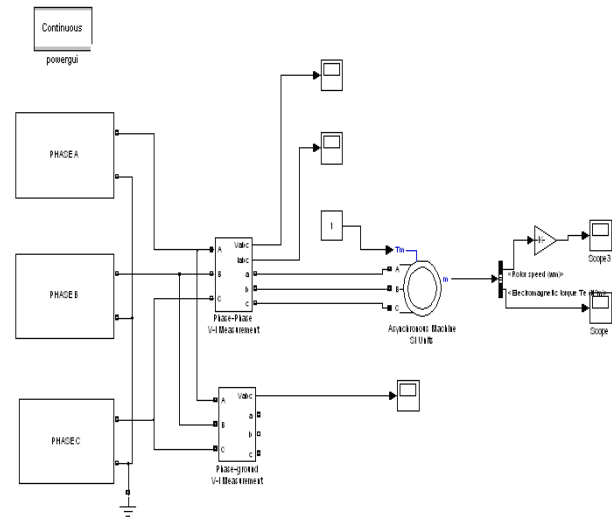| Intervals	On switches	Off switches	Voltage levels	Current flow path
I	S1	S2 , S3	+1Vs	S1,D2,D3
II	S2	S1 , S3	+2Vs	S2,D1,D3
III	S1,S2	S3	+3Vs	S1,S2,D3
IV	S3	S1 , S2	+4Vs	D1,D2,S3
V	S1,S3	S2	+5Vs	S1,D2,S3
VI	S2,S3	S1	+6Vs	D1,S2,S3
VII	S1,S2,S3	-	+7Vs	S1,S2,S3
VIII	-	S1, S2 , S3	0	D1,D2,D3

Fig. 8. Simulation diagram for fifteen level Modified Hybrid Multilevel Inverter for Induction Motor

6. PWM for Harmonics Reduction

PWM technique is extensively used for eliminating harmful low-order harmonics in input, output voltage and current of static power. In PWM control, the inverter switches are turned ON and OFF several times during a half cycle and output voltage is controlled by varying the pulse width. In this proposed multilevel inverter multiple pulse width modulation is used. This involves several number of pulses for each half cycle.

7. Total Harmonic Distortion

In order to determine the relative distortion due to harmonics on a power system, the term Total Harmonic Distortion has emerged. Total harmonic distortion is a measure of the amount of distortion

harmonics cause on the system voltage, expressed as a percentage of the fundamental.

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \times 100\% \qquad (13)$$

Where,

V_h RMS value of harmonic component h;

V_1 RMS value of the fundamental component

8. Simulation Result Analysis

The performance of the proposed modified hybrid multilevel inverter for induction motor drive is verified through the simulation results. Corresponding simulation diagram is shown in fig. 8. It is inferred that input voltages for each succeeding voltage source is 2^{s-1} V_{dc}. The total rms voltage for single phase is 228 V for 15 levels.
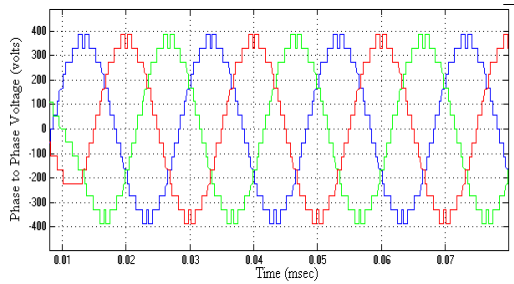

Fig. 9. Three phase line to line output voltage waveform for 15-level modified hybrid multilevel inverter
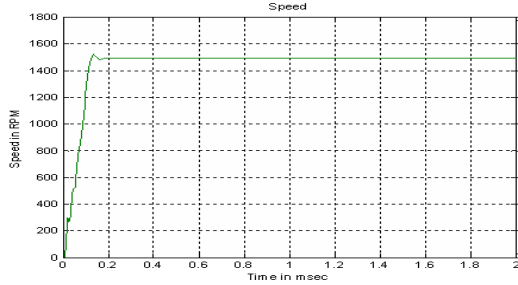

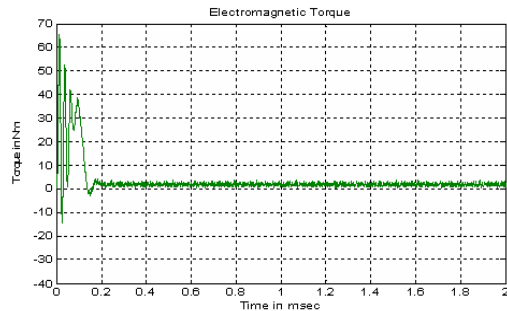Fig. 10. Speed curve of modified hybrid multilevel inverter fed induction motor

Fig. 11. Torque curve of modified hybrid multilevel inverter fed induction motor

Fig. 9, 10 and 11 show the MATLAB simulation output wave form of three phase line to line voltage, speed curve and torque response of induction motor under no load condition. From the FFT analysis window when the number of levels is increased, the harmonics and total harmonic distortion is reduced. Fig. 12 shows THD value of 7.63% for 15 level inverter output.
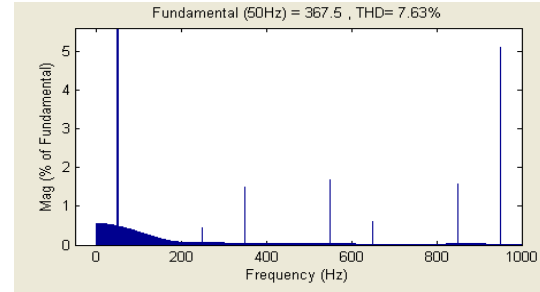

Fig. 12. FFT analysis for fifteen level Modified Hybrid Multilevel inverter

9. Comparison Results

The modified hybrid multilevel inverter involves only seven number of switches compared to the conventional hybrid multilevel inverter. It is described by Table 2. Therefore the proposed modified hybrid multilevel inverter has less switching losses than conventional hybrid and cascaded multilevel inverters.

Table. 2
Comparison of Hybrid and Modified Hybrid Multilevel Inverter

S.NO	Name of the Topology	Voltage on each stage (S)	Number of output level	Number of switches used	Number of switches used for 15 Level
1	Cascaded Multilevel inverter	S Vs	2S+1	4S	28
2	Hybrid Multilevel inverter	2^{S-1} .Vs	2^{S+1} -1	4S	12
3	New cascaded Multilevel inverter	SVs	2S+1	S+4	11
4	Modified Multilevel inverter	2^{S-1} .Vs	2^{S+1} -1	S+4	7

10. Experimental Verification

Simulation of three phase modified hybrid multilevel inverter output voltage is verified with single phase hardware proto type model. Fig 13. depicts the corresponding hardware output waveform. Hardware is included with seven MOSFETs (IRF250) switches, which are connected in modified configuration. Each unit cell is supplied by an asymmetrical DC source. A PIC 16F877 microcontroller is used as the main processor, which provides the gate logic signals. According to microcontroller signal, MOSFET gate terminals are turned on and off. Output of the inverter terminal is connected to R load. The voltage of fifteen level hybrid multilevel inverter is 10.5 volts, with frequency of 50 HZ. The hardware block diagram of modified hybrid multilevel inverter for a single phase is shown in fig. 14.
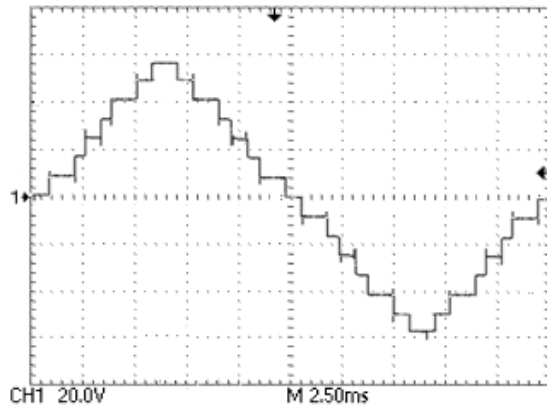

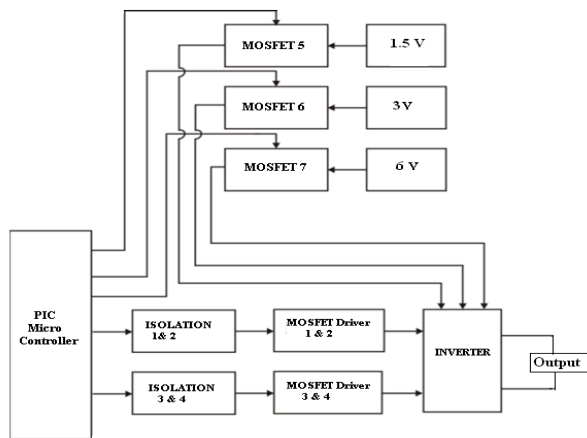Fig.13. Hardware output waveform for modified hybrid multilevel inverter

Fig. 14. Hard ware Block diagram of modified hybrid multilevel inverter

11. Conclusion

This paper revealed that proposed modified hybrid multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications. This multilevel inverter structure and its basic operations have been discussed elaborately. A detailed procedure for calculating required voltage level on each stage has been conversed. As conventional fifteen level inverter involves twelve switches, it increases switching losses, cost and circuit complexity. To achieve same number of output levels, the proposed inverter engages only seven switches with three diodes, which reduces switching losses, cost and circuit complexity. Moreover it effectively diminishes lower order harmonics. Therefore effective reduction of total harmonics distortion is achieved.

Appendix
Motor Details

Rotor Type	: Wound
Nominal Power	: 3730 W
Voltage	: 420 Volts
Frequency	: 50 Hz
Stator Resistance	: 1.115Ω
Stator Inductance	: 0.005974Ω
Rotor Resistance	: 1.083Ω
Rotor Inductance	: 0.005947Ω

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Biography

K.Ramani was born in Vedaranyam on May 7, 1982. He is graduated in 2004 from Bharathiar University, Coimbatore and post graduated in 2006 at Anna University, Chennai. He is a Research scholar in Anna University Chennai under the guidance of Dr.A.Krishnan, Dean, K.S.Rangasamy College of Technology, Tiruchengode.. He is currently working as a professor in the department of EEE at K.S.Rangasamy College of Technology, Tiruchengode from January 2006 onwards. He published 10 international/national conferences, journals. his research interest involves in power electronics, inverter, modeling of induction motor and optimization techniques. He is guiding UG, PG Students. He is an ISTE, IETE member.

M.Murugesan was born in Anthiyur on December 31, 1986. He is graduated in 2009 from Anna University, Chennai. He is post graduated M.E Power Electronics and Drives during 2011 from Anna University. He is currently working as Assistant professor at V.S.B Engineering College. His area of interest involves in Power Electronics, inverter, modeling of induction Motor. He is an ISTE life member. He published 10 international/national conferences, journals

G.Asokkumar was born in Erode on June 11, 1980. He is graduated in 2001 from Bharathidhasan University Trichy. He also received M.E degree in Power Electronics and drives during 2011 from Anna University, Chennai. He is currently working as Assistant professor at Annai Mathammal Sheela Engineering College. His area of interest involves in Power Electronics, BLDC Drives, inverter, modeling of induction Motor. He has published more than 8 papers.