SYNCHRONIZATION MECHANISMS FOR INTERNAL MONITORING AND CONTROL IN POWER ELECTRONICS CONVERTER

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Abstract: *Power Electronics Building Block (PEBB) had been proposed for complex power electronics converters design. A complex converter, such as Modular Multilevel Converter (MMC), may employ up to hundred units of PEBB. Therefore high speed internal ring network is suggested to simplify the wiring system. However, data transmission delay will cause asynchronous operation in PEBBs. This paper will review data transmission delay concept and effects on internal converter control. Three synchronization methods will be reviewed. The most accurate synchronization method will be further tested experimentally. Its achievable maximum latency will be evaluated when different section cable length is used to form the ring and during cable redundancy is activated.*

Key words: *Power Electronics Building Block (PEBB), Ring Network, Synchronization.*

1. Introduction

Distributed generation had been proposed for future smart grid to solve the energy management issues [1-3]. Various kinds of renewable energy systems (wind, solar, micro-hydropower) and storage energy systems (diesel generator, fuel cell or battery banks) can be integrated together into the grid [4-5]. The power transfer from these systems to the utility grid can be efficiently controlled using different range of power electronics converters [6-8]. Various digital control techniques have been proposed and implemented with the enhancement in microcontroller, Digital Signal Processor and FPGA [9-10].

Since different range of power electronics converters will become highly demanded, standardizing the converter design will help to simplify the process and reduce production time. Power Electronics Building Blocks (PEBBs) concept has been proposed. PEBB is a special designed hardware with the power semiconductors, gate drivers, sensors (voltage, current, and temperature), analog-to digital converter and protection circuit assembled in one single block [11-13]. The power switches can be freely configured in half-bridge or full-bridge based on a specific application. The goal is to reduce the size, operational and maintenance costs as well as provides an open plug and play design platform [14]. Thus, different range of power converters can be easily developed.

The concept of PEBBs is well suited for multilevel converters. Multilevel converter produce staircase output waveform. The output voltage may easily be scalable by adding in PEBBs. As the output waveform approaches the sinusoidal wave, total harmonic distortion is minimized. Therefore, they have been widely used in power distribution control and management [15-16]. For example, thirteen levels Cascaded H-Bridge has been proposed as static compensators [17]. The total number of PEBBs used in this application is 18 units. Although the number of PEBBs increases, they are still manageable through the classical star control interface. In star topology, all PEBBs will receive their gating signals directly from the master controller. Consequently, all the status updates and sensor measurements will be sent to the master controller with point-to-point cables.

If a converter owns few hundreds of PEBBs per phase [18], it may require a large number of wires to deliver the control, measurements and status signals. These wires properly will also increase the cost and noise problems in the converter. Due to the complexity of the star network topology, ring control network has been proposed [19-21]. All control commands, measurement variables and status updates will be put in data packet formats and transfer through the ring. As a result the complex data lines can be simplified by one ring.

The data transmission delay in ring network must be precisely compensated to prevent the converter from having catastrophic failure. In addition, the availability of data communication must be strengthened. A link breakage or a node failure in ring network may cause the master controller loss communication with other PEBBs located after the failure point. Therefore, a duplicate communication path is highly recommended. However, integrating synchronization protocol and cable redundancy together within a ring is always a challenge [22-24].

This paper will first presents the synchronization requirement and mechanisms used to properly sync up PEBBs in ring control interface. Then, an evaluation on the synchronous accuracy will be conducted based on two scenarios (different communication cable length used in ring and cable redundancy is activated). The rest of this paper is organized as follows: First, the basic communication requirements for internal monitoring and control in power electronics converter will be reviewed in Section 2. Then a detail study in synchronization requirement will be presented in Section 3. The acceptable delay will be proposed. Section 4 mainly reviews the available synchronization mechanisms which had been proposed for internal converter control. This is followed by a discussion and experiment evaluation to the most accurate synchronization method in Section 5. Lastly, Section 6 gives the conclusion.

2. Basic communication requirements in power electronics converter

The general requirement for monitoring and control in power electronics converter will be discussed based on a few important aspects listed in Table I.

Ring topology is an appropriate network topology to simplify the wiring system in converter. A master controller and PEBB units are defined as communication network nodes in a ring system. The total number of network nodes depends on the power electronics converter application. For example, a Modular Multilevel Converter which designed for motor drive control (medium voltage application) may only employ 10 units of PEBB per phase [25]. While for high voltage application (HVDC), the number of PEBB may increase more than 200 units per phase [18]. When the number of PEBBs increases more than hundred units, phase-based parallel control ring [20] is an alternative for simultaneous control and monitoring of PEBBs on each phase. Two adjacent PEBBs should always place close to each other and connected with a section of communication cable. Fiber optic is preferable as the transmission medium mainly due to its noise immunities, light weight and high speed transmission [26].

Since all data is transfer from node to node in data packet format, each node will be assigned a unique address to ease data handling. A PEBB will only accept the data packet which is specifically assigned to it. Therefore, a Slave Communication Controller (SCC) is coupled to a PEBB for data processing. Similarly the master controller will require a Master Communication Controller (MCC) to schedule the data messages. A total of 4 bytes data payload is sufficient for internal monitoring and control. Each PEBB will execute periodic sampling on voltage, current, temperature, operating status and etc. These data will be packed and sent to the master controller as input data. The master controller will start process the data after gathering all information from PEBBs. The duty cycle ratio will be determined based on a specific modulation control algorithm. Then, the output data (modulation and synchronization information) will be transmitted back to each PEBB.

The total cycle time starts form the sampling event at PEBBs until they received back their corresponding switching commands is normally specified by the converter switching frequency. A high switching frequency converter will highly require a short cycle time to complete all the data exchange and computation. For instance, minimum cycle time must be less than 50 μs for a converter with 20 kHz switching frequency. Conversely, longer cycle time is allowed for low frequency converter. So, the minimum cycle time is set as 100μs as the basic requirement. Cycle time analysis within power electronics converter had been study in [21].

Table 1
Basic communication requirements for internal monitoring and control in power electronics converters

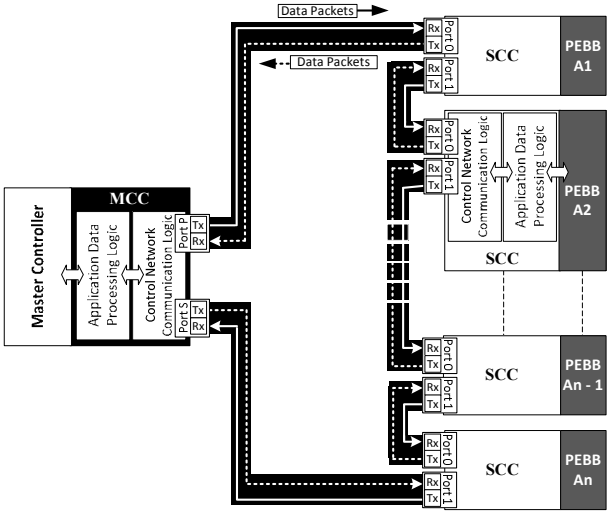
Aspect	Optimal
Network topology	Ring topology
Transmission Medium	Optical fiber
Communication mode	Master-Slave, Master-Master, Slave-Slave
Network nodes	Depend on application
Data payload	4 bytes (minimum)
Bandwidth	≈ 100 Mb/s
Minimum cycle time	100 μs
Fault tolerance	Communication cable redundancy, Silent failover
Synchronization	Necessary

The required data bandwidth in power electronics converter system can be estimated using the following equation:

$$Bandwidth = n_{PEBB} \times n_{bit\_DP} \times f_{sw} \quad (1)$$

Where n_{PEBB} indicates the total number of PEBBs appears in a ring system. The total number of bit in a data packet is designated by n_{bit_DP}. The switching frequency of the power electronics converter is presented by f_{sw}. The bandwidth is proposed to set as 100Mbps since it is proportional to the product of variables in (1).

The classical communication mode in power electronics converter control is named as Master-Slave communication mode. However, Master-Master or slave-slave (peer-peer) communication mode allows redundancy control. A backup controller and some redundant PEBBs should be placed in the system to ensure the converter remains in normal operation when some of the units fail. To increase the reliability, communication cable redundancy has been proposed [27-28]. The duplicate communication link will circulate duplicate data packets in an opposite direction. This ensures continuous data exchange in case of section cable fault or slave communication controller error. Fig. 1 shows the basic structure of a ring control interface which is used for internal monitoring and control of all PEBBs. Table 1 summarized the basic communication for monitoring and control in power electronics converter.



MCC = Master Communication Controller
SCC = Slave Communication Controller

Fig. 1: Basic structure of ring control interface in power electronics converter.

3. Synchronous operation of PEBBs in power electronics converter

Power electronics converter always requires highly synchronize operation to turn-on or turn-off the semiconductor switches in all PEBBs. In the conventional star control interface, each power semiconductors are directly control by the master controller. The gating signal is sent using point to point copper cable. As long as the master controller manages to generate the switching pattern for all PEBBs simultaneously, the synchronous operation can achieve easily. However, in the proposed ring control interface, the switching commands will be packed in a telegram and being transfer from PEBB to PEBB. Latency (data transmission delay) is inevitable. This section will first review the definition of latency and its effect in a power electronics converter. Then the concept of clock synchronization which account for PEBBs synchronous operation will be presented. Finally, an acceptable maximum delay for internal control of a converter will be proposed.

3.1 Ring network latency in power electronics converter

The latency of transferring a data message from a PEBB to its adjacent PEBB is made up of three components, i.e. transmission time, propagation delay, and processing delay. Transmission time, t_{tx}, is measures when the first bit leaving the sender node and the last bit arrives at the neighbor node. It varies accordingly to the size of data packet and the bandwidth used in the communication ring. Propagation delay, t_p, represents the required time for a bit to move from node to node. It mainly depends on the length and types of the transmission medium being used (L_{tx_medium}). Besides, the frequency of propagate signal (τ_p) may also vary the speed of propagation. The third component, processing delay, $t_{processing}$ refers to the time taken by a node to examine the data packet header, which normally include bit-level errors checking and address verifying [26]. $t_{processing}$ is assumed equivalent for each PEBB in the ring since all slave communication controllers are identical.

$$\begin{aligned} t_{delay} &= t_{tx} + t_p + t_{processing} \\ &= \frac{message\ size}{Bandwidth} + \left(\tau_p \times L_{tx\_medium}\right) + t_{processing} \end{aligned} \quad (2)$$

Fig. 2 illustrates the cumulative delays scenario. Assume same lengths of wires are used to connect two neighbor nodes in the ring network; the first PEBB may encounter latency, t_{delay} to receive its switching command. Consequently, the second PEBB will need to wait for $2t_{delay}$ to get its telegram. This propagation delay is accumulated from PEBB to PEBB. Thus, the last PEBB will encounter n times of t_{delay} to obtain its gating signals. If these delays are not properly being compensated in each PEBB, asynchronous switching operation will be conducted.

The effect of this cumulative delay had been simulated in a three phase boost converter [29]. The half-bridge power module in each phase is defined as a PEBB. So this simulation model illustrates a simple ring network which

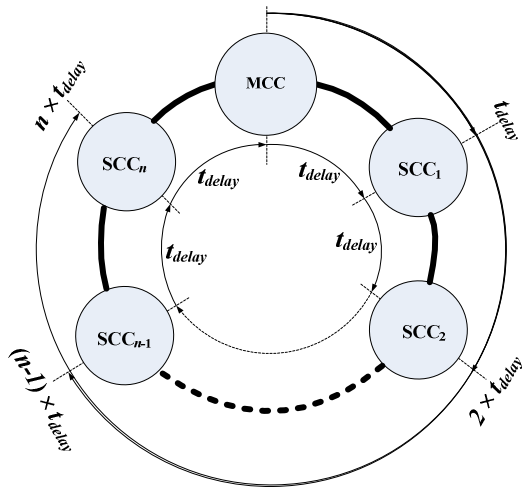


Fig. 2: Cumulative latency in ring network. Assume same length of communication cable is used to connect two neighbor nodes.

owns three units of PEBBs. The switching frequency is chosen as 20 kHz. A 0.5 μs delay (1% of the switching period) is introduced between two PEBBs. Small ripples start appearring in phase currents and DC link voltage. When the propagation delay increases to 5% of the switching period (2.5 μs), the first and third (last) PEBB will switch with a total of 5 μs delay. This delay is big enough to cause significant voltage and currents ripples to fail the converter. So, in case of a converter with hundreds unit of PEBBs, the last PEBB may encounter a huge delay. Although high voltage converter normally operated in low switching frequency, this cumulative delay is large enough to generate an incorrect output voltage level as explain in [30]. As a result, the converter may suffer catastrophic failure.

3.2 Clock synchronization protocol

To achieve synchronous operation, each node should employ a local clock (crystal oscillator). Then, a clock synchronization protocol either general-purpose or special purpose can be employed for distributed real-time control [31-32]. Basically, three steps are required to fully synchronize all the clocks. By identifying one of the local clocks as the main reference clock, static clock delay measurements will first be carried out. Then, necessary compensation can be conducted in each local clock. Finally, fine tuning of the local clock drift can be performed periodically. Data transmission delay highlighted in (2) is considered as one of the static clock delay. The data frame size, network bandwidth, communication cable are fixed throughout the converter operation. The offset between a local clock and the reference clock is also grouped as static clock delay. This offset is due to all local clocks are not synchronous to the reference clock as start up. Clock drifting is considered as a dynamic delay cause by the individual quartz variations between the reference clock and each particular local clock. When a local clock is slower than the reference clock, the speed of the local clock will be

increased. Conversely, it will be slowed down when it is found running faster than the reference clock.

When all nodes achieve clocks synchronization, the local clock can be used to generate a synchronization pulse signal to produce the power semiconductors' gating signals. Fig. 3 illustrates an example of generating the gating signals in each SCC (Slave communication Controller) locally. Assume the PWM switching command is sent in 16 bits. A 16-bit counter will be initialized on the rising edge of the synchronization pulse, *Sync* signal. The upper and lower switches gating signals for two switches in half-bridge configuration is produced by comparing the 16 bit PWM command with the running counter.

3.3 Maximum acceptable range of delay and jitter

Although the absolute constant delay can be compensated, a delay variation (jitter) is still inevitable. Jitter is an undesired deviation time of data packets reaching PEBBs in real-time transmission. It is a non-deterministic variable but may limit its range by clock synchronization algorithms. A precise clock synchronization algorithm will always keep the jitter as low as possible.

In power electronics converter, the latency and jitter are insignificant for low frequency converter. However, high frequency power electronics converters must ensure both the delay and jitter fall within the acceptable range. This range depends on the available time resolution per bit for alignment. Two key parameters mainly form the time resolution per bit, $\Delta t_{Resolution/bit}$. They are switching period of the power electronics converter, T_{sw} and resolution for a switching command n_{sw_bit}:

$$\Delta t_{\text{Resolution/bit}} = \frac{T_{sw}}{2^{n_{sw\_bit}}} \tag{3}$$

The maximum acceptable delay including the jitter is proposed to set around ±20 ns. For instant, a 10 kHz power electronics converter encodes its PWM signal as a 16-bit data (Fig. 3). This will achieve a resolution of approximately 1.53 ns per bit. Therefore, this converter may reserve ± 13 steps for alignment to achieve synchronous operation.

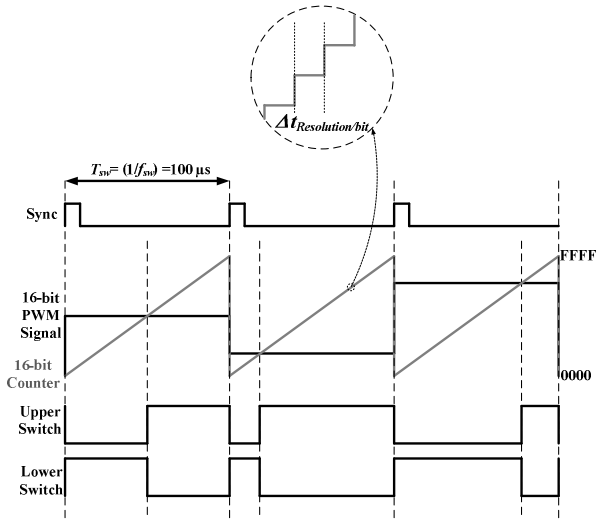


Fig. 3: Timing diagram for producing two switching signals to a half-bridge power module base on 16 bits PWM commands. Assume the converter is operated with a typical 10 kHz switching frequency.

4. Review of synchronization schemes for internal control in power electronics converters

This section will briefly review three synchronization mechanisms which have been proposed for internal monitoring and control in power electronics converter. Two custom-made synchronization schemes (PESNet 2.2 [33] and TSBS [20]) will first be presented. The reason behind custom-designed is claimed as the existing field bus such as MACRO [34] and SERCOS III [35] do not support the tight synchronous requirement to conduct simultaneous switching in PEBBs. Besides, the available control networks are too complex and have unnecessary functionality which are not required in power electronics converter. Recently, an industrial network, EtherCAT has been proposed. With its specialities on summation frame structuce and flexible data payload, it seems overcome the above mentions drawbacks [21], [36]. Its synchronization mechanism will be reviewed later.

4.1 Power Electronics System Network (PESNet)

PESNet is a custom-made control network for power electronics converter developed by Virginia Polytechnic research team [19], [37]. It may support up to 256 PEBBs per ring. The maximum data bandwidth is 125Mbps. PESNet uses optical fiber to link up an Application Manager and some units of Hardware Manager in a ring network. Application Manager acts as the master controller responsible for system initialization, implements synchronization mechanism and converter control schemes. Hardware Manager is actually a Slave Communication Controller which mainly provides communication interface with control and monitoring to a PEBB.

Network clock concept has been introduced since PESNet 2.2 [33]. A predefined communication period (default value = 2 µs) is used to cover the propagation delay in between two neighbor nodes. The master controller owns an internal counter which is identified as the master network clock in the ring. All slave nodes' local counters will be tuned accordingly to the master counter value when the synchronization sequence is kicked start. During the synchronization sequence, process data will be halt and null data will be sent using the synchronization data frame. All network nodes will continuously transmitting telegram every 2 µs until the synchronization sequence is over.

A synchronous packet will be sent by master controller to initiate synchronization process. The master network clock will automatically incremented with the time stamped in the synchronization packet. When the packet arrives at the first slave node, the time value on the synchronization packet will refresh that particular node's local clock value. Hence, this node's local clock is now synchronized with the master network clock. Then the synchronization packet will be forwarded to the subsequence slave nodes with the network clock value incremented and stamped onto the packet. The total times to fully synchronize all slave nodes will vary

according to the number of nodes appear on the ring. A figure illustrates the synchronization mechanism in PESNet 2.2 can be found in [38].

Once, all the local clocks have been synchronized, the master controller may tag a scheduled network time in the process data packet which contains a PEBB switching command. When the node receives its switching command, it will wait for its local clock to reach the given schedule time in order to execute the switching command on the PEBB. An experiment result shown that the PESNet achieved 80 ns synchronization jitter for a simple three PEBBs system [37].

4.2 Time-Stamping-Based Synchronization Method (TSBS)

Lappeenranta University of Technology had proposed a flexible time-stamping-based synchronization method which can be integrated with various communication protocols [20]. The data rate used was 100 Mbit/s. Plastic optical fiber is defined as the transmission medium. This mechanism adopted time stamping scheme which is very similar to the IEEE 1588 Standard.

In TSBS method, all nodes have a local clock and the master clock is owned by master controller. During the initialization state, master controller will send a test message mainly to check the ring validity and assign device ID to each slave nodes (PEBBs). Once the test message returns to the master controller, the total number of slave nodes in the ring is determined. The master controller will then circulate a synchronization packet through the ring. All nodes (include the master node) will stamp the transmission time and arrival time of this synchronization message. Each slave node will calculate its particular processing time by subtracting the message arrival time from its transmission time. The obtained processing time value will be forwarded back to the master controller. All slave nodes will keep a copy of its preceding node processing delay for calculating the cumulative delay later.

By collecting all the processing time delay from the slaves, master controller will start estimating the average internode delay. Internode delay mainly covers the data transmission delay and propagation delay defined in Section III. The transmission and reception time in master controller determines the total required time for a message to flow through the ring. So the average internode delay can be easily obtained when the master controller knows the total processing delays and the total number of nodes in the ring. When computation completes, master controller will broadcast the transmission time and the average internode delay. Every slave node will calculates its total delay time and the offset referring to the master node individually and tune its local clock respectively. The synchronization sequence is repeated periodically for drift corrections. The details of this synchronization schemes are given in [20], [39-40].

Experiment results in TSBS method had proven that a synchronization jitter between each pair of adjacent nodes is about 10ns [40]. However, the overall jitter for a system will accumulate based on the number of slave nodes in the ring. For instance a ring which contains four PEBBs may give a total of 40 ns jitter. In addition, if a static error is detected in the system, an additional 20ns jitter has to be counted.

4.3 EtherCAT

EtherCAT had been widely used in Control Automation Technology which may accommodate up to 65535 network nodes. The data rates may exit 100Mbps with full-duplex transmission [41]. EtherCAT Master Controller (EMC) which mainly in charge of scheduling data packets and managing synchronization mechanism is commonly found as software driver installing in a PC equipped with standard network controller. EtherCAT Slave Controller (ESC), which designed in IP Core, is suitable to download as control network communication logic in each SCC (Fig. 1). Ethernet twisted pair copper cable is used as the transmission medium.

EtherCAT implements an accurate time-stamping synchronization mechanism known as Distributed Clocks (DC). All ESCs must enable DC feature in power converter system. The first ESC will automatically recognize as the reference node with its local clock used as System Time in the ring. (EMC) will broadcast a measurement message to initialize the clock synchronization process. All ESCs will record theirs local time upon receiving this message in a specific register locally. When the measurement message reaches the last ESC in a network, it will be forwarding backward from the last ESC to the first ESC and back to the EMC. On its way back, all nodes will capture and store the message arrival time in another register. When the EMC finally received back the measurement message, it will perform a read cycle to collect all the stamping times from each node and calculate the specific propagation delay between the reference node and a slave node. Besides, the offset time will also be determined. The computed propagation delay and offset time will then be sent back to each slave node. With this information, each slave node manages to produce its local copy of system time. EMC will distribute the reference clock value (System Time) to all ESC periodically for drift compensation. Time Control Loop algorithm in each ESC will compare and tune its local copy of system time base on the received System Time. A details explanation of DC Mechanism basics can be found from [30], [33], [42-43].

EtherCAT supports generation of "SyncSignal" in all DC enable devices which can be directly used to synchronize all PEBBs switching execution accurately. Experimental results show that three units of PEBBs achieve synchronous switching with small latency less than ± 20 ns in a healthy ring [30].

5. Discussion and experimental results

PESNet 2.2 synchronization mechanism is tightly coupled to the predefined communication period. Varying in the cable type/length or data frame sizes will need to manually recalculate an appropriate communication period. This

method is not flexible. During the PESNet synchronization sequence, the data exchange has to be temporary terminated. This may interrupt the control of a converter. For instance, a complex converter with 50 units of PEBB will need approximately 100 µs to complete the synchronization sequence (if 2 µs communication period is used). However, this synchronization method has no conflict to work with cable redundancy. The cable redundancy used in PESNet 2.2 is originated from FDDI (Fiber Distributed Data Interface) concept. The secondary communication path will only be activated when fault occurs; the data packet will then be circulated through the secondary link to another end of the broken ring. Therefore, the proposed synchronization sequence will be completed with slightly longer time when ring breaks.

As compare to PESNet, the auto-tuned clocks mechanisms in TSBS method increases the flexibility for converters with PEBBs-based designed. However, the cumulative synchronization jitter may still fail to meet the synchronization requirement for a complex converter. The synchronization jitter may accumulate above 1 µs for a converter consists of more than hundred units of PEBBs in a ring. Furthermore, the average internode delay calculation will only be perfect if each section of the communication cable used to link up two adjacent nodes is identical. However, when constructing the converter into a panel, different length of fiber optic might be used to connect two neighbor nodes, especially for converter which has large number of PEBBs. There are no research works published to evaluate TSBS method combine with communication cable redundancy.

EtherCAT Distributed Clocks (DC) implements time stamping mechanism similar to TSBS. Each nodes performs the second time stamping on the returning synchronization frame increases the accuracy of the internode delay calculation. The following sub-section will present a test to closely validate EtherCAT Distributed Clocks (DC) mechanism when different length of section cable is used and during cable redundancy is activated.

5.1 Experimental Setup

Fig. 4 shows a four nodes control ring. The master node consists of an Industrial PC (IPC) from National Instruments (NI PXIe-8133) and a Real-Time Ethernet Port multiplier (CU2508). TwinCAT network card driver (version 2.11 build 2232) including the redundancy supplement is installed in the IPC to serve as EtherCAT Master Controller. CU2508 is required to support synchronization management when cable redundancy is activated. It will be recognized as the first DC enable device. Its local clock establishes the System Time [44]. The three slave nodes are identical. Each of them contains a Piggyback Controller Boards (FB1130) as Slave Communication Controller. Power switches are integrated in half-bridge module on each PEBB. Five Ethernet cables are used in this set up. They are varies in length as shown in Fig 4.

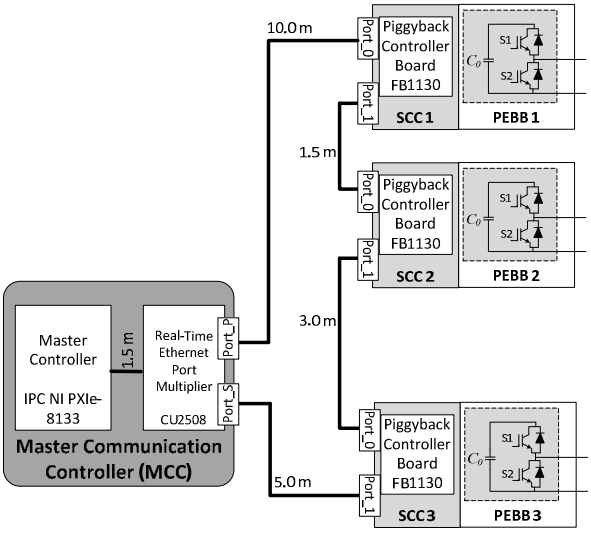


Fig. 4: Experiment setup for ring communication control with different length of section cable (1.5m, 3.0m, 5.0m and 10.0m).

5.2 Experimental Results

Three experiments will be conducted to study the achievable latency range of EtherCAT DC mechanisms. A typical switching frequency of 10 kHz is selected in the following experiments. All PEBBs will receive similar PWM switching patterns (all upper switches, *S1*s will be trigger on or off simultaneously). The lower switch, *S2* must always complement to the upper switch. The first experiment is performed with the ring stay healthy as in

Fig. 4. The zoom in view results of PEBBs gating signals are shown in Fig. 5 and Fig. 6. All the gating signals trigger synchronously without any delay; a jitter of less than ± 10 ns is captured. EtherCAT DC mechanisms had accurately tuned each local clock even when different length of section cables used in the ring.

Experiment 2 and 3 create the fault scenarios (link fault and SCC fault) to evaluate the synchronous switching operation with cable redundancy. Fig. 7 and Fig. 8 illustrate communication cable failure results (The communication cable between SCC2 and SCC3 is removed). All PEBBs continue to receive switching commands although the ring breaks. Small latency approximate 30 ns can be observed between PEBB1 and PEBB3. Then SCC2 is switched off to demonstrate node failure. Fig. 9 and Fig. 10 show that PEBB1 and PEBB3 continue to generate switching pattern except PEBB2 (node failure). The latency is approximately 15 ns.

Both experiments prove that the jitter in each node remain less than ± 10 ns. When the ring breaks, all data packets continue to be sent using the EtherCAT cable redundancy. Small delays are found within the power converter maximum acceptable latency range.

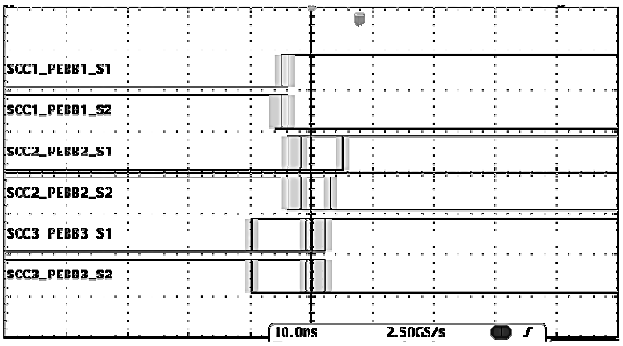


Fig. 5: Zoom in view of PEBBs switching signals – S1 switching on (10 ns/div)

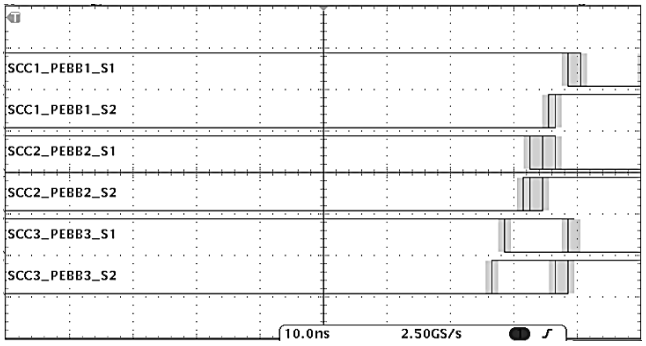


Fig. 6: Zoom in view of PEBBs switching signals – S1 switching off (10 ns/div)

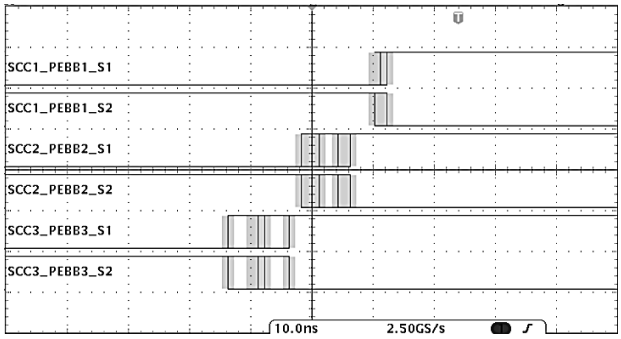


Fig. 7: Zoom in view of PEBBs switching signals when a section of cable failure in between SCC2 and SCC3 – S1 switching on (10 ns/div)

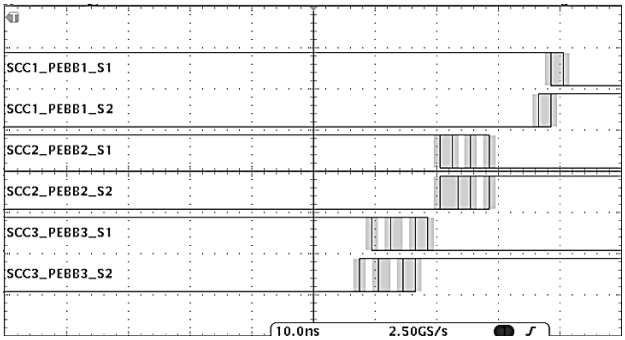


Fig. 8: Zoom in view of PEBBs switching signals when a section of cable failure in between SCC2 and SCC3 – S1 switching off (10 ns/div)

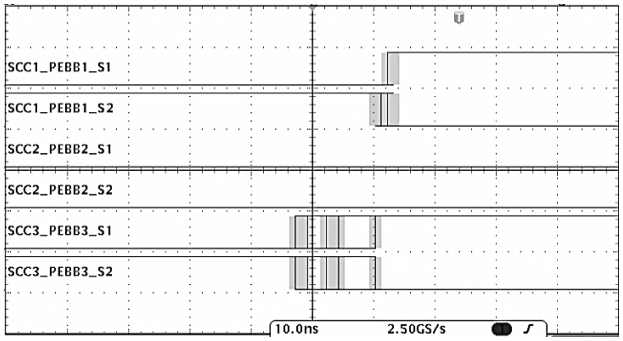


Fig. 9: Zoom in view of PEBBs switching signals when node fault occurs – S1 switching on (10 ns/div)

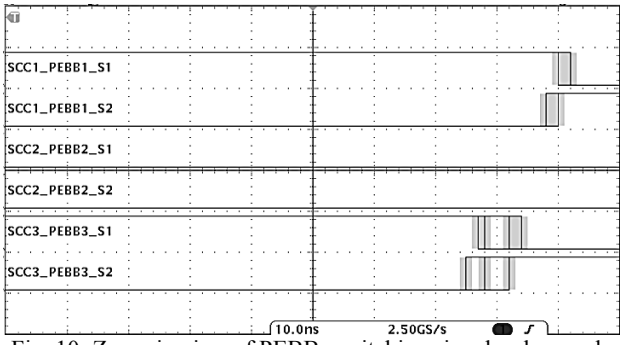


Fig. 10: Zoom in view of PEBBs switching signals when node fault occurs – S1 switching off (10 ns/div)

6. Conclusion

Power Electronics Building Block (PEBB) had been proposed to simplify the design process in complex power electronics converter such as multilevel converter. However, the classical control interface requires a large number of wires to deliver the control, measurements and status signals between PEBBs and master controller. Thus a ring communication network is suggested to reduce the complexity in wiring for a complex converter which in extreme cases may have hundred units of PEBBs. All sensor measurement and gating signals will be packed in telegram and circulated through the ring.

A set of basic communication requirements for internal monitoring and control in power electronics converter are discussed. A detail study on strict synchronization requirement has been presented. The maximum acceptable latency is proposed as ± 20 ns.

Three existing synchronization methods which had been proposed for ring control in power converter are reviewed. They include Network Clock mechanism in PESNet 2.2, Time-Stamping-Based Synchronization Method (TSBS) and Distributed Clock (DC) Mechanism in EtherCAT. Flexibility and accuracy of these methods have been discussed. The DC mechanism is recognized as the most precise protocol from this study. The time stamping on the returning synchronization frame becomes the main factor of preciseness. Thus EtherCAT is further examined experimentally using different length of communication cable as well as when cable redundancy is activated. The experimental results show that EtherCAT fulfills the proposed maximum acceptable latency range for control of power electronics converters.

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