

# Capacitor voltage balancing control for CHB multilevel inverter considering harmonic distortion based on Programmed Matrix PWM

Lazhar manai Faouzi Armi

*Higher institute of information technology and communications*

*Research and Technology Centre of Energy-PV laboratory, P.B N°95 2050 - Hammam Lif – Tunisia*

*manai\_lazhar@yahoo.fr armifaouzi@gmail.com*

**Abstract**— *In this paper, a programmed matrix pulse generator is developed to generate PWM controls signals synchronized with switching angles which are obtained as a result of Trust-region Dogleg analysis. Trust-region Dogleg method is more flexible and efficient than conventional optimization techniques and it can be extended to any m level CHB multilevel inverter operating at any switching frequency. Programmed matrix PWM allows balancing CHB multilevel inverter capacitor voltages, eliminating certain harmonic orders and avoiding dead time insertion in commutation cells control signals. Performance of the proposed method for a five-level cascaded H-bridge inverter, based on simulation studies, is evaluated and experimentally verified.*

**Key words:** *Programmed matrix PWM, Trust-region Dogleg method, CHB multilevel inverter, capacitor voltage balancing.*

## 1. Introduction

With multilevel inverter, as numbers of levels are increased, the output voltage steps generating waveform increased synchronously and at the same time the harmonic distortions are decreased [1,2]. The main advantages of multilevel inverters compared to conventional two-level inverters are lower cost, higher performance, less electromagnetic interference, and lower harmonic content [1]. The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge (CHB) inverters with separate dc voltages. Due to modularity

and the ability to operate at higher voltage levels, the CHB topology is preferred for high-power applications among other topologies [3].

In CHB inverters, as the number of levels increases, the quality of the output signal will be improved, and the inverter output voltage waveform will be closer to a sinusoidal waveform [4]. Moreover, high voltages can be managed at the dc and ac sides of the inverter, while each unit endures only a part of the total dc voltage. But the most extensively addressed drawbacks of CHB inverters are the dc voltage balance control across all dc capacitors of the H-bridge units and the dead time insertion in complementary commutation cells control signals [5]. Both have huge influences on the quality of the multilevel inverter output voltage waveform. In fact THD increase when the introduced dead time increase, mainly in low frequency and when the capacity voltages are unbalanced. Furthermore, balancing units' output fundamental voltages and avoiding dead in CHB multilevel inverter commutation cells control signals to minimize harmonic distortion level still remain challenging issues [6,7].

Several methods are put forth for the harmonic elimination in literature. The methods proceeds from the basic sinusoidal pulse width modulation (SPWM) which are not able to eliminate lower harmonics completely [8,9] and space vector modulation (SVM) where the application of SVM in cascaded topologies is usually limited to a small number of levels due to the large number of switching vectors [10,11].

Selective harmonic elimination pulse width modulation (SHE PWM) is employed in multilevel inverters which require solving the non linear harmonic equations in order to eliminate certain harmonic orders by the generation of switching angles corresponding to harmonic elimination. Theory of resultant is proposed in many researchers to derive the mathematical model, but this method is complicated, time consuming and not suitable for the varying input sources.

In fact many studies have been carried out to find optimal angles using optimization techniques such as polynomial resultants theory (PRT) [12] or genetic-algorithm (GA)-based solutions [8]. In the PRT solution, when the voltage levels of multilevel inverters are high, the resulting high order polynomial terms can no longer be solved. In a GA-based method, the main challenge is that the result may fall into the trap of local minimums. Therefore, despite its considerable efficiency for large dimension optimization problems, it cannot guarantee the best optimized result [3].

In this paper selective harmonic elimination technique is implemented using Trust Region Dog Leg. This algorithm resulted from previous useful algorithms to compensate their shortcomings. In particular:

- The class of methods based on the Newton iteration fails whenever the Jacobean matrix becomes singular, and when the initial guess is far from the solution.
- The steepest descent method assures the movement in a direction that decreases the objective function, but the steps are very small and the computation time is large.

Dogleg utilizes Newton and steepest descent methods. The combination of these two methods ensures a fast convergence and a solution of function in the steepest descent direction. Trust-region method has better computational efficiency and exhibits more stable convergence characteristic. It is considerably more robust than other optimization methods without any extra computational burden.

In this paper, Trust region dogleg optimization technique is utilized to find out the optimized switching angles using a set of non-linear equations derived to selectively eliminate specific harmonics (Selective Harmonic Elimination). As result, a programmed matrix PWM (PMPWM) is developed which allows:

- Replace HB cell DC voltage with a capacitor and provides voltage regulation across its voltage
- Eliminate certain order harmonics
- Avoid the dead time insertion in complementary commutation cells control signals
- Obtain the desired multilevel inverter output voltage wave form with minimum Total Harmonic Distortion (THD)

This paper is organized as follows. Section 2 describes power topology of cascade multilevel inverter. Harmonic minimization problem in CHB multilevel inverter based on trust region Dogleg optimization is explained in section 3. Section 4 provides the detailed analytical discussion of programmed matrix PWM and voltage balancing control methods. Simulation results are included in section 5. Experimental results are presented in section 6. Finally, the concluding remarks are drawn in section 7

## 2. Power Topology Of Cascade H-BRDIGE multilevel inverter

The basic structure of hybrid multilevel inverter is based on connection of H-Bridge inverter units (HBs). Figure 1(a) shows the circuit for one phase leg of a multilevel inverter with  $j$  HBs in each phase. Each unit has its own separated dc source (SDCS), which may be obtained from an ultracapacitor, battery, fuel cell, solar cell, etc [3,4]. In order to generate the multilevel voltage waveform, the ac terminal voltages of different H-bridge inverters are connected in series, and the overall output voltage  $V_a$  is given by the sum of H-bridge voltages [6]. Each full bridge inverter can generate three different dc voltage levels of  $+E$ ,  $0$  and  $-E$  in its ac terminal, which depends on the state of four commutation cells  $Si_1$ ,  $Si_2$ ,  $Si_3$ , and  $Si_4$ , such as  $i$  represents the H-bridge number with  $i \in [1 j]$  [13]. To obtain  $+E$ ,  $Si_1$  and  $Si_3$  switches are turned on. While for  $-E$  level  $Si_2$  and  $Si_3$  are turned on. The output voltage would be made zero while switching on either the switch pairs  $Si_1$  and  $Si_3$  or  $Si_2$  and  $Si_4$  [7]. If the DC-link voltages of HBs are identical, is called symmetrical multilevel inverter. However, it is possible to have different values among the DC-link voltages of HBs, and the circuit could be called Asymmetrical multilevel inverter. In a symmetrical cascade multilevel inverter where the DC-link voltages of HBs are identical, for  $j$  HB units one phase leg, DC link

voltages are  $V_1=V_2=\dots=V_j=E$ , where  $E$  is the unit voltage. The numbers of output level are normalized by:

$$m = 2j + 1 \quad (1)$$

$j$  is the number of the H-Bridge inverter connected in series, and  $m$  is the number of output levels in each phase as seen in equation (1).

The synthesized single-phase staircase voltage of an  $m$ -level cascade inverter is illustrated in Figure 1(b). To obtain the three-phase configuration, the outputs of three single-phase cascaded inverters can be connected in Y or  $\Delta$  shape [12].

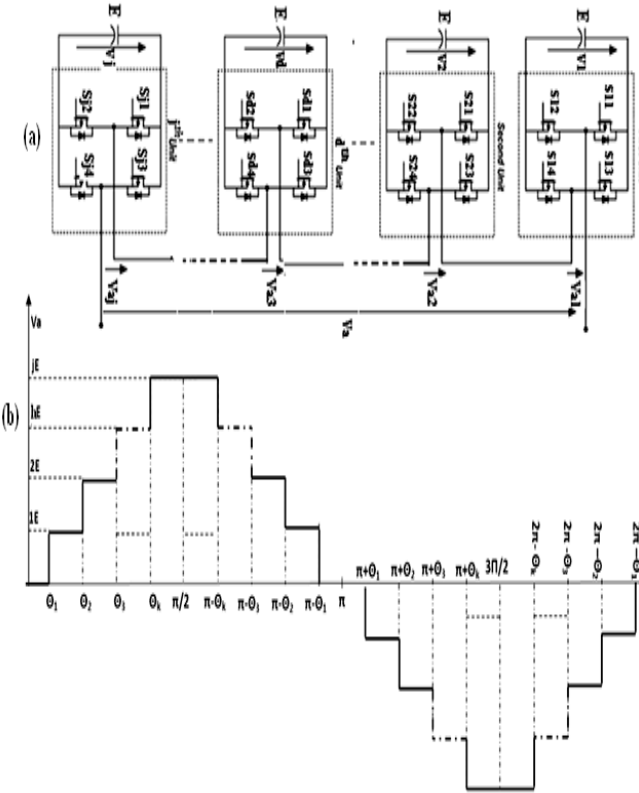


Fig.1: (a) Topology of a single-phase Cascade HB multilevel inverter. (b) Staircase CHB multilevel inverter output voltage.

### 3. Harmonic Elimination based on trust region dogleg analysis

In this section staircase voltage waveform as shown in figure 1(b) is chosen for the select harmonic elimination (SHE) technique in multilevel inverters [5].

The number of switching angles in a quarter cycles is limited to  $k$  in the staircase voltage waveform. In this method, the number of harmonics that can be eliminated is limited to  $s-1$ , such as  $s$  is the number of half cycle levels and  $E$  is the amplitude of the voltage levels.

By using Fourier series the staircase output of multilevel inverter with equal input sources is described in equation.(2).

$$V_a(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} H_n(\theta) \sin(n\omega t) \quad (2)$$

Where,  $H_n$  is the amplitude of the harmonics.

The switching angles  $\theta_1 \dots \theta_k$  must satisfy the following condition

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \dots \theta_k \leq \frac{\pi}{2} \quad (3)$$

Because of an odd quarter-wave symmetric characteristic, the harmonics with an even order become zero. Subsequently,  $H_n$  becomes

$$H_n(\theta) = \frac{4E}{n\pi} \sum_{k=1}^{s-1} \cos(n\theta_k) ; \text{ For all odd } n \quad (4)$$

$$H_n(\theta) = 0 ; \text{ For all even } n \quad (5)$$

The system of equations to be solved contains  $k$  nonlinear equations and is represented by the following.

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \dots \cos(\theta_k) = \frac{sM\pi}{4} \\ \cos(5\theta_1) + \cos(5\theta_2) + \dots \cos(5\theta_k) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \dots \cos(7\theta_k) = 0 \\ \vdots \\ \cos(n\theta_1) + \cos(n\theta_2) + \dots \cos(n\theta_k) = 0 \end{cases} \quad (6)$$

The objective is to find the switching angles to force the component odd harmonics to zero while keeping the relative fundamental component at a desired follow

$$H_1 = \frac{V_{a,1}}{E} \quad (7)$$

Where  $V_{a,1}$  is the magnitude of fundamental frequency of given voltage

And  $M$  is the modulation index defined as:

$$M = \frac{V_{a,1}}{sE} ; V_1 = V_2 = \dots = V_j = E \quad (8)$$

Switching angles are calculated with the help of MATLAB program using trust region dogleg algorithm for a range of modulation indexes. The flowchart of the dogleg trust region algorithm is shown in Figure 2

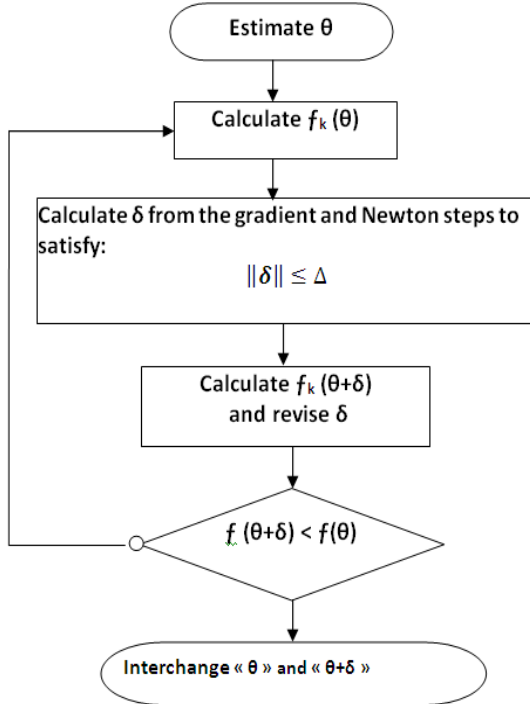


Fig.2. Trust Region Dogleg algorithm flow chart for calculate switching angles

Angles are calculated using equation (4) which must be satisfied.

$\theta$  is an array containing initial guess for:  $\theta_1 + \theta_2 + \theta_3 + \dots + \theta_k$

Where,  $\delta$  is the correction step,  $\Delta$  is the trust region radius, and  $f(\theta) = \sum_{i=1}^k [f_i(\theta)]^2$  is the sum of squares of residuals.

As shown in Figure 2, the first step of iteration is to find a correction  $\delta$  to be applied to the approximation  $\theta$ . This correction is a combination of the Newton direction and the steepest descent direction. This retains the fast convergence of the Newton's method, and assures getting a stationary point of  $F(\theta)$  by the steepest descent direction [14-16].

- If  $\Delta$  is large, the correction  $\delta$  is the Newton step only.
- If  $\Delta$  is small, the correction  $\delta$  is a multiple of the steepest descent step only.

The second step is to revise  $\Delta$  in order to determine the step-length for the new iteration to be successful in obtaining the inequality  $F(\theta+\delta) < F(\theta)$  [19,20]. The trust region radius can be increased or decreased. The third step is to check if the correction  $\delta$  has decreased the function values. If yes, replace  $\theta$  by  $\theta+\delta$  (fourth step). If not, repeat the iteration with the new smaller value of  $\Delta$ .

#### 4. Programmed Matrix PWM Algorithm For CHB Five Levels Inverter Control

In this section, a cascaded multilevel inverter with only two H-bridge cells is considered. For a two-cell inverter ( $n=2$ ), effective number of output voltage levels  $s$  is equal to 3 ( $s=3$ ) and the number of the switching angles to be calculated is equal to  $s-1=2$ , ( $\theta_1$  and  $\theta_2$ ). In fact  $\theta_1$  and  $\theta_2$  correspond respectively to the 5<sup>th</sup> and 7<sup>th</sup> harmonic that must be eliminated. As result, output voltage  $V_{a1}$  is either  $-V_1$ , 0, or  $+V_1$  while the output voltage of second HB cell (HB2), can be either  $-V_2$ , 0, or  $+V_2$ . Accordingly, the output voltage of the converter in different cases is shown in figure 3.

However, we demonstrate in this section that only the first cell needs to be supplied by a real dc power source and the remaining cell can be supplied with capacitor replacing its dc source [1, 15]. In this case the entire power can be supplied by only the first source. The replacing capacitor must only maintain a constant dc voltage supplying zero net power. Although this approach benefits from cost reduction and balancing the voltage across the replacing capacitor turns out to be a challenge [15]. Voltage regulation of the replacing capacitor is a key issue for the quality of the CHB multilevel inverter output voltage wave form [9, 11].

In this section, the impacts of the connected load to the cascaded H-bridge inverter as well as the switching angles on the voltage regulation of the capacitor are studied. This study proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported

Moreover, dead time has a huge impact on the quality of the CHB output voltage waveform. THD increase when dead time is introduced in complementary commutation cells control signals. Mainly in low frequency, when dead time increase THD increase and this is verified experimentally in section 6.

As shown in figure 3, CHB five levels inverter commutation cells control signals and switching angles are programmed in a matrix form. Based on redundant states, we select the appropriate switching angles for which we correspond the adequate CHB Five levels control signals. Control signals pattern choice is based on some requirements such as the desired CHB Five levels inverter output voltage, HB2 capacitor voltage balancing and dead time elimination.

In fact the objective of this section is to develop a programmed matrix PWM (PMPWM) which allows to:

- Replace HB2 DC voltage ( $V_2$ ) with a capacitor and provide voltage regulation across its voltage, in this regard a technique to regulate the voltage of the replacing capacitor is described below.
- Eliminate the 5<sup>th</sup> and 7<sup>th</sup> harmonics
- Avoid the dead time insertion in complementary commutation cells control
- Obtain the desired multilevel inverter output voltage

As it can be observed from figure 3, if  $V_1=V_2=E$ ,

the output voltage has five (5) levels. The output voltage level at  $E$  can be generated in one way, to choose  $V_{a1}=V_1=E$  and  $V_{a2}=0$ . In this case,  $V_2$  will be charged for positive output currents. The second way is to choose  $V_{a1}=0$  and  $V_{a2}=E$ . In this case,  $V_2$  will be discharged for positive output currents. As result we must choose the first way in which the capacity voltage will be charged.

A similar argument can be made when the desired output voltage is  $-E$ . In this case, we must choose  $V_1=0$  and  $V_2=-E$  in which  $V_2$  will be charged for negative output currents. Therefore, the output voltage will have five levels as illustrated in figure 3.

To balance HB2 capacitor voltage, redundant states are used to select the appropriate switching angels  $\theta_1$  and  $\theta_2$  which will be described here and must satisfy the following condition.

$$(0 < \theta_1 < \theta_2 < \pi/2) \quad (9)$$

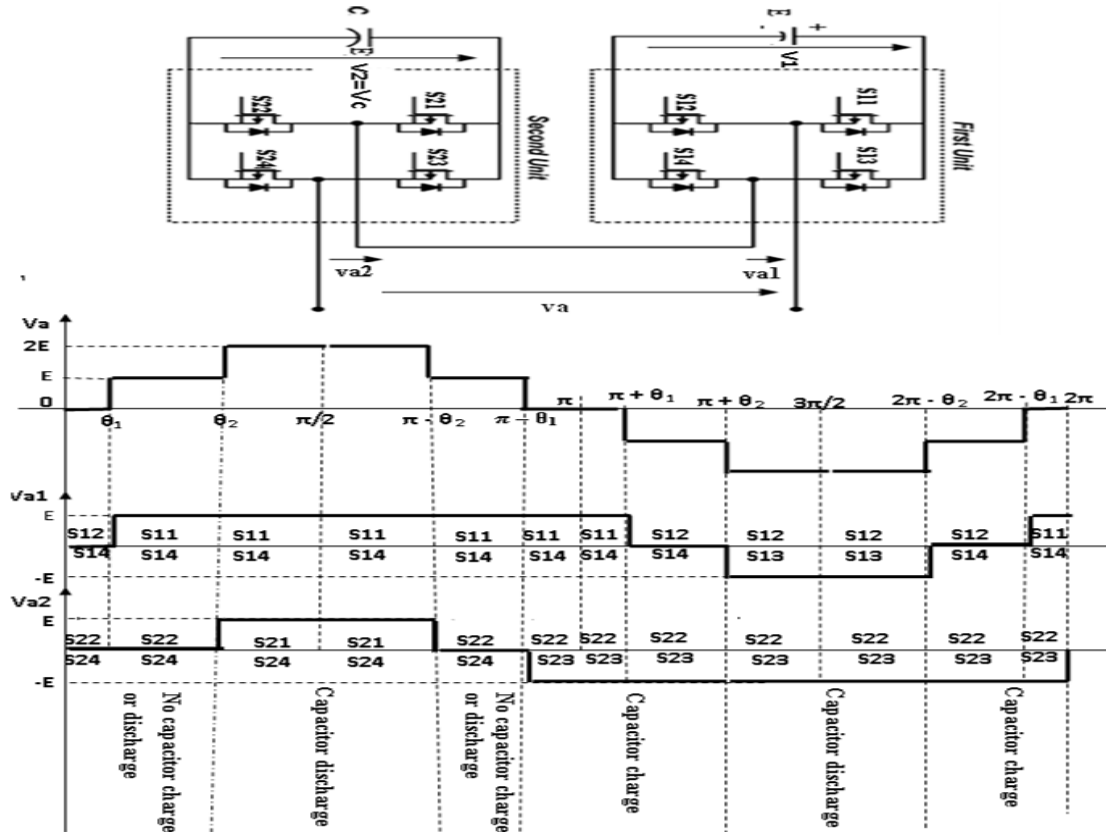


Fig 3: Programmed Matrix PWM for a single phase HB five levels inverter

Based on Figure3, the period can be divided into the following subintervals

Interval	HB 2 capacitor voltage state
I: $0 < \omega t < \theta_1$	no capacitor charge or discharge
II: $\theta_1 < \omega t < \theta_2$	no capacitor charge or discharge
III: $\theta_2 < \omega t < \pi - \theta_2$	capacitor discharge
IV: $\pi - \theta_2 < \omega t < \pi - \theta_1$	no capacitor charge or discharge
V: $\pi - \theta_1 < \omega t < \pi + \theta_1$	capacitor charge
VI: $\pi + \theta_1 < \omega t < \pi + \theta_2$	capacitor charge
VII: $\pi + \theta_2 < \omega t < 2\pi - \theta_2$	capacitor discharge
VIII: $2\pi - \theta_2 < \omega t < 2\pi - \theta_1$	capacitor charge
IX: $2\pi - \theta_1 < \omega t < 2\pi$	capacitor charge

Table1. HB2 capacitor voltage states

In order to achieve capacitor voltage regulation, the capacitor discharge in subintervals III and VII must be less than the capacitor charge in subintervals V, VI, VIII and IX.

In subintervals I and II capacitor is not involved and obviously  $V_C(\theta_1) = V_C(\theta_2) = V_C = E$ .

Assuming that the initial voltage of the capacitor is  $E$ , we can express the capacitor voltage in subinterval III as:

$$V_C(\omega t) = E - E e^{-\frac{\omega t - \theta_2}{\omega \tau}} \quad (10)$$

$T_3$  is the duration of subinterval III. In this case the capacitor voltage has decreased by:

$$\Delta V_C(T_3) = V_C(\theta_2) - V_C(\pi - \theta_2) = E e^{-\frac{\pi - 2\theta_2}{\omega \tau}} \quad (11)$$

In subinterval IV where  $T_4$  is the duration of this subinterval, capacitor is not involved and obviously

$V_C(\pi - \theta_2) = V_C(\pi - \theta_1)$ . For the fourth subinterval, we can write.

$$\Delta V_C(T_4) = V_C(\pi - \theta_2) - V_C(\pi - \theta_1) = 0 \quad (12)$$

For the fifth subinterval where  $T_5$  represents its duration, capacitor charges and its voltage has increased by:

$$\Delta V_C(T_5) = V_C(\pi + \theta_1) - V_C(\pi - \theta_1) \quad (13)$$

$$\Delta V_C(T_5) = E(e^{-\frac{\pi - 2\theta_2 + 2\theta_1}{\omega \tau}} - e^{-\frac{2\theta_1}{\omega \tau}}) \quad (14)$$

$T_6$  is the duration of subinterval VI where capacitor charge, and its voltage has increased by

$$\Delta V_C(T_6) = V_C(\pi + \theta_2) - V_C(\pi + \theta_1) \quad (15)$$

$$= E(-e^{-\frac{\theta_2 - \theta_1}{\omega \tau}} + e^{-\frac{\theta_1 + \theta_2}{\omega \tau}} + e^{-\frac{\pi - \theta_1 - \theta_2}{\omega \tau}} - e^{-\frac{\pi - \theta_2 + \theta_1}{\omega \tau}}) \quad (16)$$

Concerning subinterval VII where  $T_7$  represents its duration, capacitor discharges and its voltage has decreased by:

$$\Delta V_C(T_7) = V_C(2\pi - \theta_2) - V_C(\pi + \theta_2) \quad (17)$$

Such as:

$$\Delta V_C(T_7) = E(e^{-\frac{\pi - 2\theta_2 - 2\theta_1}{\omega \tau}} + e^{-\frac{2\pi - 4\theta_2}{\omega \tau}} + e^{-\frac{2\pi - 3\theta_2 + \theta_1}{\omega \tau}} - e^{-\frac{\pi - 2\theta_2}{\omega \tau}} - e^{-\frac{\pi - 3\theta_2 - \theta_1}{\omega \tau}} - e^{-\frac{2\pi - 4\theta_2 + 2\theta_1}{\omega \tau}}) \quad (18)$$

During subinterval VIII, where  $T_8$  represents its duration. Capacitor voltage has increased by:

$$\Delta V_C(T_8) = V_C(2\pi - \theta_2) - V_C(\pi + \theta_2) \quad (19)$$

Such as:

$$\Delta V_C(T_8) = E(1 + e^{-\frac{2\theta_1}{\omega\tau}} + e^{-\frac{\theta_2-\theta_1}{\omega\tau}} - e^{-\frac{\theta_2+\theta_1}{\omega\tau}} + 2e^{-\frac{\pi-2\theta_2}{\omega\tau}} - 2e^{-\frac{\pi-\theta_2-\theta_1}{\omega\tau}} - 2e^{-\frac{\pi+2\theta_1-2\theta_2}{\omega\tau}} + 2e^{-\frac{\pi-\theta_2+\theta_1}{\omega\tau}} - e^{-\frac{2\pi-4\theta_2}{\omega\tau}} + e^{-\frac{2\pi-3\theta_2-\theta_1}{\omega\tau}} + e^{-\frac{2\pi-4\theta_2+2\theta_1}{\omega\tau}} - e^{-\frac{2\pi-4\theta_2+\theta_1}{\omega\tau}})e^{-\frac{\theta_2-\theta_1}{\omega\tau}} \quad (20)$$

$T_9$  is the duration of this subinterval IX. The capacitor voltage has increased by:

$$\Delta V_C(T_9) = V_C(2\pi) - V_C(2\pi - \theta_2) \quad (21)$$

Such as:

$$\Delta V_C(T_9) = E(1 - e^{-\frac{2\theta_2}{\omega\tau}} - e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + e^{-\frac{\theta_2+\theta_1}{\omega\tau}} - 2e^{-\frac{\pi-2\theta_2}{\omega\tau}} + 2e^{-\frac{\pi-\theta_2-\theta_1}{\omega\tau}} + 2e^{-\frac{\pi+2\theta_1-2\theta_2}{\omega\tau}} - 2e^{-\frac{\pi+\theta_1-\theta_2}{\omega\tau}} + e^{-\frac{2\pi-4\theta_2}{\omega\tau}} - e^{-\frac{2\pi-3\theta_2-\theta_1}{\omega\tau}} - e^{-\frac{2\pi-4\theta_2+2\theta_1}{\omega\tau}} + e^{-\frac{2\pi-4\theta_2+\theta_1}{\omega\tau}})(e^{-\frac{\theta_2-\theta_1}{\omega\tau}} - e^{-\frac{\theta_1}{\omega\tau}}) \quad (22)$$

For successful capacitor voltage regulation, we need to have:

$$|\Delta V_C(T_3)| + |\Delta V_C(T_7)| \leq |\Delta V_C(T_5)| + |\Delta V_C(T_6)| + |\Delta V_C(T_8)| + |\Delta V_C(T_9)| \quad (23)$$

After simplification, the constraint on the switching angles that must be satisfied can be described as follow:

$$1 - e^{-\frac{2\theta_1}{\omega\tau}} + e^{-\frac{\pi+2\theta_1-2\theta_2}{\omega\tau}} - e^{-\frac{\pi-\theta_2+\theta_1}{\omega\tau}} + e^{-\frac{\pi-2\theta_2}{\omega\tau}} + e^{-\frac{2\pi-3\theta_2+\theta_1}{\omega\tau}} - e^{-\frac{\theta_2-\theta_1}{\omega\tau}} - e^{-\frac{\pi-\theta_2+\theta_1}{\omega\tau}} + e^{-\frac{\pi-3\theta_2-\theta_1}{\omega\tau}} \geq 0 \quad (24)$$

Since the capacitor for the auxiliary inverter (HB2) is chosen to be a big capacitor, we can make some assumption to simplify equation and achieve a simpler formula. If we assume that time of each subinterval of the output voltage waveform is less  $\tau = R \cdot C$  by expansion of exponential terms of the equation (24) and using only two first term of the series, equation (24) can be simplified as

$$3\theta_2 - 5\theta_1 > \frac{3\pi}{7} \quad (25)$$

Based on trust-region to calculate the switching angle to eliminate 5<sup>th</sup> and 7<sup>th</sup> harmonics, we represent in figure 4 the switching angles  $\theta_1$  and  $\theta_2$ , versus the modulation index M. Based on this graphic we must choose the index modulations which verify the relation (25) to obtain CHB 5 levels inverter with a balanced capacitor voltage

and in the same time to eliminate the 5<sup>th</sup> and 7<sup>th</sup> harmonics.

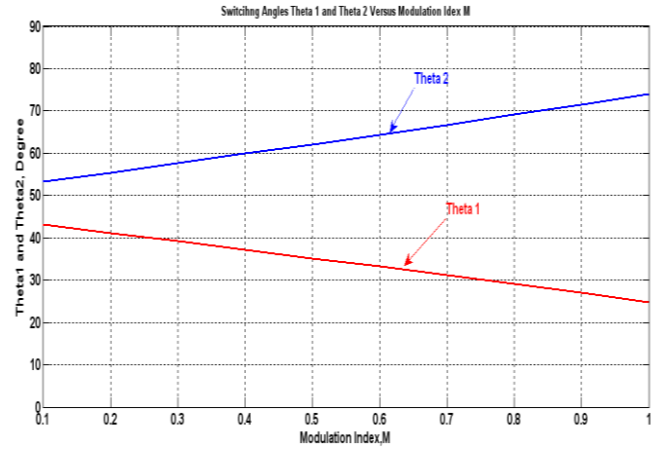


Fig.4. Switching angles  $\theta_1$  and  $\theta_2$  versus modulation index M based on Trust Region Dogleg method

Figure 4, shows that relation (25) is verified and HB2 capacitor voltage is balanced, only for  $M \in [0.88 \ 1]$ .

## 5. Simulation Results

Based on MATLAB-Simulink, single phase five levels inverter is used to drive a resistive load ( $R=50\Omega$ ) such as the first HB inverter unit (HB1) DC source voltage = 20V, HB2 capacitor voltage =20V with a capacity value  $C=150\mu f$ .

In case modulation index  $M$  is desired to be 0.9 the switching angles should be  $\theta_1=27.001^\circ$  and  $\theta_2=73.650^\circ$ .

Based on simulation result of figure 5, HB2 capacitor voltage is balanced, and the predictions of (24) and (25) on capacitor voltage regulation agree with the simulation result.

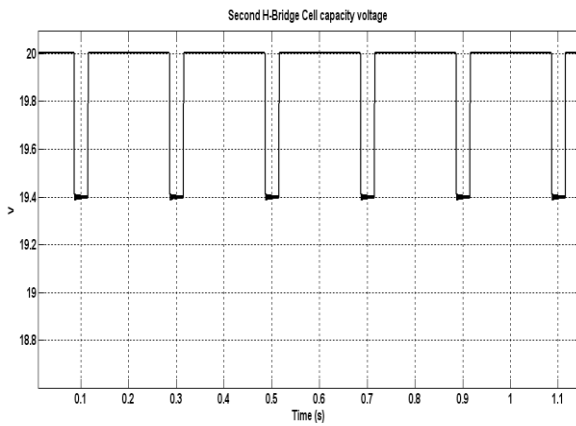


Fig.5.Simulation result of the HB2 capacitor voltage evolution

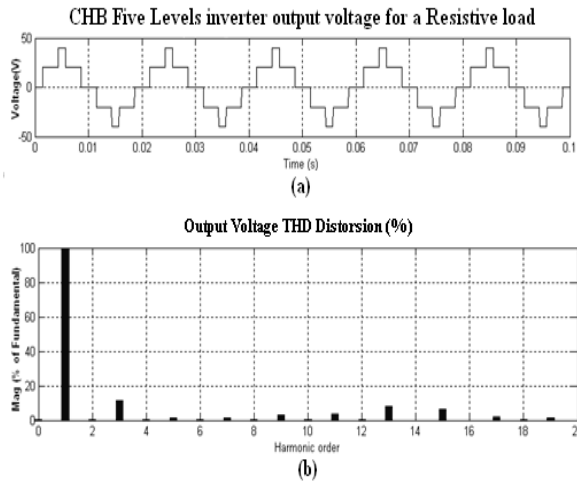


Fig.6. (a) CHB five levels inverter output voltage, (b) Output voltage THD distortion (%)

Simulation results for the replacing capacitor voltage and output voltage waveform are depicted in Figure 5 and figure 6(a), respectively. As it can be observed from the simulation results of figure 6(a), the regulation of the capacitor voltage is feasible if  $\theta_2$  is very close to  $\pi/2$ .

Figure 6(a), and 6(b), show that for  $M=0.9$ ,  $\theta_1=27.001^\circ$  and  $\theta_2=73.650^\circ$ , the desired CHB five level inverter output voltage is obtained, and the 5<sup>th</sup> and 7<sup>th</sup> are eliminated.

## 6. Hardware realization and experimental results

A low-power five-level CHB inverter prototype has been developed to verify the feasibility of the proposed strategy and confirm the validity of the simulation and theoretical findings. The prototype inverter is based on two-cell CHB units by using the 800V, 7.8A MOSFET (IRFPE50) as switching devices. CHB five levels inverter is used to drive a resistive load ( $R=50\Omega$ ) with HB1 DC source voltage = 20V and HB2 capacitor voltage =20V with capacitor value  $C=150\mu f$ . Output voltage frequency:  $f=50$  Hz. Modulation index is chosen to be  $M=0.9$  where the switching angles  $\theta_1=27.001^\circ$  and  $\theta_2=73.650^\circ$ .

The programmed matrix PWM binary file (. bin file) is loaded in a Programmable EPROM, used to generate the required PWM waveform control signals after storing the required switching angles(degree values), obtained in the previous section and converting them into time domain. A binary counter to convert switching angles from degree values into time domain ( $\mu s$ ) as shown in figure 7. The Less Significant Bytes (LSB) ( $A_0...A_7$ ) of EPROM address bus are used as base of time for programmed matrix PWM. Base of time is generated by an 8 bits counter.

Most Significant Bytes (MSB) of the address bus ( $A_8.. A_{15}$ ) are used for CHB Five inverter control signals.

As shown in figure.7, the 8 control signals of the CHB five levels inverter commutation cells are generated at the output data bus of the EPROM ( $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8$ ).

Figure 8 shows the realized experimental set-up to test the programmed matrix implemented into EPROMs to control the five levels CHB inverter.



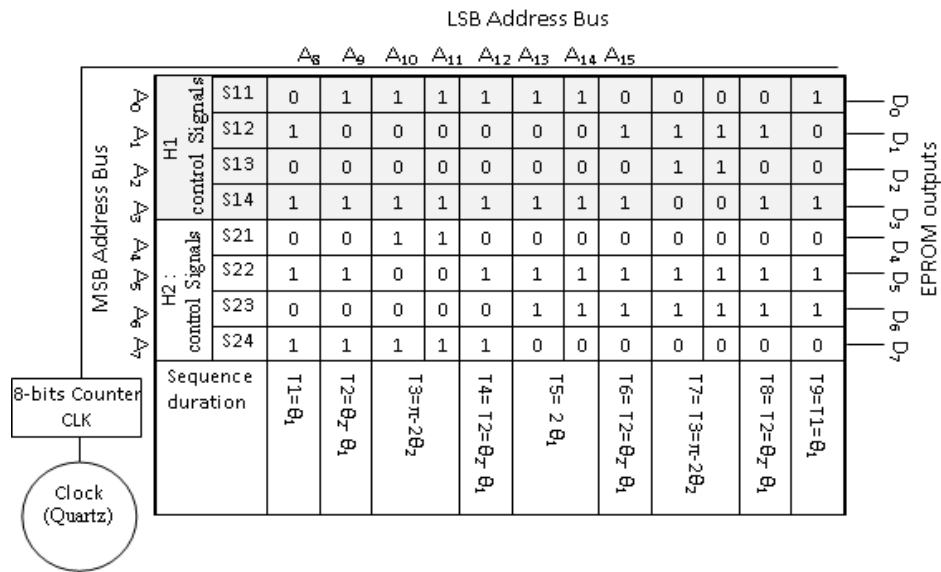


Fig.7. Programmed Matrix PWM synoptic for single phase CHB 5 levels inverter

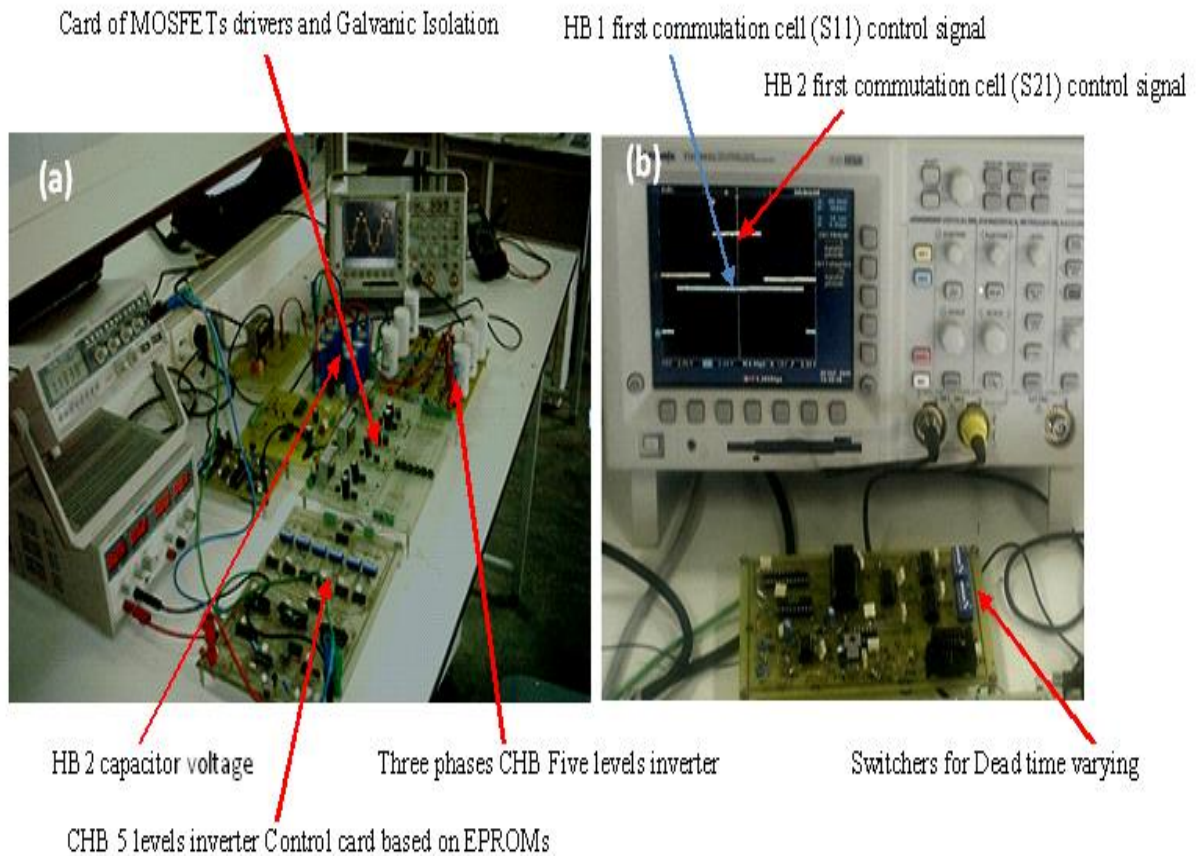


Fig.8. (a) Photograph of the Experimental Prototype of the PMPWM for CHB five levels inverter control  
(b) Control signals of the first commutations cells of HB1 and HB2 respectively

Figure 9 shows the experimental HB2 capacitor voltage. It is clear that HB2 capacitor voltage is balanced and it evolves to its target operating voltage. This result confirms that the programmed matrix PWM modulator guarantees the HB2 capacitor voltage balance.

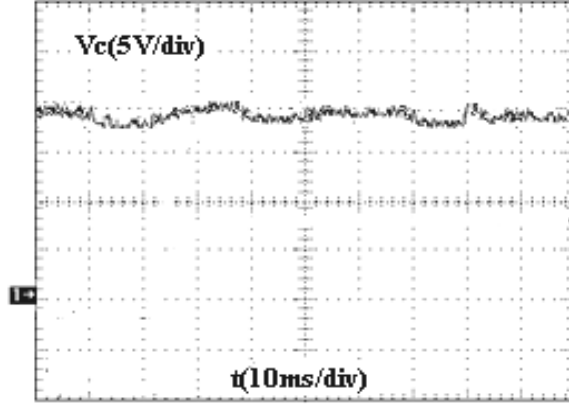


Fig.9. Experimental result of HB2 capacitor voltage

The experimental result of the per phase five levels CHB inverter is given by figure 10 and figure 11. We can clearly see in figure 10 that the output voltage is formed by  $m=5$  distinct voltage levels.

Figure 11, shows that for  $M=0.9$ ,  $\theta_1=27.001^\circ$  and  $\theta_2=73.650^\circ$  and for the desired CHB five level inverter output voltage the 5<sup>th</sup> and 7<sup>th</sup> are eliminated. In fact experimental results confirm the high performances of the embedded Programmed Matrix PWM control of this inverter.

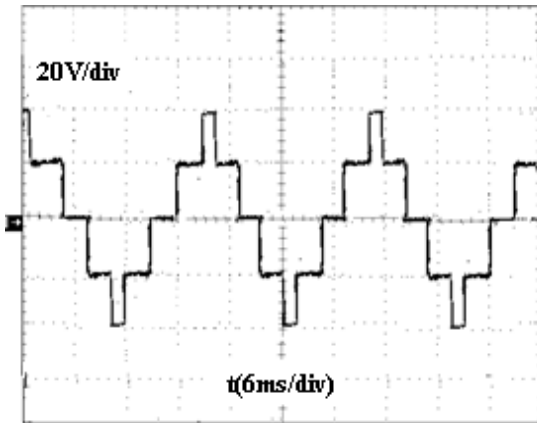


Fig.10.Experimental result of the single phase CHB five levels inverter output voltage waveform

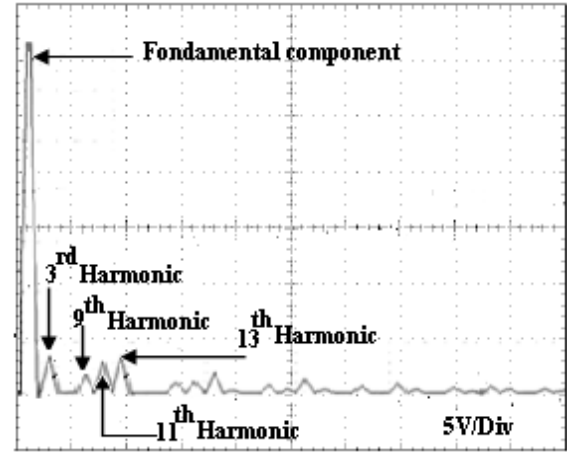


Fig.11.FFT analysis of the experimental output voltage

The comparison of hardware results with the simulation results is shown in figure 12. From this figure, it is concluded that for the modulation indices ranging from 0.88 to 0.98 when HB 2 capacitor voltage balancing condition is verified, both hardware and simulation results are very close and almost they agree each other.

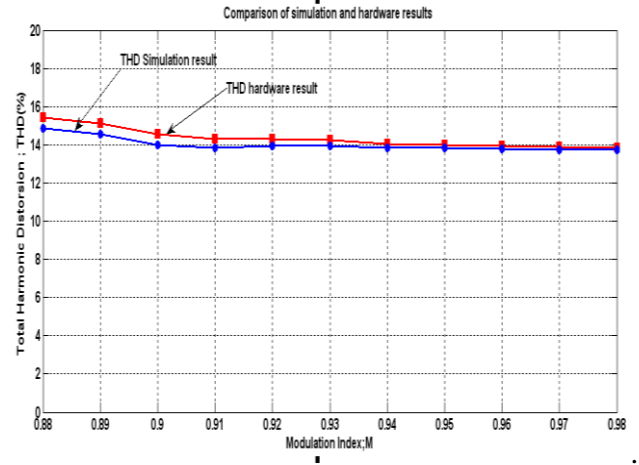


Fig.12.Comparison of simulation and hardware results

In experimental section, switchers are used for varying dead time. It is introduced in complementary commutation cells control signals for one unit H-Bridge cell. As results, figure 13, shows that when dead time increase THD increase. This illustrates the huge impact of dead time on the quality of the cascade multilevel inverter output voltage.

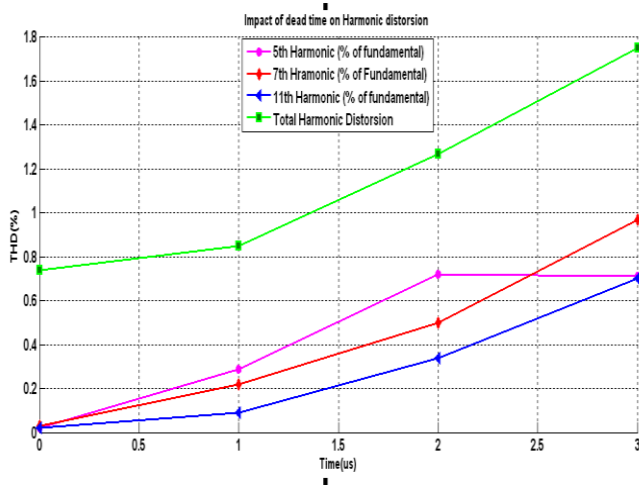


Fig.13. Dead time impact on harmonic distortion

## 7. Conclusion

The single-dc-source cascaded H-bridge inverter was investigated in this paper. Trust-region dogleg technique has been used to obtain the optimum switching angles. A programmed matrix PWM based on trust region dogleg is developed to control CHB Five levels inverter.

A prototype model based on this Novel technical for cascaded five levels inverter control is implemented to validate the simulation results. The comparison of hardware results with the simulation results discloses that hardware results closely agree with that of simulation

In this paper Programmed matrix PWM objectives are achieved and it allows eliminating the 5th and 7th harmonic of the output voltage, balancing the HB2 capacitor voltage and avoiding dead time insertion in complementary commutation cells control signals.

## References

1. Lin, B.R.: High power factor ac/dc/ac converter with H-bridge cascade five-level PWM inverter. *European Transactions on Electrical Power* Vol 11,pp. 97-106, 2001
2. Lazhar, M., Faouzi B.A., : Control of a Four Levels Inverter by a Programmed Matrix PWM based on EPROMS. *International Review of Electrical Engineering*; Vol 4,pp.1189-1197, 2009.
3. Mehrdad, T.H., Hassan T., Kaveh, R.: Harmonic Minimization in Multilevel Inverters Using Modified Species-Based Particle Swarm Optimization. *IEEE Transactions On Power Electronics* Vol 24,pp.: 2259-2267, 2009
4. Mehrdad, T.H., Hassan, T: Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization. *IEEE Transactions On Power Electronics*. Vol 57,pp. 3678-3684, 2010
5. Ke S, Dan Z, Jun M, Leon M-T, Jianze W, Mingfei B, Yanchao J, Xingguo C. Elimination of Harmonics in a Modular Multilevel Converter Using Particle Swarm Optimization-Based Staircase Modulation Strategy. *IEEE Transactions On Industrial Electronics*, Vol 61,pp.5311-5322, 2014,
6. Albert, A.S., Manigandan, T. : Optimal Harmonic Stepped Waveform Technique for Solar Fed Cascaded Multilevel Inverter. *JEET*,pp. 742-751, 2015
7. Koutroulis, E., Dollas, A.: Development of an FPGA-Based SPWM Generator for High Switching Frequency DC/AC Inverters. *IEEE Transactions On Power Electronics*.Vol 29, pp. 356 – 365, 2014
8. Shengfang, F., Kai, Z., Jian, X ., Yaosuo, X.:An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control. *IEEE Transactions on Power Electronics*, Vol 30, pp. 358 – 371, 2014
9. Jingsheng, L: Integration of energy storage components with cascaded H-bridge multilevel converters. doctorate of philosophy, Curtis law Wilson Library,pp 1:81, 2009
10. Joshi M.V, Sujatha, P., Seetha R.A.K: Harmonic analysis and FPGA implementation of SHE controlled three phase CHB 11-level inverter in MV drives using deterministic and stochastic optimization techniques. *Springer plus*,pp. 2:370, 2013
11. Verma,V.,Kumar,A.: Single phase cascaded multilevel photovoltaic sources for power balanced operation. *IEEE International Conference on Power Electronics (IICPE)*, pp.1 – 6, 2012,
12. Tariq Kl., Syed Z.H., Syeda Z.N.: Imranullah . Development of Improved Diode Clamped Multilevel Inverter Using Optimized Selective Harmonic Elimination Technique. *Emerging Trends in Electrical, Electronics & Instrumentation Engineering*,Vol 1 pp:17-28, 2014
13. Amin G., Hossein M., Mohsen F., : Simple Voltage Balancing Approach for CHB Multilevel Inverter Considering Low Harmonic Content Based on a Hybrid Optimal Modulation Strategy. *IEEE Transaction on power Delivery*. Vol 27,pp. 2150-2158, 2012
14. Janjamraj N., Oonsivilai A.: Harmonic Elimination of Hybrid Multilevel Inverters Using Particle Swarm Optimization. *World Academy of Science, Engineering and Technology*, Vol 6, pp. 1340-1345, 2012

15. Farid K., Mouna S. L., Abdelaziz K., Mohamed El H. B.: Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives. *IEEE Transactions On Energy Conversion*, Vol 26, pp.64-72, 2011
16. Rech, C., Pinheiro, J. R.: Impact of hybrid multilevel modulation strategies on input and output harmonic performance. *IEEE Transaction on Power Electronics*. Vol 22, pp. 967–977, 2007
17. Mei J., Xiao,K., Shen B., Tolbert B.M., Zheng J : A new selective loop bias mapping phase disposition PWM with dynamic voltage balance capability for modular multilevel converter,” *IEEE Transactions on Industrial. Electronics*. Vol 61, pp.798–807, 2014
18. Waltz R. A., Morales J. L., Nocedal J., Orban D.: An interior algorithm for nonlinear optimization that combines line search and trust region steps. *Math. Programming*, Vol 107, pp.391-408, , 2006,
19. NIM G., Orban D., Sartenaer,A., Toint., P.L: Sensitivity of trust-region algorithms to their parameters. Vol 35, pp. 227-241, 2005
20. Jorge N, Figen O, Richard A.W: An Interior Point Method for Nonlinear Programming with Infeasibility Detection Capabilities. *Mathematics Subject Classification*, pp.1-30, 2000
21. Conn,A., Gould, N., Orban, D., & Toint., P.L . Primal-dual trust-region algorithm for non-convex nonlinear programming. *Mathematical Programming*, pp. 215-249, 2000