COMPARATIVE PERFORMANCE ANALYSIS OF PV BASED GRID-TIED SINGLE PHASE ASYMMETRICAL MULTILEVEL INVERTER USING DIFFERENT PWM TECHNIQUES

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Abstract: *This paper is based on the comprehensive performance analysis of single phase grid-tied photo voltaic system with asymmetric configuration of cascaded H-bridge Multi-level Inverter. The work has been carried out for both the Level shifted pulse width modulation and the phase shifted pulse width modulation techniques. For extracting maximum power from photo voltaic source P&O based Maximum power point tracking algorithm is implemented with a control scheme which provides independent control of each DC link voltage. The comparative performance analysis of harmonics under different irradiation is also shown. Overall system performance is enhanced employing L-C-L filter. The proposed nine level inverter is based on transformer-less configuration that requires only two PV sources with lesser number of switches as compared to conventional Cascaded Multi-level Inverters. Modeling and simulation of the proposed model are implemented in MATLAB/Simulink environment.*

Key words: *Asymmetrical Multi-level, LCL Filter Inverter, Photo Voltaic (PV) cell, Total Harmonic distortion (THD).*

1. Introduction

In the present scenario, the fossil fuels are gradually decreasing thereby increasing the demand for non-conventional energy. Solar photovoltaic (PV) systems are most demanding as non-conventional energy supplies. The reasons for adopting PV system in large extent are its eco-friendly nature, zero pollution, no greenhouse gas emission, easy allocations in remote location or in roof top of houses [1][2]. Furthermore, solar energy system is gaining popularity because of its easy availability and different arrangements such as grid connected or standalone load. Grid connected system has the advantage of its efficient and easy utilization of PV power.

As the power demands are increasing, the demand for different types of modern and efficient power electronics converters is also rising. Multi-level inverter (MLI) is the latest power electronics converter device which allows smoother conversion of voltage in multiple levels with very less (Total harmonic distortion) THD level [3]. Moreover, these converters are capable of handling very high power and high voltage efficiently as compared to the other conventional two level inverters. Classical multi-level topologies have been categorized into the three types such as Neural point clamped multi-level inverter (NPC-MLI), Flying capacitor multilevel inverter (FC-MLI), Cascaded H-bridge multilevel inverter (CHB-MLI) topologies [4][5].

Asymmetrical multilevel inverter is a modification as well as advantageous to the existing cascaded H-bridge structure. First, the DC input to asymmetrical multilevel inverter cells is not symmetrical but scaled in some particular ratio [6].When compared to conventional multilevel inverters (MLI), the switching losses can be minimized in asymmetrical multilevel inverters by using lesser no of semiconductor switch. Asymmetrical CHB-MLI can provide more number of output voltage levels simply with same number of circuit components as compared to classical cascaded MLI [7].

A single phase grid connected PV system with transformer has been proposed in [8]. This scheme focused on the control of individual DC link voltage for each PV module with acceptable amount of common mode leakage current in turns making system more complex as well as reduces the overall efficiency of the system. The drawback of high common mode leakage current for transformer-less grid connected PV system was achieved using a suitable switching strategy was discussed in [9].

The non-linear characteristics of PV cell create the difficulties to achieve the maximum power under normal operation. In PV cell, only 35-40 % of energy incident can be converted directly to the electrical energy. Thus, Maximum power point tracker (MPPT) is employed along with DC-DC converters to obtain the maximum operating point of power from the PV module. Perturb and observe (P&O) method for maximum power point tracking has been used to enhance the energy harvesting from each PV module [10-12], [13–15]. Multilevel Inverter with PV module is a better choice for the efficient power generation [16]. In Cascaded MLI, more than one DC link exists and several DC link provides chances for independent voltage control where it is also possible to track MPPT of different PV module which is advantageous under partial shading problem.

Several PWM modulation techniques are proposed in [18]–[19], [20], [21]–[22], [23-28], [29-32] for different configuration of MLI where carrier based Phase-Shifted PWM (PS-PWM) [19], [26], [22], Level-

Shifted PWM (LSPWM) [8], [12], [27] are generally used for MLI topologies. Space Vector PWM (SVPWM) [17], [30], [32], Selective Harmonic Elimination PWM (SHEPWM) [24] are gaining popularity now-a-days. Carrier based PWM techniques like Double-Reference PWM [18], [25] and Triple- Reference PWM techniques [26] are used for MLI grid tied inverter based on reduced switches.

Various types of closed-loop control techniques are used in [18-19], [27], [28], [20], [29], [13-15], [23-31] to achieve synchronization between MLI output current and voltage with grid current and voltage respectively. The linear Proportional Integral (PI) [18]-[19], [25], [28]-[33] method provides efficient operation for grid control.

In this paper, PI-based controller is designed for controlling the grid voltage and grid current thereby keeping the power factor nearly unity. A Generalized asymmetrical cascaded MLI for single phase PV based grid tied application has been studied that deals with the two control loops i.e. inner current control loop and outer voltage control loop. In this work both phase shifted and level shifted PWM techniques are used for comprehensive analysis of THD spectrum at different irradiance. Reference signal is chosen in such a way that so that it is in phase with grid voltage and grid current thus keeps the power factor close to unity. This paper proposes a suitable control strategy for single phase transformer- less grid connected PV configuration.

2. Overall System Topology

Block presentation of overall system is depicted in Fig. 1 where PV cell voltage is boosted up by a DC-DC boost converter and then fed to the load through multilevel inverter (MLI). MLI provide nearly smooth output voltage with less harmonic distortion thus meeting the requirements of load demand. A suitable filter is connected across the MLI for minimization of the ripple in the current as well as the voltage so to make it nearly sinusoidal. After fulfilling the load demand, the rest of the PV module power is utilized in the grid. The grid voltage and the grid current plays an important role as they are the main components for generating the carrier based SPWM pulses in accordance with the reference voltage and fed to the MLI semi-power conductor switches. The controller compares the dc link voltages of respective PV module with the grid voltage and the grid current. The dark arrow shows the direction of power flow from PV cell to the grid side and the dotted arrow. When the PV cell power generated being less than the grid, power will flow from the grid to the load as shown in Fig.1.

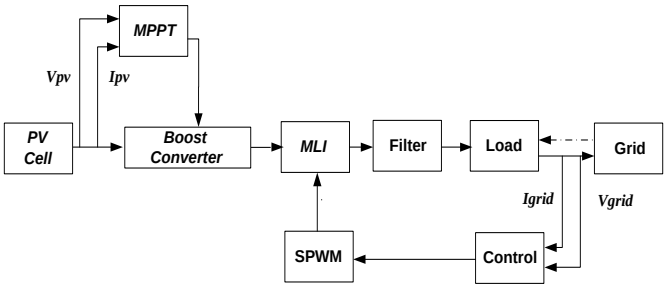

Fig.1. Block presentation of overall system topology.

2.1. Generalized n-Level Cascaded Multilevel Inverter Topology

Cascaded H-bridge multilevel inverter (CHB-MLI) is employed among the other classical configurations such as Flying capacitor (FC-MLI) or Neutral point clamp (NPC-MLI) as it provides very simple structure for generation of stepped output voltage. CHB-MLI also has inherent self-voltage balancing capability and does not suffer through dc link voltage unbalance where each bridge acts as a single module that can be operated independently. The generalized cascaded H-bridge single phase N-level multilevel inverter (CHB-MLI) for grid-tied system is shown in Fig. 2. Number of H-bridges denoted by 'n' connected in cascaded manner having equal DC link voltage for each H-bridge structure where 'N' is the output phase voltage levels for the single phase inverter having (2N+1) number of line voltage levels at the output.

2.2. Cascaded Asymmetrical Multilevel Inverter grid-tied System

In this configuration, DC link voltage in all the H-bridges is arranged in some particular ratio. Each PV module output voltage is different i.e. m_1V_{dc}, m_2V_{dc}, …, m_nV_{dc} for asymmetrical N-Level CHB-MLI whereas for conventional CHB-MLI or symmetrical N-Level CHB-MLI have equal DC link voltages i.e. $m_1V_{dc}= m_2V_{dc}=\ldots= m_nV_{dc}$. Asymmetrical N-Level CHB-MLI enables the more number of level as compared to the conventional cascaded MLI.

In this work, asymmetric CHB-MLI structure has been used to obtain nine level output phase voltages. The voltage at first H-bridge is $m_1=3$ and the second bridge voltage is $m_2=1$. Thus, the trinary voltage combination (3:1) generates the nine different levels of phase voltages. As the circuit for nine level asymmetrical MLI is same as the five level conventional MLI except the different DC link voltage ratio thereby reducing the number of components required as shown in Table 1.

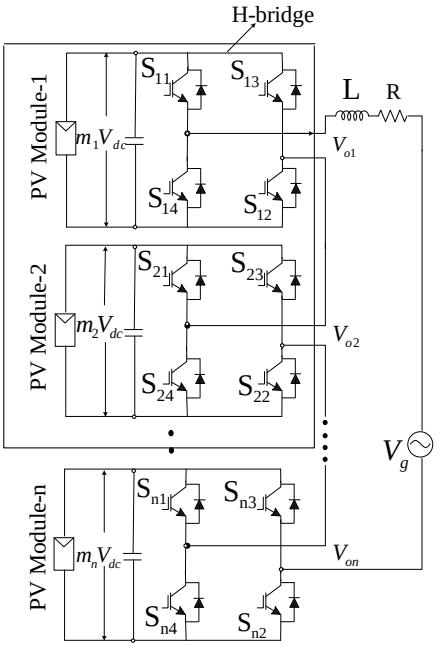

Fig. 2. Generalized single phase n-level cascaded H-bridge inverter (CHB) for the grid-tied system.

Table 1: Comparative analysis of components required for symmetrical and Asymmetrical CHB-MLI

Types of MLI	No. of levels	No of DC Link Capacitor	No of switches required	No. of voltage sources
Symmetrical	9	4	16	4
Asymmetrical	9	2	8	2

Table 2: Switching Sequences of Asymmetrical CHB-MLI

Voltage Levels	**Switching Pulses**							
	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}
+4V	1	1	0	0	1	1	0	0
+3V	1	1	0	0	1	0	1	0
+2V	1	1	0	0	0	0	1	1
+V	1	0	1	0	1	1	0	0
0	1	0	1	0	0	1	0	1
-V	1	0	1	0	0	0	1	1
-2V	0	0	1	1	1	1	0	0
-3V	0	0	1	1	0	1	0	1
-4V	0	0	1	1	0	0	1	1

The switching states of CHB-MLI remains the same for symmetrical CHB-MLI and for asymmetrical CHB-MLI as shown in Table 2. For generation of each output voltage level, one pair of switch from the upper H-bridge and the other pair of switch from the lower H-bridge is conducted.

When switch S_{11} and S_{12} is ON, voltage $+3V_{dc}$ starts flowing from the upper H-bridge and voltage $+V_{dc}$ generated from switches S_{21} and S_{22} of the lower H-bridge is summed with $+3V_{dc}$ that generates voltage $+4V_{dc}$ ($+3V_{dc}+V_{dc}$) through the load.

When switch S_{11} and S_{12} is ON, voltage $+3V_{dc}$ starts flowing from the upper H-bridge and voltage $+0V_{dc}$ generated from switches S_{21} and S_{23} of the lower H-bridge is summed with $+3V_{dc}$ that generates voltage $+3V_{dc}$ ($+3V_{dc}+0V_{dc}$) through the load.

When switch S_{11} and S_{12} is ON, voltage $+3V_{dc}$ starts flowing from the upper H-bridge and voltage $-V_{dc}$ generated from switches S_{23} and S_{24} of the lower H-bridge is summed with $+3V_{dc}$ that generates voltage $+2V_{dc}$ ($+3V_{dc}-V_{dc}$) through the load.

When switch S_{11} and S_{13} is ON, voltage $+0V_{dc}$ starts flowing from the upper H-bridge and voltage $+V_{dc}$ generated from switches S_{21} and S_{22} of the lower H-bridge is summed with $+0V_{dc}$ that generates voltage $+V_{dc}$ ($+0V_{dc}+V_{dc}$) through the load.

When switch S_{11} and S_{13} is ON, voltage $+0V_{dc}$ starts flowing from the upper H-bridge and voltage $+0V_{dc}$ generated from switches S_{22} and S_{24} of the lower H-bridge is summed with $+0V_{dc}$ that generates voltage $+0V_{dc}$ ($+0V_{dc}+0V_{dc}$) through the load.

When switch S_{11} and S_{13} is ON, voltage $+0V_{dc}$ starts flowing from the upper H-bridge and voltage $-V_{dc}$ generated from switches S_{23} and S_{24} of the lower H-bridge is summed with $+0V_{dc}$ that generates voltage $-V_{dc}$ ($+0V_{dc}-V_{dc}$) through the load.

When switch S_{13} and S_{14} is ON, voltage $-3V_{dc}$ starts flowing from the upper H-bridge and voltage $+V_{dc}$ generated from switches S_{21} and S_{22} of the lower H-bridge is summed with $-3V_{dc}$ that generates voltage $-2V_{dc}$ ($-3V_{dc}+V_{dc}$) through the load.

When switch S_{13} and S_{14} is ON, voltage $-3V_{dc}$ starts flowing from the upper H-bridge and voltage $+0V_{dc}$ generated from switches S_{22} and S_{24} of the lower H-bridge is summed with $-3V_{dc}$ that generates voltage $-3V_{dc}$ ($-3V_{dc}+0V_{dc}$) through the load.

When switch S_{13} and S_{14} is ON, voltage $-3V_{dc}$ starts flowing from the upper H-bridge and voltage $-V_{dc}$ generated from switches S_{23} and S_{24} of the lower H-bridge is summed with $-3V_{dc}$ that generates voltage $-4V_{dc}$ ($-3V_{dc}-V_{dc}$) through the load.

2.3. PV System with MPPT Controller

The circuit diagram PV cell is depicted in Fig. 3 where Iph represents the phase current and Id is the current through diode. Current provided by PV cell should be converted to dc voltage with a suitable capacitor. In case of PV cell, the two most important parameters are the open circuit voltage, Voc and the short circuit current, Isc and these parameters determines the actual ratings of PV cell. Rp and Rs are its parallel and series resistance which has a fixed value for a specific PV cell model. The value of other different constants which are used are listed in Table 3 [34-37].

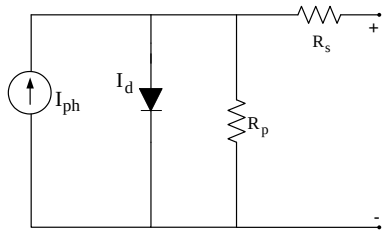

Fig.3. Circuit diagram of PV cell.

This paper deals with an asymmetrical CHB-MLI, so the number of series and parallel modules in two H-bridges are different as the DC Link voltages are of different ratio. For the first bridge number of series and parallel module are different than that of the second H-bridge. Number of module is chosen in such that the second H-bridge voltage provides approximately one third of the voltage of first H-bridge voltage.

The output of the PV system is non-linear. Also, when a PV array is directly connected to load, the impedance of the load dictates its operating conditions. To mitigate this problem, a maximum power point tracking (MPPT) technique is used to maintain the PV module's operating point at the maximum power point (MPP).A variety of maximum power point tracking methods are developed [38-40], which may vary with the implementation complexity, sensed parameters, required number of sensors, convergence speed and cost.

In this proposed work, perturb and observe (P&O) method is implemented because of its simple implementation, lesser time to track the MPP and several other economic reasons as well. In P&O algorithm, first V_{pv} and PV cell current I_{pv} is measured and the initial power P_i is calculated. Then a small perturbation is applied in duty pulse thus resulting changes in the PV cell voltage and PV cell current simultaneously. Again the power is calculated as P_m with the condition applied that whether the power is more than the previous value of power. Perturbation is said to be going in the right direction if the power calculated is being more than the previous value of power otherwise it is said to be perturb in the reverse direction. In this way, maximum power point is reached and corresponding maximum voltage is also obtained from the PV module.

Table 3: Parameter of PV module

Name	Parameters	Value
Boltzman Constant	K	$1.38*10^{-23}$
Series Resistance	R_s	0.18Ω
Parallel Resistance	R_p	360.002 Ω
Open circuit Voltage	V_{oc}	21.1 V
Short Circuit Current	I_{sc}	3.8 A
Short circuit current/temperature coefficient	K_i	$2.2*10^{-3}$
Irradiance	Λ	$1kW/m^2$
Electron charge	Q	$1.6*10^{-12}$
Band gap Energy	E_g	1.1eV
Ideality Factor	A	1.36
No of cell in a module	C	36

2.4. Sinusoidal Pulse Width Modulation Technique

SPWM techniques are the most reliable technique for generating PWM pulses. Bipolar PWM uses one carrier signal that is compared with the reference to decide between two different voltage levels. The multicarrier based PWM strategies i.e. Phase Shifted (PS) and Level Shifted (LS) PWM is the most common and popular technique for PWM control of cascade MLI.

Level shifted PWM depending on its carrier phase is classified into three category such as Phase Disposition PWM (PD-PWM), Phase Opposition Disposition PWM(POD-PWM) Alternate Phase Opposition Disposition PWM (APOD-PWM) whereas the phase shifted PWM (PS-PWM) as applied and are explained as follows:

Level Shifted PWM: All the triangular carrier signals are placed in a specific amplitude band, they all have equal amplitude but position of amplitude band is different, they can be in same phase or different phase [41].

a. **Alternate phase opposition disposition PWM (APOD-PWM):** All the triangle carrier signals are alternatively displaced by 180° or in phase opposition as shown in Fig. 4(a)
b. **Phase disposition PWM (PD-PWM):** All the carriers above zero level and below zero level in phase among them, shown in Fig. 4(b)
c. **Phase opposition disposition PWM (POD-PWM):** All the carrier above zero level are in phase whereas below zero level these carrier are in phase opposition to that of the carriers above the zero level as shown in Fig.4(c)
d. **Phase Shifted PWM:** In phase shifted

technique all carriers are shifted in phase rather than their level. In this method all the carrier are have same frequency and same peak amplitude but delayed by phase i.e. have different phase. Phase delay is given by $d=f_c/(n-1)$, where d is delay, 'n' is no of level and 'f_c' is the carrier frequency.

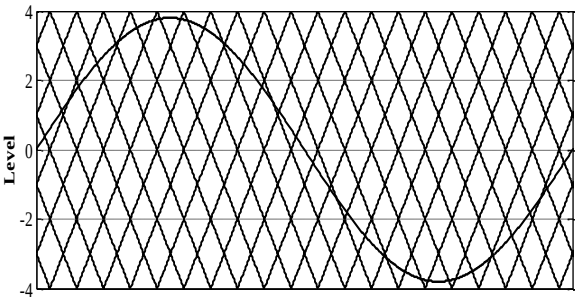

Fig. 4 (a). APOD-PWM Strategy.

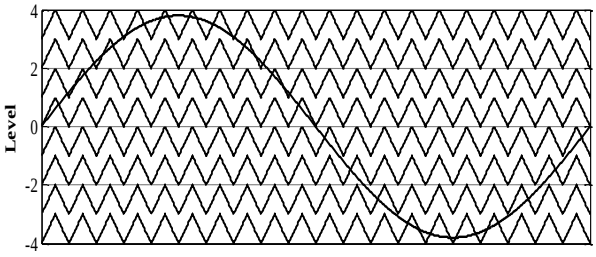

Fig. 4(b). PD-PWM Strategy.

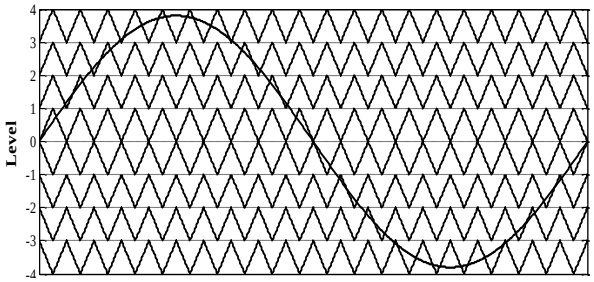

Fig. 4(c). POD-PWM Strategy.

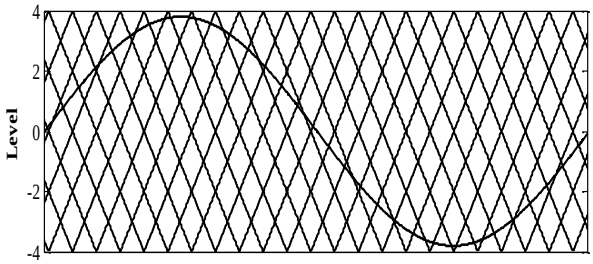

Fig. 4(d). PS-PWM Strategy.

3. L-C-L Filter

The output voltage and current of proposed CHB MLI must be filtered in order to reduce the ripples and to improve the quality of output voltage. L-C-L filter is thus used as shown in Fig 5. It have certain advantages over other filters [21,28,29], such as it has good performance over higher order harmonics and better dynamic response.

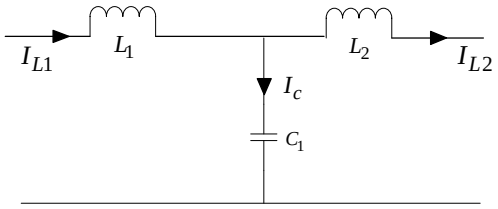

Fig. 5. L-C-L filter

For keeping the power factor nearly unity, a high value of filter inductance must be avoided but as the generated voltage is very large for this work so the inductor of higher rating is chosen to filter the ripples. The values of inverter side inductor L_1 and the grid side inductor L_2 chosen to be 40 mH and capacitor C chosen to be 22 µF. L-C-L filter connected grid current cannot be easily controlled, there is always chances of instability so it must have a suitable controller for synchronizing the proposed CHB-MLI output with the grid current as well as the grid voltage.

3. Controller for Closed Loop Design

In the outer voltage control loop, the DC link voltage of upper H-bridge i.e. V_C^1 ($3V_{dc}$) is added with the DC link voltage of lower H-bridge i.e. V_C^2 (V_{dc}) and compared with the suitable reference for a particular solar irradiance level where different reference voltage is generated corresponding to its irradiance level. Simulation is carried out for three different irradiance level (1000W/m^2, 800W/m^2, 600W/m^2) thus generating three different reference voltage for both the DC link and a look up table is designed for monitoring the change in irradiance level. Two PI controllers are required for independent control of DC link voltages of upper H-bridge i.e. V_C^1 ($3V_{dc}$) and lower H-bridge i.e. V_C^2 (V_{dc}). Total DC link voltage, $V_C^3 = V_C^1 + V_C^2$ is compared with the reference voltage of upper H-bridge, V_R^1 which is then fed to PI_1 controller for providing reference current to control the inner current loop.

In inner current control loop, PI_1 output is multiplied with sinusoidal signal which is in same phase with the grid voltage V_{grid}, a Phase Locked Loop (PLL) is used for providing this sinusoidal signal. Finally the reference current, I_{grid}^* is compared with grid current, I_{grid} fed to PI_3. The output of controller PI_3 i.e. V_{grid}^* is subtracted from the grid voltage V_{grid} thus generating a reference signal V_{ref1} for the inverter. The inner current control loop plays an important role to keep the power factor closed to unity. The DC link voltage of lower H-bridge, V_C^2 is compared with reference voltage, V_R^2 and fed to PI_2. Output of PI_2 controller is also multiplied with the sinusoidal signal which is in phase with grid voltage thereby generating the second reference signal, V_{ref2}.

The two references, V_{ref1} and V_{ref2} are combined and generates nine-level PWM pulse for the asymmetrical

multilevel inverter (MLI).

In this work, the purpose of controller is to synchronize the MLI output with grid and prevents voltage-current unbalancing under all condition. Controller is designed by considering that the overall PV module output voltage is always greater than the grid voltage, even under cloudy weather when irradiance level falls still PV module output voltage should greater than grid voltage, otherwise power flow will be reversed. Controller is designed with the same concept as for controlling conventional cascade MLI in [20,27,24]. Control scheme based on two loop model as shown in fig 6.

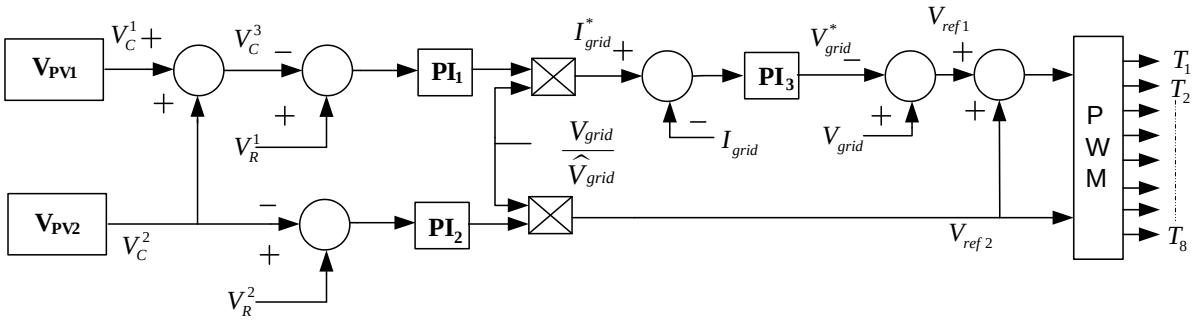

Fig. 6. Controller for proposed asymmetrical Multilevel Inverter

3.1. Stability Analysis

For controlling the inverter PWM, closed Loop system must be stable. The stability of the closed loop is shown by Bode magnitude and phase plot. This paper uses direct MATLAB linear analysis for Bode plot It is observed from the Bode plot that the open loop system is stable, Fig. 7(a), shows the stability of the outer voltage controlled loop and the Fig: 7 (b) shows stability of the overall control loop.

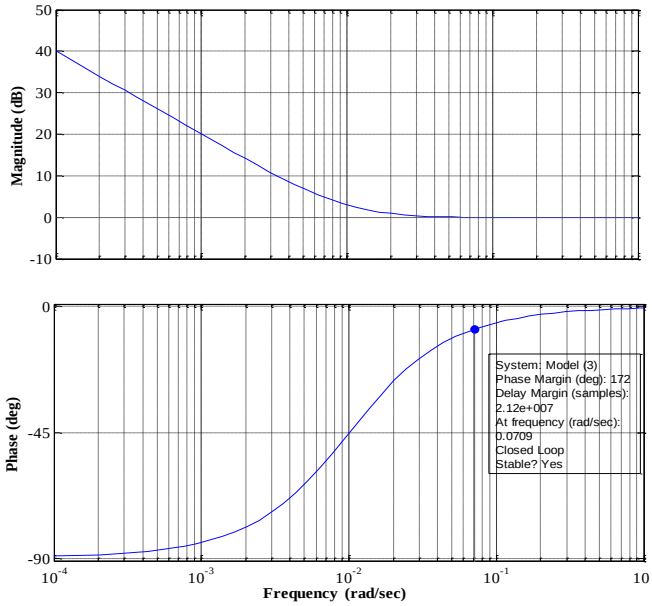

Fig. 7(a). Bode Plot of outer voltage controlled Loop

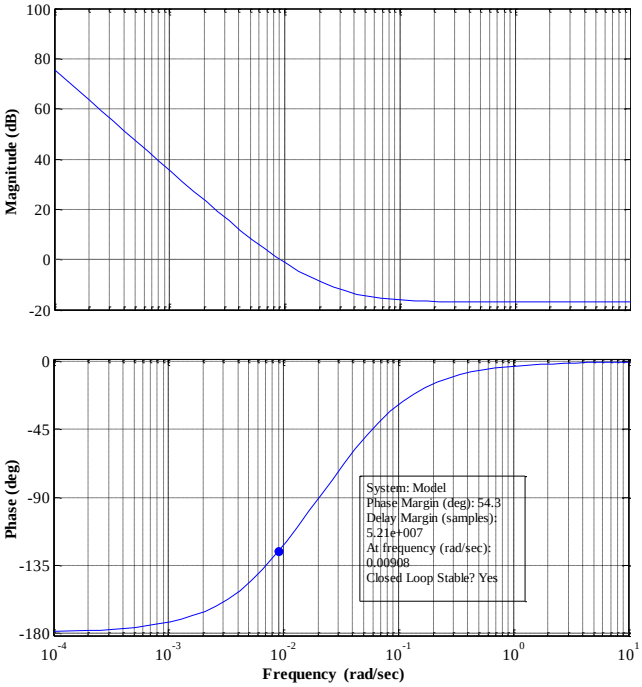

Fig. 7(b). Bode Plot of overall control Loop

4. Simulation Results and Discussion

In asymmetrical CHB-MLI, the voltages in two bridges are in 3:1 ratio, there are always chances of unequal magnitude of levels under varying irradiance level. This work is mainly designed for irradiance level of 1000 W/m^2 and temperature 25°C under this irradiance level voltages are in perfectly 3:1 ratio. Under varying irradiance i.e. 800 W/m^2 and 600 W/m^2 and constant temperatures 25°C, there is a little variations in 3:1 voltage ratio. When the irradiance level fall DC link voltage of the two bridges also fall. Fig. 8(a), shows the simulation result for PV cell DC link voltage under different irradiance level.

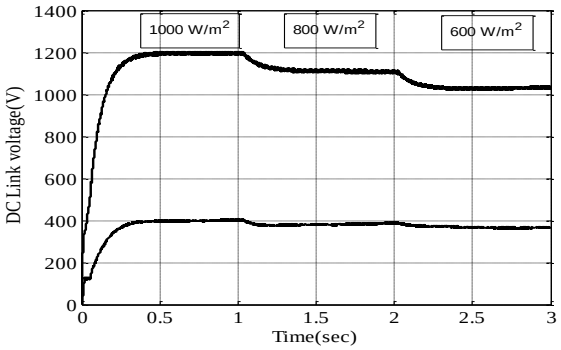

Fig. 8(a). DC Link Voltage under Varying Irradiance and Constant Temperature (25°C).

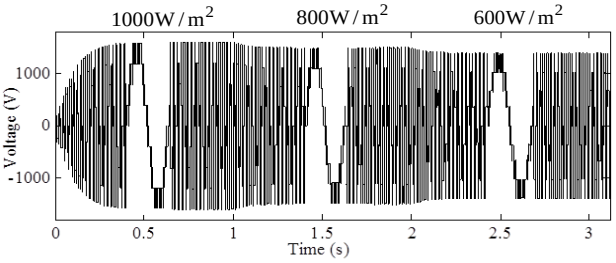

Fig. 8(b). Nine Level Output Voltage Under Varying Irradiance and Constant Temperature.

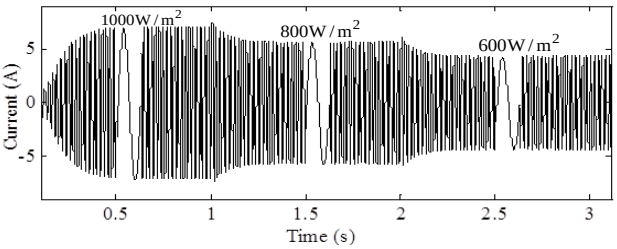

Fig. 8(c). Filtered Current Output Under Varying Irradiance.

In fig. 8(b) shows the nine-level asymmetrical MLI output voltage under varying irradiance and fig.8(c) shows filtered current output of MLI under different irradiance level. Both the figures are magnified to show the levels of output voltage and nearly sinusoidal current for 1000 W/m^2 , 800 W/m^2 and 600 W/m^2 at the constant temperature of 25°C.

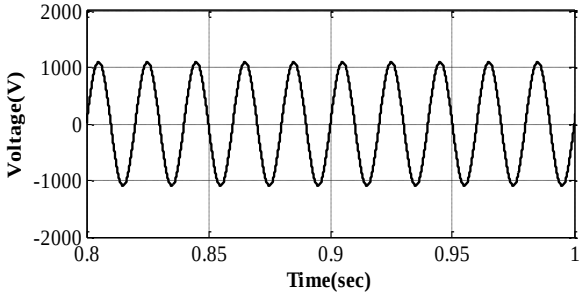

Fig. 9(a). Grid Voltage at Irradiance 1000W/m^2

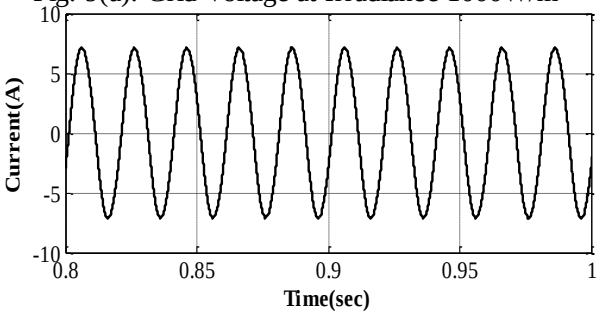

Fig. 9(b) Grid Current at Irradiance 1000W/m^2

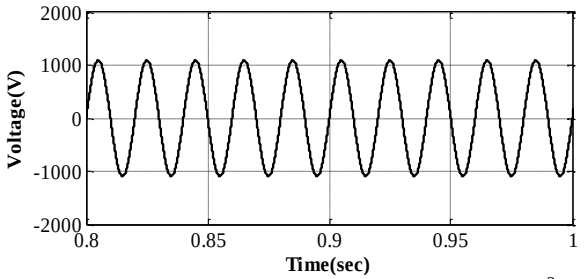

Fig. 9(c) Grid Voltage at Irradiance 800W/m^2

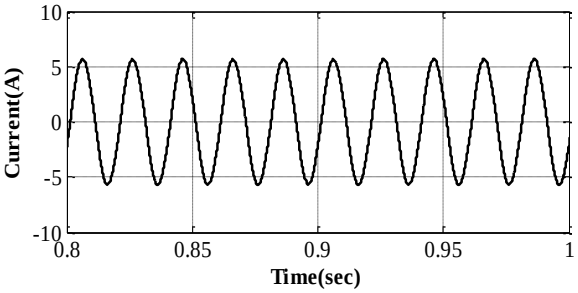

Fig. 9(d) Grid Current at Irradiance 800W/m^2

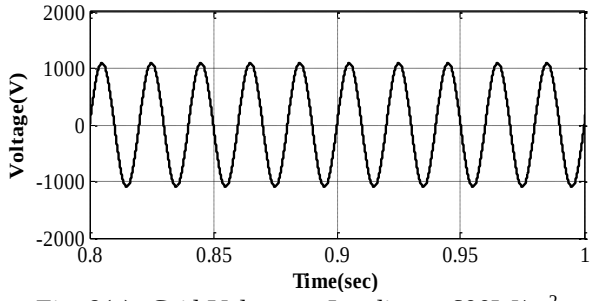

Fig. 9(e). Grid Voltage at Irradiance 600W/m^2

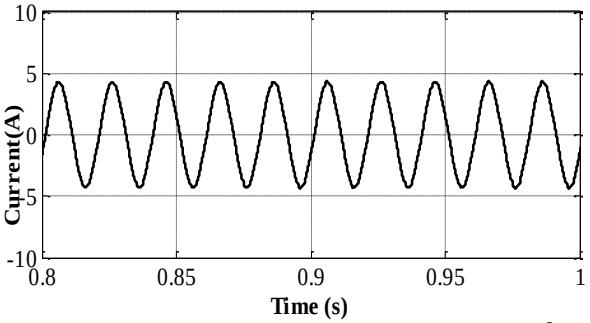

Fig. 9(f). Grid Voltage at Irradiance 600W/m^2

In fig.9 (a)-9(b) grid voltage and inverter current under 1000W/m^2 irradiance level are shown. Similarly, 9(c)-9(d) and 9(e)-9(f) shows grid voltage and inverter current under 800 W/m^2 and 600 W/m^2 respectively. Under varying irradiance, current and voltage are nearly in same phase i.e. power flow will be always from source side to grid side keeping the power factor close to unity.

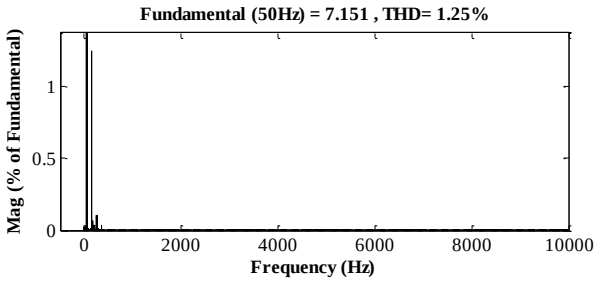

Fig. 10(a). % THD (APOD) under 1000W/m^2

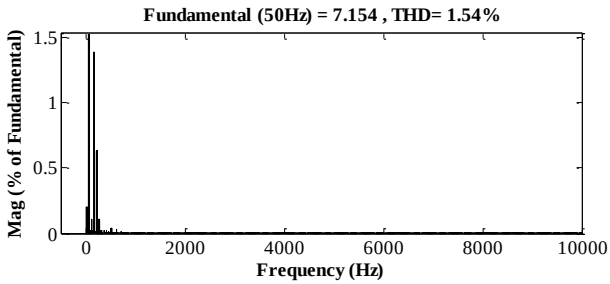

Fig. 10(b). % THD (PD) under 1000W/m^2

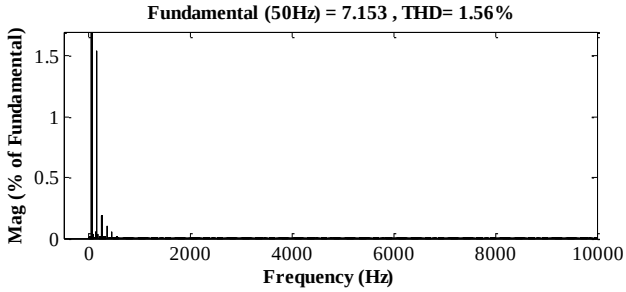

Fig. 10(c). % THD (POD) under 1000W/m^2

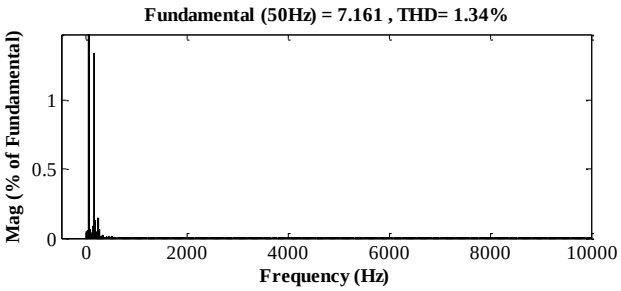

Fig. 10(d). % THD (Phase Shift) under 1000W/m^2

THD analysis of the current is shown in fig. 10(a)-(d). This work is focused for 1000W/m^2 irradiance, the DC Link output voltage at 1000W/m^2 is in exactly 3:1 ratio, so the ripple in current is very less. Under this condition, best result is obtained for APOD scheme where THD level is around 1.25%, THD level for other PWM control is also shown. With fall in irradiance, voltage ratio of 3:1 is getting disturbed i.e. there is a small percentage of error occurs in 3:1 ratio of DC link voltage thereby when irradiance falls from 1000 W/m^2 to 800 W/m^2 and 600 W/m^2 THD level of all the four PWM control method increases.

Table. 4. %THD at Different Irradiance.

Irradiance	PD-SPWM	POD-SPWM	APOD-SPWM	PS-SPWM
1000W/m^2	1.54	1.56	1.25	1.34
800W/m^2	1.64	1.51	1.61	1.63
600W/m^2	3.41	2.98	3.43	3.37

It is noticed from table 4 that at 1000 W/m2 APOD scheme provides the better result but as the irradiance fall, POD provides the better result among other PWM control. When the DC link voltage of asymmetrical cascaded MLI is not perfectly in the ratio of 3:1 due fall in irradiance, POD scheme provides better THD performance.

5. Conclusion

In modern power system, Grid connected PV cell applications are in demand, Grid tied MLI with PV cell could be good choice for generation of voltage and with using asymmetric MLI the cost and complexity of conventional symmetrical MLI is minimized. This paper analyzed the performance of asymmetrical cascaded MLI with PV cell for Grid connected application. From all the THD analysis of different PWM scheme, it is seen that the Level shifted APOD scheme is best at constant irradiance for asymmetrical cascaded MLI when exact ratio of voltage is maintained whereas under irradiance variance, POD scheme provides the best result. A different controller is presented in this work which is capable of operating under varying irradiance condition for asymmetrical cascaded multilevel inverter.

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