

# COMPARATIVE STUDY BETWEEN PSPWM AND SVPWM TECHNIQUES BASED ON MLI FOR INDUCTION MOTOR DRIVE

**Ahmed EL-SANABARY**

Port Said University, Portsaid, Egypt  
eng\_san88@yahoo.com

**Ahmed E. KALAS**

Port Said University, Portsaid, Egypt  
kalas\_14@yahoo.com

**Osama M. EL BAKSAWI**

Port Said University, Portsaid, Egypt  
usama\_bak@yahoo.com

**Kamel EL-SERAFY**

Port Said University, Portsaid, Egypt  
relserafi@hotmail.com

**Abstract:** Multi-level inverters (MLIs) are recently the promising converters for high-power medium-voltage AC drives due to their superior characteristics over conventional 2-level converters. This paper presents a study for the performance of Induction Motor drive using different modulation techniques based on Multi-level cascaded inverter topology. The applied pulse width modulation (PWM) techniques are Phase shifted PWM which is the preferred Sinusoidal PWM for this topology and space vector PWM. A simple space vector modulation algorithm is introduced for this comparison. A passive filter is carefully designed in order to reduce the distortions of the resulted voltage and current waveforms to safe limits. Experimental setup is implemented for this study using DS1104 control unit. In this paper, simulation and experimental results are carried out to investigate the differences between the modulation techniques for these drives.

**Key words:** Multi-level inverter, AC drives, SPWM, SVPWM, topology, filter design.

## 1. Introduction

IN RECENT YEARS, as the demand of high power, medium voltage drive (MVD) applications is increasing, MVD inverter structures are receiving a great attention in researching and marketing affairs. The trend now is to replace the traditional two-level inverters with Multi-level inverters (MLI)s to guarantee a high power quality and efficient performance for MVDs as they generate output waveforms with low total harmonic distortion (THD) and smaller common voltages. They can also operate at lower switching frequencies and sustain higher operating voltages [1]–[4].

The main MLI topologies are capacitor-clamped (flying-capacitors), diode-clamped (neutral-clamped), and cascaded H-bridge inverters. Compared to other topologies, cascaded Multi-level inverter has the higher ratings of output voltages and power besides it's considered the most reliable and modular topology. However, it faces some difficulties in the availability of isolated voltage sources and the complexity of the layout due to the large number of semiconductor switches [5]–[8].

Several modulation techniques are applied for MLIs such as Selective Harmonic Elimination (SHE), Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM)[9]–[11]. SPWM and SVPWM are using high switching frequencies. SPWM splits into Phase Shifted SPWM and Level Shifted SPWM, Phase Shifted SPWM is applicable for Cascaded MLI[12]. SVPWM is a digital modulation technique firstly applied for two-level inverter. It's then extended to MLIs but with more complex algorithms. However, it is considered the optimal technique as: i) It can utilize the highest dc link voltage which reduces THD and commutation losses; ii) It is applicable for digital signal processing (DSP) implementation [13], [14]. For power quality and performance enhancement for these drives, passive filters should be used to compensate the harmonic distortion and the reactive power [15]. An LC filter is designed to reduce the total harmonic distortion (THD) according to IEEE standard limits. This paper studies the performance of induction motor drive system applying two PWM techniques based on a 3-level cascaded inverter showing THD minimization using LC filter. The whole control system is implemented using MATLAB /SIMULINK. A prototype system using digital signal processing (Dspace 1104) control unit is built and experimental results are obtained to validate the simulation work.

## 2. Inverter Topology

Fig.1 shows the popular topology of cascaded Multi-level inverters. A three phase, three-level inverter circuit is used. It consists of 3 cells for each phase. Each cell has 4 switches with a separate dc-bus voltage.

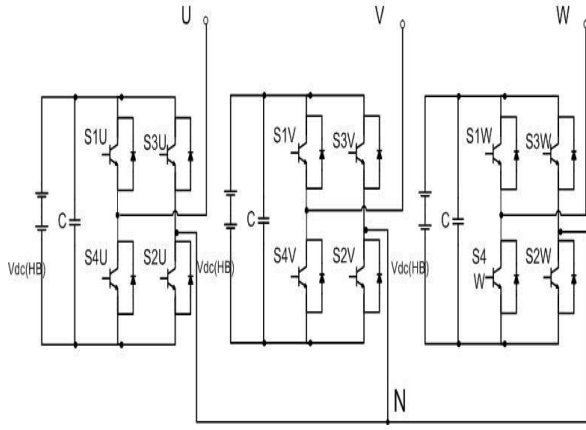


Fig.1 Three level inverter.

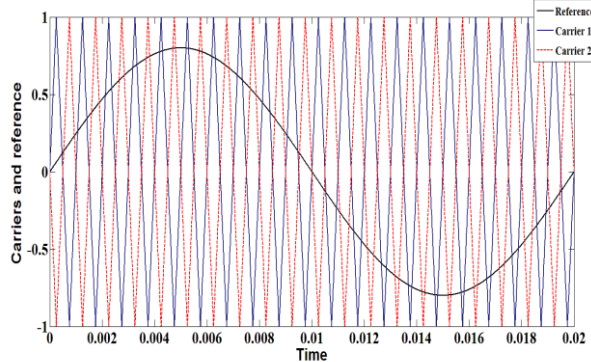
### 3. Phase shifted PWM

Several techniques based on the classical SPWM have been developed to apply on multilevel inverters. Multicarrier PWM methods for multilevel inverters are described in many publications in the technical literature [16]–[18]. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. Phase Shifted PWM is particularly selected for cascade H-bridge because the comparing signals can directly drive converter switches. In PSPWM, The principle of standard 2-level PWM is modified to use more than one carrier to generate the driving signals. In a converter with  $n$  levels,  $(n - 1)$  phase shifted carriers are necessary. The phase shift is done to minimize the harmonic distortion of the output using the delay ( $\Delta$ ) given by[19];

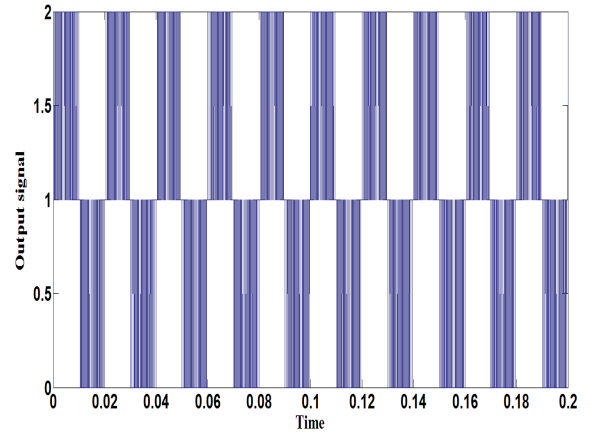
$$\Delta = \frac{T_s}{n-1} \quad (1)$$

Where: ' $T_s$ ' is the switching period.

For a 3-level inverter, the carriers needed are two carriers with a delay equal to  $(\Delta = T_s/2)$ ; to drive the gate signals. The output waveform is generated as the sum of all the comparison signals as in Fig.2.b.



(a)



(b)

Fig.2 Phase Shift PWM signal waveforms for 3-level converters in per unit. a) Carriers and reference; b) Output waveform; ( $M_a = 0.8$ ,  $f_{sw} = 1$  kHz).

### 4. Space vector PWM

A lot of SVPWM algorithms have been presented during last years [20]–[24]. The chosen scheme is based on a simple SVPWM algorithm proposed by Gupta [25], [26]. The concept of space vector modulation is derived from rotating field of AC machine which is used for modulating the inverter output voltage. The three phase quantities can be transformed to their equivalent 2-phase quantity either in synchronously rotating frame (or) stationary frame [27].

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

The space vector diagram of a three-phase, 3-level voltage source inverter is a hexagon, consisting of six sectors. Each sector has four triangles as shown in Fig.3.

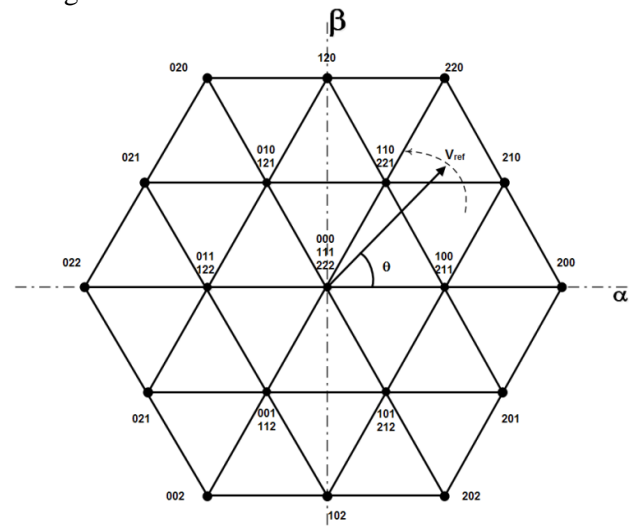


Fig.3 the space vector diagram.

The algorithm is illustrated in Fig.4 which shows how to locate the voltage vector ( $V_{ref}$ ) in the first sector which is applicable for other sectors too. Here, the location of point P is detected by identifying its triangle, and then the on-times for this triangle can be calculated using the virtual two-level geometry. For optimal switching sequence, voltage vectors should be chosen to decrease the number of switching when transferring from states to another to decrease thermal stresses on active switches.

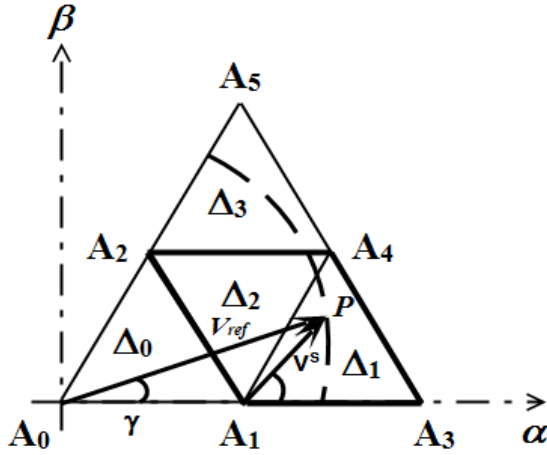


Fig.4 first sector of the space vector diagram [25].

The search for the triangle that has point P can be obtained by using two integers  $k_1$  and  $k_2$ , which are dependent on the coordinate ( $v_\alpha, v_\beta$ ) of point P as [25]:

$$k_1 = \text{int} \left( v_\alpha + \frac{v_\beta}{\sqrt{3}} \right) \quad (3)$$

$$k_2 = \text{int} \left( \frac{2v_\beta}{\sqrt{3}} \right) \quad (4)$$

Where; the reference vector ( $v_{ref}$ ), moves on a circular trajectory as shown in Fig.4. The point P of the reference vector can be located in any of the four triangles ;( $\Delta_0 - \Delta_4$ ).

## 5. Harmonics problem and filter design

The special feature of MLIs is that when the number of levels is increased; it reduces the THD. Even though, this reduction is not enough for safe operation limits for standalone load applications. According to the “IEEE std. 519 -1992” limits; the THD value of output voltage and current waveforms for 3-level inverter should not exceed 5%. These harmonic distortions can be regulated using a passive filter to improve the drive system performance[28].

LC filters are used to attenuate the harmonics. LC-

filter has one inductor in series and one capacitor connecting in parallel with inductor. To design the filter, some limits on the parameter values should be considered [29]–[31]. For a standalone load, the system impedance may be considered infinite while for the grid, or a micro-grid, it may be almost zero (the stiff mains). The filter transfer function has been derived using its single phase electrical diagram as shown in Fig.5. The equations for the currents and voltages of the filter is given by (5), (6) [32], [33].

$$V_i(s) = I(s) \left( L_f s + \frac{1}{C_f s} + R_d \right) \quad (5)$$

$$V_o(s) = I(s) \left( \frac{1}{C_f s} + R_d \right) \quad (6)$$

Where  $s$  denotes the Laplace operator and  $L_f$ ,  $C_f$  and  $R_d$  are the filter inductance, capacitor and damping resistor respectively.

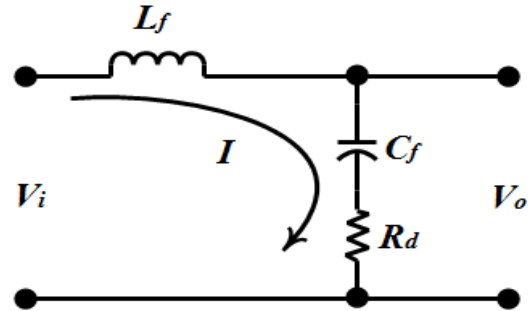


Fig. 5 LC-filter equivalent circuit.

To design the filter inductor [30]; the inverter circuit operation is similar to a buck chopper and it works according to its switching frequency. The conventional voltage equation of any inductor is:

$$V_L(t) = L \frac{di(t)}{dt} \quad (7)$$

This equation can be re-written in Eq.8 according to the circuit parameters; knowing that the worst case ripple condition is at duty cycle of 0.5 and the filter inductor should limit the ripple current to 10% of the rated output current.

$$L_{filter} = \frac{V_{dc}}{8 f_{sw} \Delta I_{max}} \quad (8)$$

The capacitor value is calculated as a fraction ( $x$ ) of the reactive power absorbed at rated power which indicates to the power factor. This fraction is limited to the maximum power factor variation seen of 0.05p.u; however, values  $> 0.05p.u$  can be used [34]:

$$C_f = x \cdot C_b ; \quad 0.05p.u < C_f < 0.1p.u \quad (9)$$

However, the oscillation should be avoided using passive damping resistor; this resistor can be calculated as in Eq.10 [18];

$$R_d = \frac{1}{3 \cdot w_{res} \cdot C_f} \quad (10)$$

All parameter values of this filter design are shown in Table.1.

Table.1 Parameter values of LC filter Design for Multi-level inverter connected with IM

| System parameters |                         |
|-------------------|-------------------------|
| $V_{dc}$          | 300 V                   |
| $f_{sw}$          | 3.6 KHz                 |
| $V_{n(L-L)}$      | 400 V                   |
| $P_n$             | 5 KW                    |
| $f_n$             | 50 Hz                   |
| $L_f$             | $5.08 \cdot 10^{-3}$ H  |
| $C_f$             | $5 \cdot 10^{-6}$ Farad |
| $f_{res}$         | 1 KHz "within limits"   |
| $R_d$             | 10 ohm                  |

## 6. Simulation results

The cascaded inverter is simulated using Matlab/Simulink and the following results of voltage and current waveforms for both PSPWM and SVPWM 3-level inverters are obtained in order to investigate and compare the performance of CHB Multilevel inverter using the induction motor as a standalone load. Fig.6 and Fig.7 show the resulted line-line voltage waveforms while Fig.8 and Fig.9 show the waveform of phase currents drawn by the induction motor.

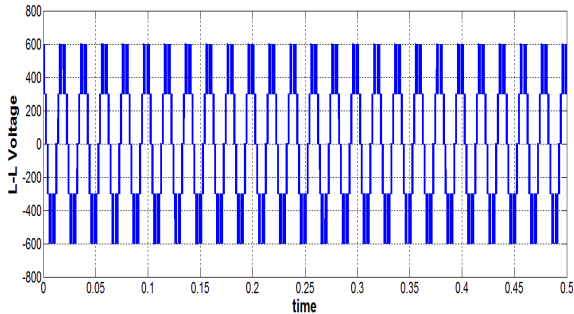


Fig.6 Line – Line Output voltage waveform of Induction motor using SVPWM.

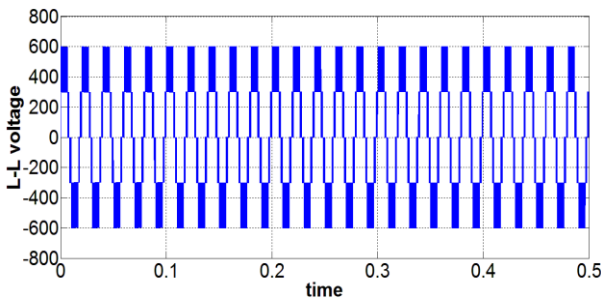


Fig.7 Line – Line Output voltage waveform of Induction motor using PSPWM.

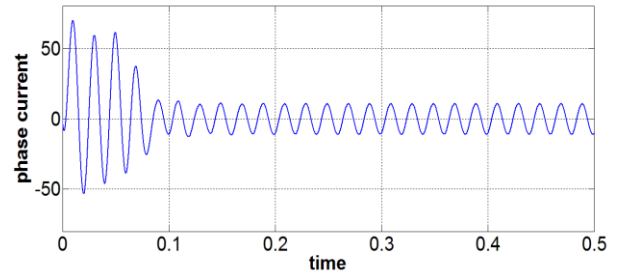


Fig.8 phase current waveform of Induction motor using SVPWM.

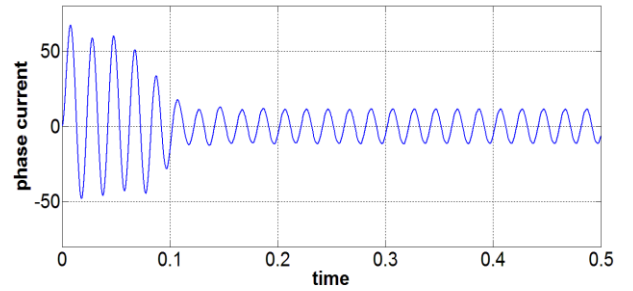


Fig.9 phase current waveform of Induction motor using PSPWM.

The THD of the Output voltage for both 3-level inverters connected to the induction motor are reduced to safe values as shown in the following results. Consequently; the current profile drawn by the induction motor is enhanced. The following results of THDs for 3-level inverter using LC filter are shown in figures to approve this enhancement.

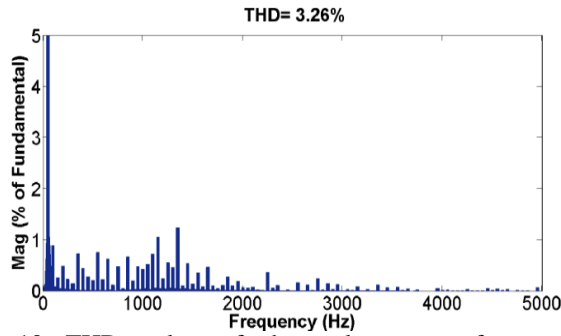


Fig.10 THD value of the voltage waveform of Induction motor using SVPWM.

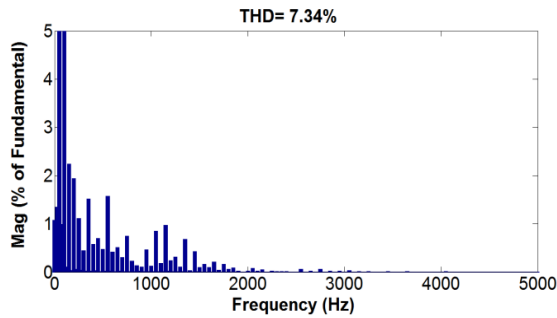


Fig.11 THD value of the current waveform of Induction motor using SVPWM.

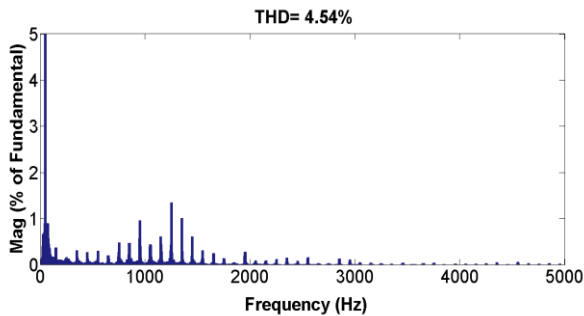


Fig.12 THD value of the voltage waveform of Induction motor using PSPWM.

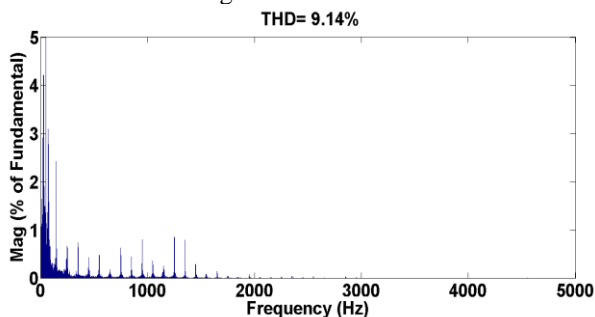


Fig.13 THD value of the current waveform of Induction motor using PSPWM.

As the motor drive is characterized by its torque; it's likely to show the torque profile of this motor in both modulation techniques. Figures 14 and 15 show the motor torques with a good dynamic performance. However, there are notable torque pulsations when using PSPWM compared to SVPWM due to higher current harmonic components.

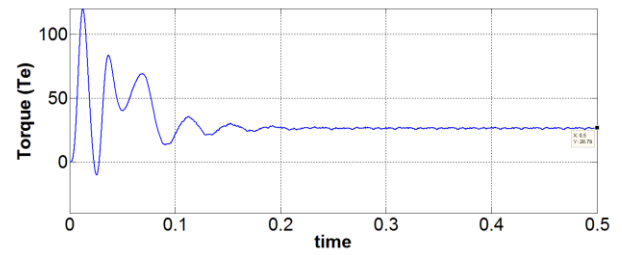


Fig.14 Output torque of Induction Motor connected to 3-level inverter using SVPWM.

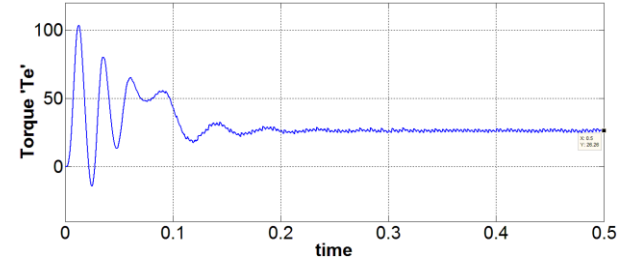


Fig.15 Output torque of Induction Motor connected to 3-level inverter using PSPWM.

## 7. Experimental results

In order to validate the simulation results, a prototype system for multi-level inverter drive is implemented using digital signal processor (Dspace 1104) control kit. The experimental tests are carried out using a low power converter system, as shown in Fig.16, with the following parameters:  $V_{dc} = 120$  V,  $f_c = 3.6$  kHz,  $f_e = 50$  Hz and const. load torque.

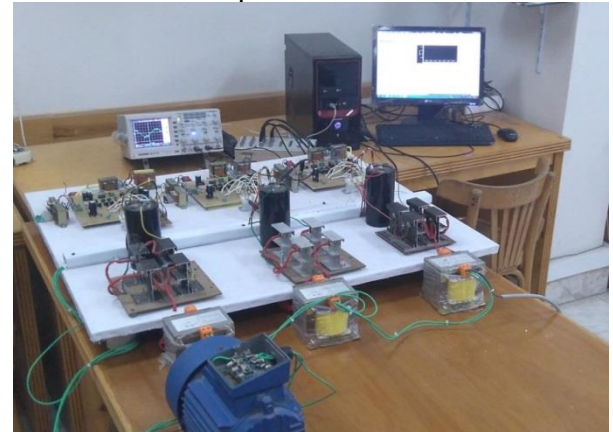


Fig.16 Experimental setup of MLI, interface boards, and DSP controller.

Figures 17 and 18 show the line-line voltage  $V_{L-L}$  and phase current waveforms ( $V_{L-L}=106.7$  volts and  $I_{ph}=1.414$  Amp.) with  $M_a$  at 0.9 and frequency = 50 Hz, respectively.



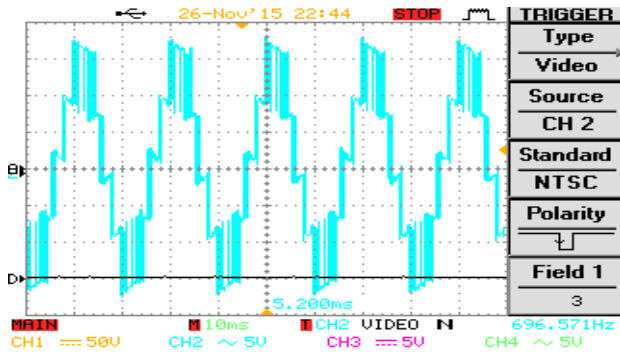


Fig.17 Measured Line – Line Output voltage (scale 50V/div.).

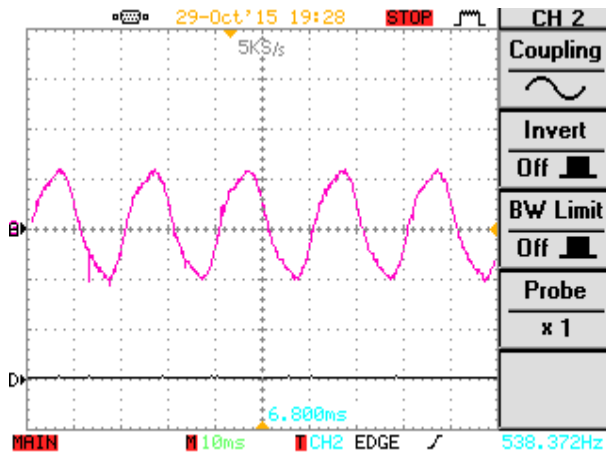


Fig.18 Measured Phase current of IM (scale 200mV/div.), (sensor 100mV/Amp.).

A comparison between THD values for each inverter is conducted in Table.2.

Table.2 Comparison between THD values for each inverter

| 3-level | Voltage THD "Using PSPWM" | Voltage THD "Using SVPWM" | Current THD "Using PSPWM" | Current THD "Using SVPWM" |
|---------|---------------------------|---------------------------|---------------------------|---------------------------|
|         | 4.54 %                    | 3.26 %                    | 9.14 %                    | 7.34 %                    |

## 8. Conclusion

This paper has presented a detailed analysis of the induction motor drive for different PWM techniques based on a 3-level cascaded inverter showing THD minimization using LC filter. PSPWM and SVPWM have been applied to the Cascaded MLI as the preferred modulation techniques for this topology. The passive filter has been designed to limit the THD of output voltage to the standard safe limits typically ( $\leq 5\%$ ). A

prototype system for the 3-level cascaded inverter has been presented in this paper to validate the simulation work. Using this filter; the measured values of THD obtained are 3.26% for SVPWM and 4.54% for PSPWM while these values for the current are 7.34% for SVPWM and 9.14% for PSPWM. It is noticed that the aimed THD reduction of the output voltage has been achieved; also, the current profile of the motor has been enhanced but its THD is still higher than standards which affects the motor torque profile. Although the output voltage of both techniques has achieved the IEEE standards, it is concluded that SVPWM converter drive gives a higher quality than PSPWM using the same filter size. So; there is no need to increase the number of levels for this kind of drives to avoid extra expenses of adding components. On the other hand, it'd be effective to implement the 5-level inverter to determine the differences. In practice, it's convenient to use multilevel inverters up to 5-levels for such a drive.

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