MULTILEVEL INVERTER TOPOLOGIES USING FLIPFLOPS

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Abstract: Multilevel inverters are used in high power applications for reducing the voltage rating of the semiconductor switching devices. This paper proposes three types of multilevel inverter topologies by using flip flops and logic gates. The topologies are five level cascaded multilevel inverter, five level diode clamped multilevel inverter and five level flying capacitor multilevel inverter. The switching states of the topologies are formed as the Boolean equations by using the four bit counter. The equations are given as the input to the each switch of the multilevel inverter by using the logic gates. The proposed topologies can produce the five level output which are nearer to the sinusoidal wave. This proposed system is used to reduce the total harmonic distortion (THD) and also increases the performance of the system.

Key words: CMLI, DCMLI, FCMLI, flip flops, gates.

1. Introduction.

An inverter is an electronic device used to convert the Direct Current (DC) into Alternating Current (AC). Multilevel inverters are classified into three types: cascaded multilevel inverter, flying capacitor multilevel inverter and diode clamped multilevel inverter. Flip flop is a data storage element that has two stable states. It is used to store the state information. Flip flops can be splitted into types. It can be simple or clocked. The simple one is latches, while clocked devices are called as flip flops. Bharatkar et al [1] proposed a cascaded multilevel inverter for high voltage and high power output application. Khoun jahan et al [2] developed a topology which reduces the number of switches and cost. K. Sudheer Kumar et al [3] proposed a new multilevel inverter topology with reduced number of switches which is used to control the hybrid electric vehicles. Ayoub Kavousi et al [4] developed a cascaded multilevel inverter, in which the harmonics are minimized by using the Bee optimization method. Damoun Ahmadi et al [5] proposed the harmonic elimination method for high power multilevel inverters. FaeteFilho et al [6] presents a eleven level cascaded multilevel inverter. In this proposed method the harmonics are eliminated by using the artificial neural networks. Malinowski M et al [7] proposed different topologies, control strategies and modulation techniques for cascaded multilevel inverters. Filho F et al [8] described the single phase eleven level cascade multilevel DC-AC grid -tied inverter. Villanueva E et

al [9] proposed a single phase cascaded H bridge converter for a grid connected photovoltaic application. Haiwen Liu et al [10] described the PWM method for hybrid cascaded multilevel inverter. Daher.S et al [11] presented the multilevel inverter topologies for standalone photovoltaic systems. Jason R. Wells et al [12] developed a modulation based method for harmonic elimination. José Rodríguez et al [13] proposed different topologies with separate DC sources. It also presents control and modulation method for the topologies.   S.Sirisukprasert et al [14] analyses the multilevel voltage source converters based on modulation technique.

2. Five level Cascaded multilevel inverter using Flip flops

The general structure of the multilevel inverter is used to generate the sinusoidal waves from the several levels of input DC sources. The stress on each switching device can be reduced by using the multilevel inverter which is proportional to the number of levels of multilevel inverter. One of the proposed topology is five level Cascaded Multilevel Inverter (CMLI) which is shown in Fig. 1(a).
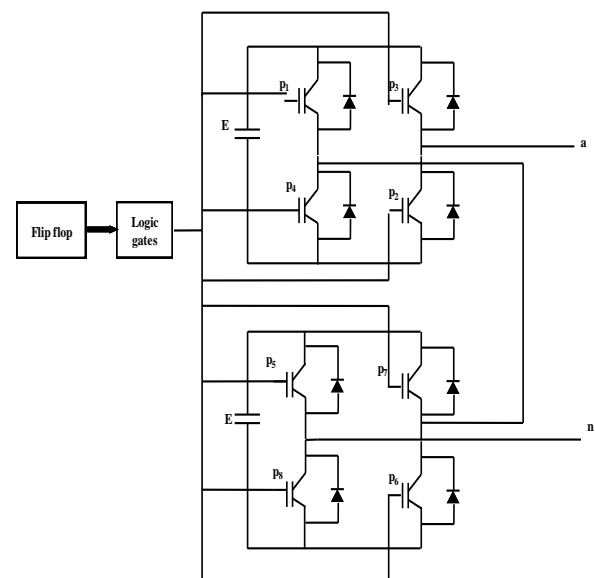

Fig. 1(a). Flip flop based five level Cascaded multilevel inverter

Table 1
Switching states of five level Cascaded multilevel inverter

Switching states								Output voltage
P1	P2	P3	P4	P5	P6	P7	P8	
1	1	0	0	1	1	0	0	2E
1	0	1	0	1	1	0	0	E
1	0	1	0	0	1	0	1	0
0	0	1	1	1	0	1	0	-E
0	0	1	1	0	0	1	1	-2E

The above table represents the switching states of the five level cascaded multilevel inverter. Here P1, P2, P3, P4, P5, P6, P7, P8 represents the switches of the multilevel inverter and E represents the input voltage source. To obtain 2E, P1, P2, P5, P6 switches will be turned ON and the other switches should be turned OFF. For E, P1, P3, P5, P6 switches are turned ON. For 0E, P1, P3, P6, P8 switches will be turned ON. To get –E, P3, P4, P5, P7 switches will be turned ON and the remaining switches must turned OFF. The switches P3, P4, P7, and P8 are turned ON for -2E. E denotes the input voltage of the multilevel inverter. By using these switching states and the four bit counter, the following Boolean equations are formed.

$$P1=C'B'A'+CBA+D' \qquad (1)$$
$$P2=D'CA'+D'B'A+D'C'B \qquad (2)$$
$$P3=C'B'A'+CBA+D \qquad (3)$$
$$P4=DCA'+DB'A+DC'B \qquad (4)$$
$$P5=C'B'+CB+D' \qquad (5)$$
$$P6=D'CB'+D'C'B \qquad (6)$$
$$P7=C'B'+CB+D \qquad (7)$$
$$P8=DCB'+DC'B \qquad (8)$$

The above equations are given as the input by using the logic gates and flip flops. The logic diagram for these equations is drawn by using the logic gates. This logic diagram for each switch is given as the input. The schematic diagram for JK flip flop is shown in Fig .1(b).
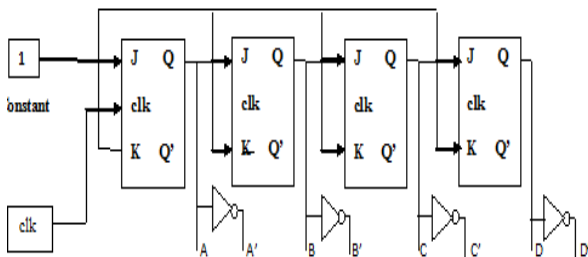

Fig. 1(b). Schematic diagram of JK flip flop

Here A, A', B, B', C, C', D, D' represents the output of the JK flip flop. These outputs are given as the input to the logic diagram which is formed by using logic gates for each switch. Each switch has the separate logic diagram. This topology produces the five level output with reduced Total Harmonic Distortion (THD). The simulation output of the five level flip flops based cascaded multilevel inverter is shown in Fig. 2.
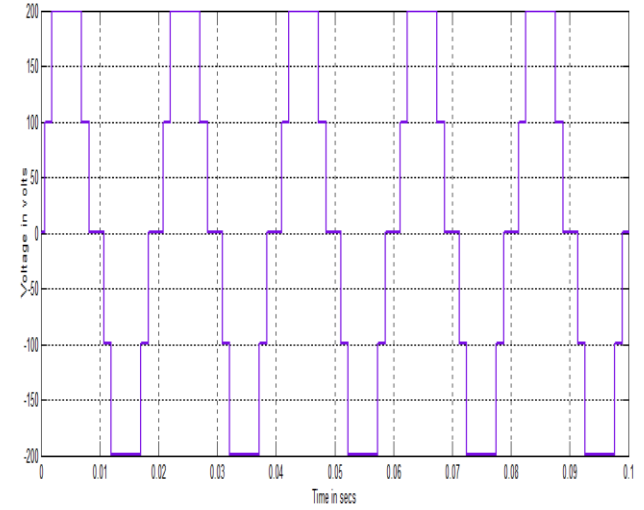

Fig. 2. Simulation output of Flip flop based five level Cascaded multilevel inverter

A logic gate is a physical device which is used to implement a Boolean function that is, it performs a logical operation on one or more logical inputs and produces a logical output. The flip flops can be classified into four types. JK flip flop, SR flip flop, D flip flop and T flip flop. The THD analysis for five level CMLI is shown in Fig. 3.
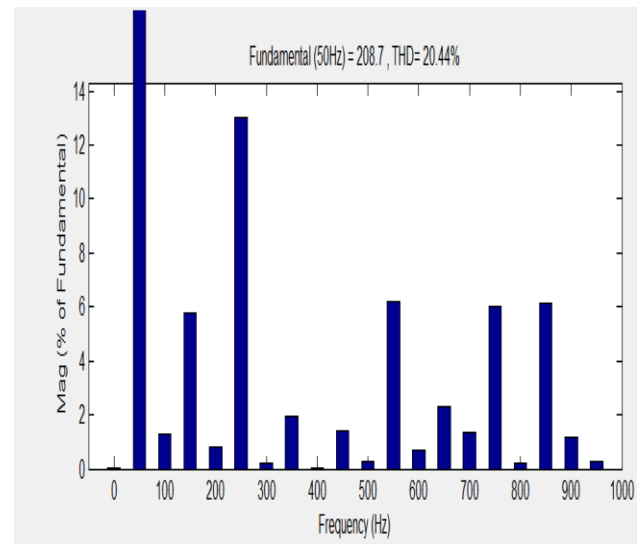

Fig. 3. THD analysis for Flip flop based five level CMLI.

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3. Five level Diode Clamped multilevel inverter using Flip flops

The next proposed method is five level Diode Clamped Multilevel Inverter (DCMLI). The schematic diagram is shown in Fig. 4.
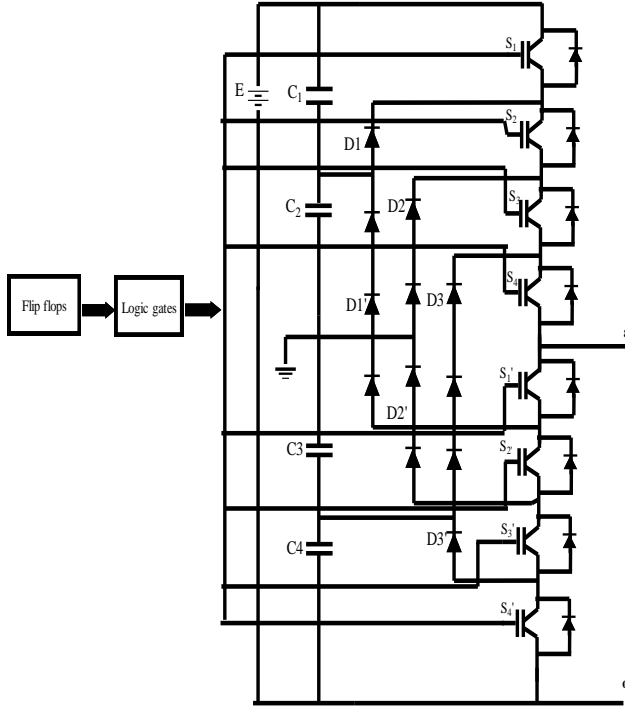

Fig. 4. Flip flop based five level diode clamped multilevel inverter

This proposed method can produce five output levels. The levels are $2V_{dc}$, V_{dc}, $0V_{dc}$, $-V_{dc}$, $-2V_{dc}$. The switching state is shown in table 2.

Table 2
Switching states of five level Diode clamped multilevel inverter

Switching states								Output voltage
S1	S2	S3	S4	S1'	S2'	S3'	S4'	
1	1	1	1	0	0	0	0	2E
0	1	1	1	1	0	0	0	E
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	-E
0	0	0	0	1	1	1	1	-2E

In the level of 2E, the upper four switches will be turned ON. For E, the upper switches S2 to S4 and the lower switch S1' should be turned ON. For 0E, turn ON the upper switches S3, S4 and the lower switches S1', S2'. In the level of –E, the upper switch S4 and the lower switches S1' to S3' must be turned ON. For -2E, the lower four switches will be turned ON. The

Boolean equations are listed below.

S1= D'CB'+D'C'B   (9)
S2= D'CA'+D'B'A+D'C'B   (10)
S3= C'B'A'+CBA+D'   (11)
S4= C'B'+CB+D'   (12)
S1'= C'B'+CB+D   (13)
S2'= C'B'A'+CBA+D   (14)
S3'= DCA'+DB'A+DC'B   (15)
S4'= DCB'+DC'B   (16)

Like the five level CMLI, this proposed system also can produce five level output with the help of flip flops and the logic gates. The simulation output of proposed five level diode clamped multilevel inverter is shown in Fig. 5.
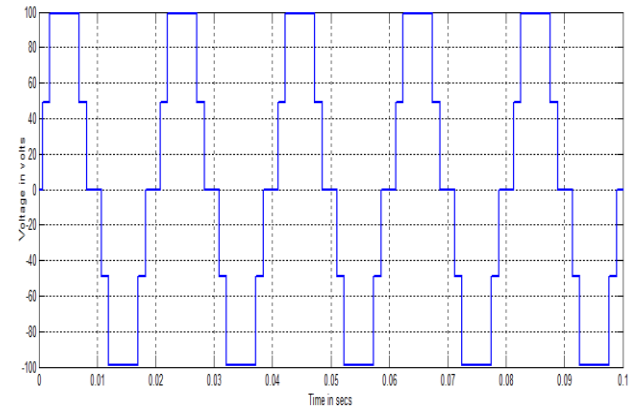

Fig. 5. Simulation output of Flip flop based five level Diode clamped multilevel inverter

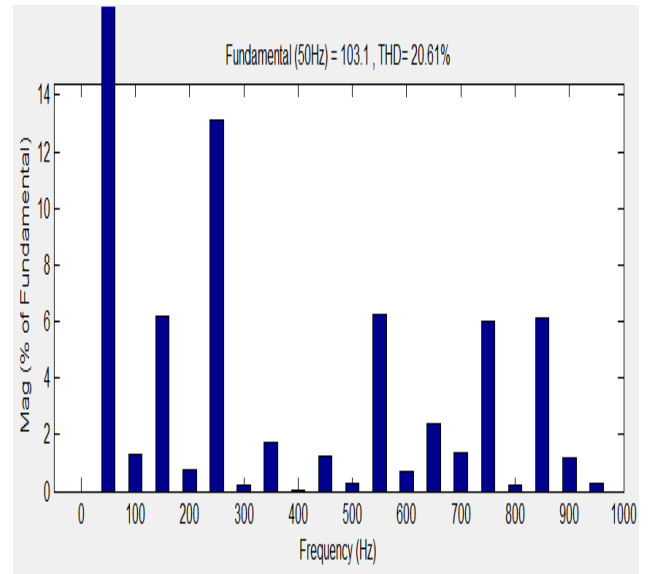The THD analysis for five level diode clamped multilevel is shown in Fig. 6.

Fig. 6. THD analysis for Flip flop based five level DCMLI.

4. Five level Flying Capacitor multilevel inverter using Flip flops

The next proposed topology is five level Flying

Capacitor Multilevel Inverter (FCMLI) using flip flops and logic gates. The schematic diagram of this proposed method is shown in Fig. 7.
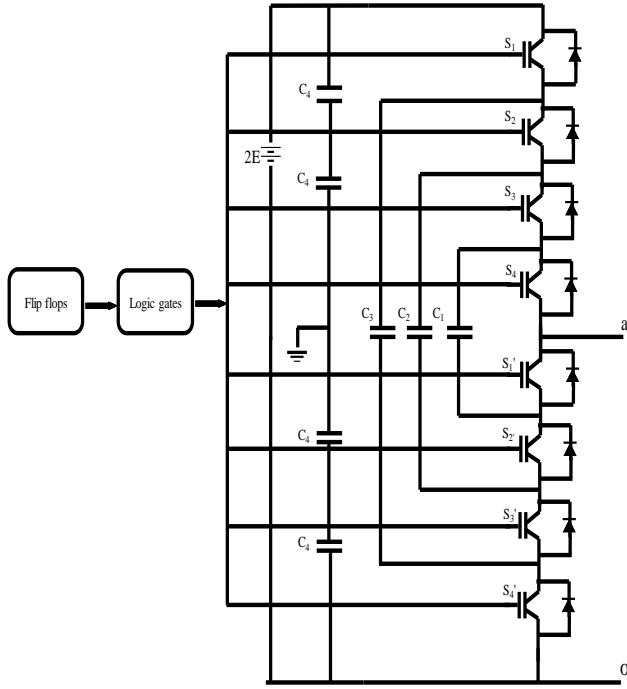

Fig. 7. Flip flop based five level flying capacitor multilevel inverter

The switching states of the above proposed method is shown in table 3. These switching states are given as the input in the form of Boolean equation as the above two proposed topologies.

Table 3
Switching states of five level flying capacitor multilevel inverter

Switching states								Output voltage
S1	S2	S3	S4	S1'	S2'	S3'	S4'	
1	1	1	1	0	0	0	0	2E
1	1	1	0	1	0	0	0	E
1	1	0	0	1	1	0	0	0
1	0	0	0	1	1	1	0	-E
0	0	0	0	1	1	1	1	-2E

To obtain 2E, the upper four switches will be turned ON. For E, turn ON the upper three switches S1 to S3 and the lower switch S1'. In the level of 0E the upper switches S1, S2 and the lower switches S1', S2' should be turned ON. For –E the upper switch S1 and lower switches S1', S2', S3' must be turned ON. To get -2E the lower four switches will be turned ON and the remaining switches should be turned OFF. The Boolean equations of proposed method is,

$$S1= C'B'+CB+D' \qquad (17)$$

$$S2= C'B'A'+CBA+D' \qquad (18)$$
$$S3= D'CA'+D'B'A+D'C'B \qquad (19)$$
$$S4= D'CB'+D'C'B \qquad (20)$$
$$S1'= C'B'+CB+D \qquad (21)$$
$$S2'= C'B'A'+CBA+D \qquad (22)$$
$$S3'= DCA'+DB'A+DC'B \qquad (23)$$
$$S4'= DCB'+DC'B \qquad (24)$$

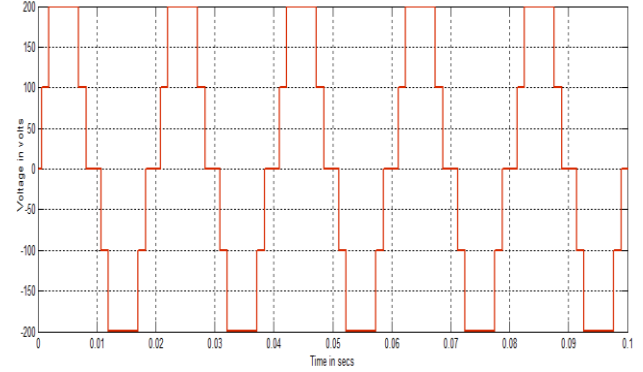The simulation output of this proposed method is shown in Fig. 8.

Fig. 8. Simulation output of Flip flop based five level flying capacitor multilevel inverter

The total harmonic distortion analysis of this five level flying capacitor multilevel inverter topology is shown in Fig. 9.

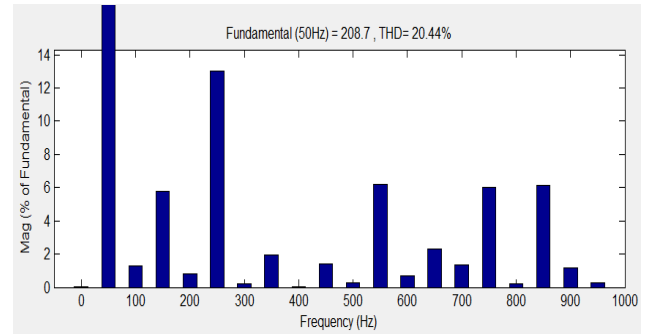$$THD= \frac{\sqrt{V_2{}^2+V_3{}^2+....+V_n{}^2}}{V_1} \qquad (25)$$

Fig. 9. THD analysis for Flip flop based five level FCMLI.

Table 4
Parameter of proposed three topologies.

Topology	Flip flop based five level CMLI	Flip flop based five level DCMLI	Flip flop based five level FCMLI
Total Harmonic Distortion	20.44%	20.61%	20.44%
RMS value	147.5	147.5	147.2

The above table represents the total harmonic distortion and the RMS value of the three proposed topologies. These THD values are lower than the conventional topologies.

$$V_{RMS} = \frac{V_P}{\sqrt{2}} \qquad (26)$$

5. Conclusion

In this paper flip flop based multilevel inverter topologies are presented. The topologies are five level cascaded multilevel inverter, diode clamped multilevel inverter and flying capacitor multilevel inverter. By using the flip flops and logic gates, the proposed inverter topologies can synthesize high quality output voltage near to sinusoidal wave. The circuit configuration is simple and easy to control. This method is mainly used to reduce the total harmonic distortion (THD) and also used to increase the performance of the system.

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