VOLTAGE STABILITY MARGIN IMPROVEMENT USING MULTI UPFCS

A. MOTIEBIRJANDI
Motiebirjandi@srttu.edu

D. FATEH
D.fateh@srttu.edu

M. ABBASI
Mhm.abbasi@gmail.com
Faculty of Electrical Engineering, Shahid Rajaee Teacher Training University, Lavizan, Tehran, IRAN

Abstract: *Unified power flow controller (UPFC) is able to improve the voltage stability margin in power system. Appropriate operation of this device is depended on its proper placement. Different papers have discussed about the placement of UPFC for improving the voltage stability margin. In most of these papers, the placement of one UPFC has addressed. In this research, a method for placement of multi UPFCs has introduced and the effects of each UPFCs has analyzed to increase voltage stability margin. For this purpose, power system loading factor has been applied to locate UPFCs and results of one or multi UPFCs effects has presented by drawing voltage profile. The proposed method has applied on IEE 5-bus and IEEE 30-bus standard systems and simulation results confirm the increase of voltage stability margin in power system.*

Key words: *Power system, Multi UPFCs placement, Power system loading factor, Voltage stability margin.*

1. Introduction.

The most important issue in power system is stability [1]. One way to increase stability is to use UPFC. But using this device requires its proper placement. In recent years, different methods introduced for placement of one UPFC. For instance in [2], one UPFC placement has been done using voltage stability index. In [3] the algorithm of differential equations is used for the placement of one UPFC for system reliability. Authors of [4-8] used artificial intelligence methods for UPFC placement. Also in [9, 10], system loading weight index factor (PI) is used for one UPFC placement. But multi UPFCs placement and providing the results of their effect is only presented in [11], using numerical method of Mixed-integer and power flow equations. In [12], using the loading factor sensitivity respect to the reactive power flow of lines, only the priority of multi UFPCs placement is discussed. But this paper has been no discussion about using multi UPFCs. Power system loading factor is an index that its increase significantly affects the voltage stability margin. For this purpose, in this research using the loading factor sensitivity respect to the reactive power flow of lines, placement of multi UPFCs and their effect on voltage stability margin is done. Voltage profile is a useful tool for evaluation of voltage stability margin in power systems. So effects of using multi UPFCs and the proposed method is studied by plotting the voltage profile for IEEE 5-bus and IEEE 30-bus standard systems.

2. Newton-Raphson Algorithm

Newton-Raphson Algorithm is used to calculate the buses voltage. For a system with n buses, the injected current into the ith bus can be written as equations (1, 2) [2]:

$$I_i = \sum_{j=1}^{n} Y_{ij} V_j \tag{1}$$

$$I_i = \sum_{j=1}^{n} |Y_{ij}||V_j| < (\theta_{ij} + \delta_j) \tag{2}$$

Complex power of the ith bus is as follows:

$$P_i - jQ_i = V_i^* I_i \tag{3}$$

$$P_i - jQ_i = (|V_i| < -\delta_i) . \sum_{j=1}^{n} |Y_{ij}||V_j| < \theta_{ij} + \delta_j \tag{4}$$

Active and reactive power equations can be obtained by separating the real and imaginary part of the complex power:

$$P_i = \sum_{j=1}^{n} |Y_{ij}||V_i||V_j| \cos(\theta_{ij} - \delta_i + \delta_j) \tag{5}$$

$$Q_i = -\sum_{j=1}^{n} |Y_{ij}||V_i||V_j| \sin(\theta_{ij} - \delta_i + \delta_j) \tag{6}$$

By expanding equation (5) and (6) as Taylor series which can be summarized:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} K & N \\ M & L \end{bmatrix} \begin{bmatrix} \Delta\delta \\ \Delta|V| \end{bmatrix} \tag{7}$$

Where K, N, M and L are matrices. Matrix K constitutes of diagonal and off-diagonal elements respectively with equations (8) and (9):

$$\frac{\partial P_i}{\partial \delta_i} = \sum_{j \neq i} |Y_{ij}||V_i||V_j| \sin(\theta_{ij} - \delta_i + \delta_j) \tag{8}$$

$$\frac{\partial P_i}{\partial \delta_j} = -|Y_{ij}||V_i||V_j| \sin(\theta_{ij} - \delta_i + \delta_j) \quad j \neq i \tag{9}$$

Matrix N constitutes of diagonal and off-diagonal elements respectively with equations (10) and (11):

$$\frac{\partial P_i}{\partial |V_i|} = 2|V_i||Y_{ij}| \cos(\theta_{ii}) + \sum_{j \neq i} |Y_{ij}||V_j| \cos(\theta_{ij} - \delta_i + \delta_j) \tag{10}$$

$$\frac{\partial P_i}{\partial |V_j|} = |Y_{ij}||V_i|\cos(\theta_{ij} - \delta_i + \delta_j) \quad j \neq i \tag{11}$$

Matrix M constitutes of diagonal and off-diagonal elements respectively with equations (12) and (13):

$$\frac{\partial Q_i}{\partial \delta_i} = \sum_{j \neq i} |Y_{ij}||V_i||V_j|\cos(\theta_{ij} - \delta_i + \delta_j) \tag{12}$$

$$\frac{\partial Q_i}{\partial \delta_j} = -|Y_{ij}||V_i||V_j|\cos(\theta_{ij} - \delta_i + \delta_j) \quad j \neq i \tag{13}$$

Matrix L constitutes of diagonal and off-diagonal elements respectively with equations (14) and (15):

$$\frac{\partial Q_i}{\partial |V_i|} = -2|V_i||Y_{ij}|\sin(\theta_{ii}) - \sum_{j \neq i} |Y_{ij}||V_j|\sin(\theta_{ij} - \delta_i + \delta_j) \tag{14}$$

$$\frac{\partial Q_i}{\partial |V_j|} = -|Y_{ij}||V_i|\sin(\theta_{ij} - \delta_i + \delta_j) \quad j \neq i \tag{15}$$

And the Jacobian matrix is defined as equation (16):

$$J = \begin{bmatrix} K & N \\ M & L \end{bmatrix} \tag{16}$$

3. UPFC model

Static model of UPFC is presented at Fig. 1 [12]. UPFC constitutes of two converters that are connected to each other with a DC link. The shunt converter (converter 1) is connected to the bus at the beginning of the line through a shunt transformer. The series converter (converter 2) is connected to the transmission line through a series transformer. This converter injects the Vs voltage into the transmission line. Converter 1 also injects or absorbs reactive power to the bus at the beginning of the line. This is shown with Iq current in Fig. 1. Also converter 1 supplies and absorbs the real power demanded by converter 2 throughout the DC link by Iq current.

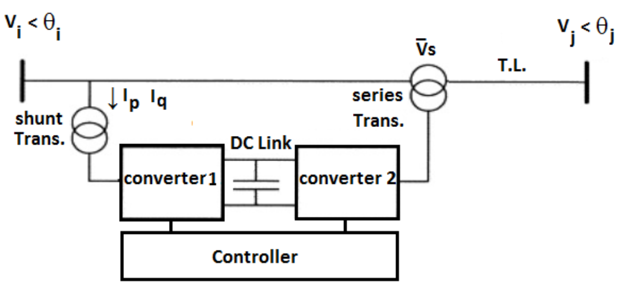

Fig. 1. Static model of UPFC.

4. Loading factor

With increasing load in power system, variations in buses voltage will occur. Loading ratio is named as loading factor (λ) and is the same for all buses in a power system. In this research, the loading factor sensitivity respect to the reactive power flow of lines is used for optimal placement of UPFC. By assumption of placing UFPC in line i-k in the way that the shunt converter is connected to bus-i, the power balance equation for bus-i is defined as (17):

$$Q_{Gi} - (Q_{Dib} + \lambda.K_{Di}.S_{\Delta base}\sin\phi_i) = Q_{ik} + \sum_{\substack{j=1 \\ ,j \neq k}}^{n} |V_i||V_i||Y_{ij}|.\sin(\delta_i - \delta_j - \theta_{ij}) \tag{17}$$

In equation (17), Q_{Gi} and Q_{Dib} are the generated and demanded reactive power at bus-i, respectively. K_{Di} is constant multiplier showing the rate of change of load at bus-i that is considered equal to 1 for all buses. $S_{\Delta base}$ is base power. ϕ_i is the load power factor angle at bus-i. $|V_i| < \delta_i$ shows the amplitude and angle of voltage at bus-i. $|Y|_{ij} < \theta_{ij}$ is the line admittance and n is the total number of system buses. The loading factor sensitivity respect to the reactive power flow through lines is defined as equation (18) [12]:

$$\frac{\partial \lambda}{\partial Q_{ik}} = Y^{-1}[Z^{-1}(1 - X) - 1] \tag{18}$$

Where

$$X = \sum_{\substack{j=1 \\ ,j \neq k}}^{n} \{[|V_i|\frac{\partial |V_j|}{\partial Q_{Gi}} + |V_j|\frac{\partial |V_i|}{\partial Q_{Gi}}].|Y_{ij}|.\sin(\delta_i - \delta_j - \theta_{ij}) + |V_i||V_j||Y_{ij}|.\cos(\delta_i - \delta_j - \theta_{ij}).[\frac{\partial \delta_i}{\partial Q_{Gi}} - \frac{\partial \delta_j}{\partial Q_{Gi}}]\} \tag{19}$$

$$Y = K_{Di}S_{\Delta base}\sin\phi_i \tag{20}$$

$$Z = \frac{\partial Q_{ik}}{\partial Q_{Gi}} = [|V_i|\frac{\partial |V_k|}{\partial Q_{Gi}} + |V_k|\frac{\partial |V_i|}{\partial Q_{Gi}}].|Y_{ik}|\sin(\delta_i - \delta_k - \theta_{ik}) + |V_i||V_k||Y_{ik}|\cos(\delta_i - \delta_k - \theta_{ik})[\frac{\partial \delta_i}{\partial Q_{Gi}} - \frac{\partial \delta_k}{\partial Q_{Gi}}] \tag{21}$$

Each line that has the highest value of the loading factor sensitivity to the reactive power flow through line is considered as the optimal place for UPFC. If amplitude of $\frac{\partial \lambda}{\partial Q_{ik}}$ is higher than amplitude of $\frac{\partial \lambda}{\partial Q_{ki}}$, bus-i is the place for shunt converter of UPFC and beginning of line i-k is its series converter and vice versa. It should be noted that UPFC should not be place at generator bus.

5. Optimal place of multi UPFCs

5.1. IEEE-5-BUS system

Fig. 2 shows IEEE 5-BUS system. In [7], lines parameters of this system is presents.

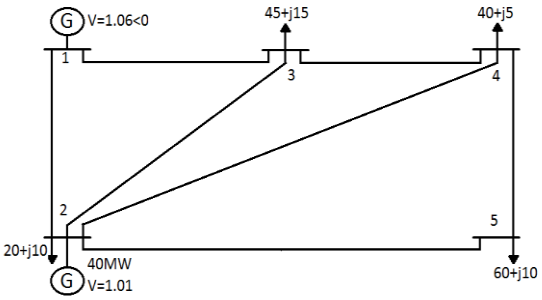

Fig. 2. IEEE 5-bus system.

To determine the optimal location of UPFC, the factor of $\frac{\partial \lambda}{\partial Q_{ik}}$ of all lines are computed and presented in Table 1 for different conditions, including system with different faults and system without fault. By analyzing Table 1, it is seen that line 3-4 in most cases has the maximum value of the factor of $\frac{\partial \lambda}{\partial Q_{ik}}$ and is considered as the best place for the first UPFC. Line 4-5 in two cases has the highest value of ($\frac{\partial \lambda}{\partial Q_{ik}}$). Thus Line 4-5 is selected as the location for the second UPFC.

Table 1

Absolute Value of $\frac{\partial \lambda}{\partial Q_{ik}}$ of all lines for IEEE 5-bus system with various contingencies.

CONTINGENCY	**Lines**			
	3-4	4-3	4-5	5-4
Intact System	24.92	4.1	0.94	2.78
Outage of Line 1-2	0.2	0.91	18.08	0.41
Outage of Line 1-3	1.4	1.03	7.72	5.7
Outage of Line 2-3	27.77	5.25	1.4	3.03
Outage of Line 2-4	64.11	5.71	0.85	3.98
Outage of Line 2-5	1.77	0.44	0.49	1
Outage of Line 3-4	-	-	0.0011	0.003
Outage of Line 4-5	7.35	0.71	-	-

5.2. IEEE-30-BUS system

Fig. 3 shows the IEEE 30-BUS system. This system's parameters are presented in [13].

Table 2 represents the value of the factor of $\frac{\partial \lambda}{\partial Q_{ik}}$ with outage of different lines. By analyzing this table, it can be seen that in most cases, four lines 24-45, 10-17, 24-23, 10-20 have the highest value of the factor of $\frac{\partial \lambda}{\partial Q_{ik}}$. Therefore, these lines are the priority of placement of multi UPFCs.

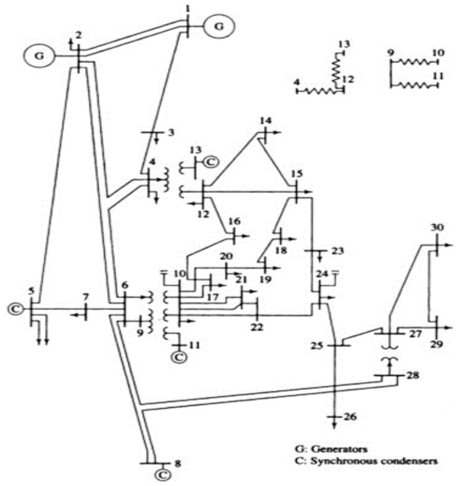

Fig. 3. IEEE 30-bus system.

With a bit more attention on the mentioned lines, it is apparent that lines 24-25 and 24-23 are connected to the bus 24 and the results show that one UPFC should be placed on bus 24. Because the line 24-25 in most cases have the highest value of $\frac{\partial \lambda}{\partial Q_{ik}}$, so the first UPFC is placed at line 24-25. Lines 10-17 and 10-20 also indicate that one UPFC should be placed at bus 10. In most cases line 10-17 has higher value of $\frac{\partial \lambda}{\partial Q_{ik}}$ in comparison to line 10-20, so line 10-17 is introduced as the proper place for the second UPFC. Also from Table 2, it is apparent that lines 12-16 and 12-14 propose the bus 12 as the third proper place for UPFC. Because the line 12-16 has higher value of $\frac{\partial \lambda}{\partial Q_{ik}}$ in comparison to line 12-14, so line 12-16 is the proper place for the third UPFC.

6. Simulation results

PSAT power system toolbox is used in order to analyze the effect of using multi UPFCs on voltage stability margin.

6.1. IEEE-5-BUS

Simulation is done for plotting bus-5 voltage profile and voltage stability margin analysis in two conditions: system with no fault and system with outage of line 2-4. First, the system voltage profile is calculated and plotted when there are no fault. Fig. 4 shows the system voltage profile with no fault in 3 conditions: without UPFC, with first UPFC and with two UPFC. According to this figure, the use of one and two UPFCs increases the voltage stability margin. Moreover, using two UPFCs has linearized the system's voltage profile. This figure shows that using one UPFC has increased the voltage stability margin compared to the case of using no UFPC. But using multi UPFCs, has a significant increase in voltage stability margin.

Table 2

Absolute Value of $\frac{\partial \lambda}{\partial Q_{ik}}$ of all lines for IEEE 30-bus system with various contingencies.

CONTINCENCY	Lines									
	24-25	24-23	10-17	10-20	12-14	12-16	21-22	4-3	15-18	15-23
Intact system	8.02	5.47	7	6.08	6.72	4.34	4.11	0.06	3	2.33
Outage of Line 1-2	2.01	4.27	4.66	4.81	4.02	549.49	3.81	0.62	27.59	8.26
Outage of Line 1-3	7.51	3.6	9.11	6.28	7.63	3.67	3.47	30.32	2.81	2.36
Outage of Line 2-4	8.09	4.82	7.25	6.1	7	4.1	3.95	0.18	2.94	2.36
Outage of Line 3-4	6.2	3.46	8.97	6.28	7.85	3.6	3.45	0	2.8	2.42
Outage of Line 2-5	3.64	5.12	8.83	6.19	7.46	4	3.36	0.42	3.05	2.58
Outage of Line 2-6	6.13	7.23	6.62	5.91	6.73	4.51	4.04	0.21	3.34	2.57
Outage of Line 4-6	2.6	3.1	4.04	4.81	4.22	20.33	5.68	11.52	21.57	10.57
Outage of Line 5-7	11.99	4.31	7.41	6.19	7	4.08	4	0.07	2.88	2.28
Outage of Line 6-7	7.21	4.79	7.49	6.18	6.98	4.21	3.96	0.14	2.86	2.29
Outage of Line 6-8	3.84	6.65	7.03	6.06	6.71	4.34	3.92	0.02	2.95	2.43
Outage of Line 12-14	5.85	12.47	7.2	5.58	0	4.25	4.35	0.08	0.06	0.04
Outage of Line 12-15	3.12	3.22	77.05	3.96	2.33	2.39	6.81	0.07	20.5	134.9
Outage of Line 12-16	6.22	4.34	4.2	7.15	5.4	0	3.91	0.04	3	2.47
Outage of Line 14-15	7.5	6.2	7.01	6	8.68	4.3	4.15	0.06	2.1	1.61
Outage of Line 16-17	7.22	4.71	5.27	6.61	6.06	7.56	4	0.01	0.94	2.36
Outage of Line 15-18	8.06	3.08	8.08	3.9	6.77	3.54	3.73	0.01	0	1.59
Outage of Line 18-19	8.3	4	7.49	4.81	6.75	3.92	3.92	0.03	0.51	1.92
Outage of Line 19-20	6.2	276.72	5.88	26.74	6.68	5.96	4.8	0.2	1.55	4.6
Outage of Line 10-20	5.6	16.87	5.61	0	6.65	6.63	5.08	0.25	1.42	6.02
Outage of Line 10-17	9.84	6.97	0	5.03	8.43	2.3	4.02	0.25	2.92	2.09
Outage of Line 10-21	1.57	1.64	7	5.6	6.85	4.65	1	0.11	3.67	1.78
Outage of Line 10-22	4.1	3.64	6.76	5.74	6.77	4.42	18.19	0.08	3.17	2.15
Outage of Line 21-22	20.42	9.51	7.23	6.34	6.75	4.2	0	0.06	2.81	2.6
Outage of Line 15-23	3.55	3.38	7.58	7.66	6.46	3.55	7.3	0.01	1.84	0
Outage of Line 22-24	1.66	2.51	7.36	5.72	7.16	4.32	3.24	0.09	3.34	2.21
Outage of Line 23-24	5.3	0	7.02	6.46	6.54	4.12	4.67	0.05	2.55	3.09
Outage of Line 24-25	0	4.24	7.36	6.27	6.42	4.28	4.81	0.18	2.9	2.11
Outage of Line 25-27	1.2	2.22	8.35	6.67	6.67	4.52	10.1	0.17	3.44	1.66
Outage of Line 27-29	158.48	4.55	7.2	6.16	6.77	4.35	4.32	0.06	3.02	2.22
Outage of Line 27-30	27.2	4.3	7.3	6.19	6.8	4.35	4.4	0.06	3.03	2.19
Outage of Line 29-30	11.86	5.11	7.06	6.11	6.74	4.34	4.18	0.06	3	2.3
Outage of Line 8-28	11.94	4.83	7.27	6.15	6.82	4.3	4.12	0.07	2.96	2.27
Outage of Line 6-28	7.42	3.12	8.75	6.51	7.2	4.06	4.44	0.14	2.93	2.08

For better understanding of using one and multi UPFCs, a fault is put in the system. Fig. 5 shows the voltage profile of system with outage of line 2-4. This figure also represents the tremendous impact of UPFCs in improving voltage stability margin. As it is seen from Fig. 5, the first UPFC has greatly increase the voltage stability margin. The voltage stability margin has increased even further by using two UPFCs.

The system's voltage stability margin, with line 2-4 outage and by using one and two UPFCs is even greater than the system's voltage stability margin in case of no fault and using no UPFC. This is pictured in Fig. 6.

Table 3 gives a numerical report of Fig. 4 and Fig. 5 for the maximum value of IEEE 5-bus system's loading factor (λ). The maximum system's loading factor increase is apparent using one and two UPFCs.

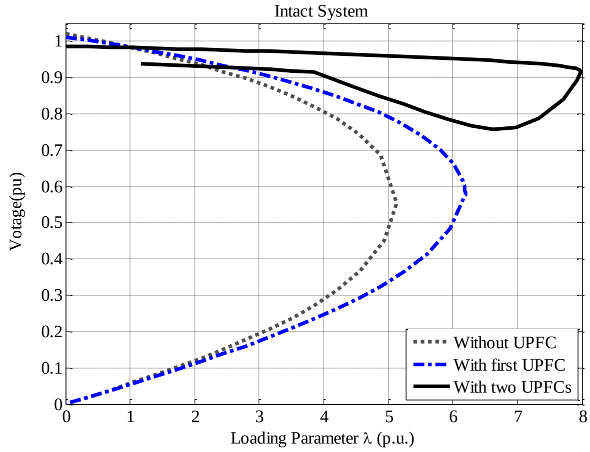

Fig. 4. Voltage profile of IEEE 5-bus system without fault.

stability margin and decrease of downward slope voltage profile using one and two UPFCs is apparent in this figure. Table 4 gives a numerical report of Fig. 7 and Fig. 8 for the maximum value of system's loading factor (λ) for IEEE 30-bus. The maximum system's loading factor increase is achieved by placing UPFCs.

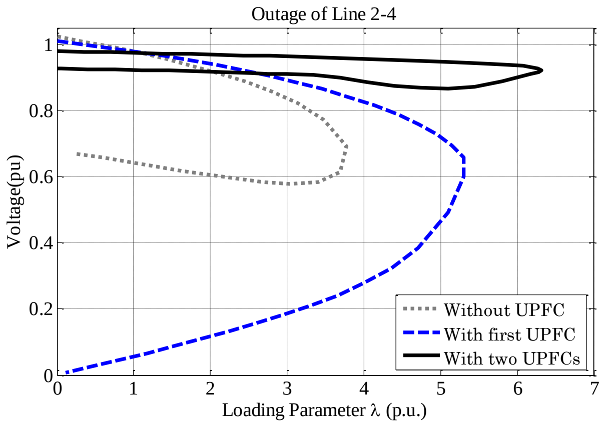

Fig. 5. Voltage profile of IEEE 5-bus system for the outage of line 2-4.

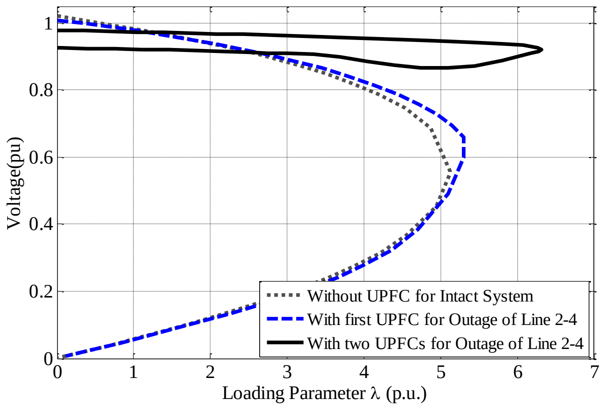

Fig. 6. Effect of two UPFCs in IEEE 5-bus system.

Table 3
Maximum loading factor(λ) of IEEE 5-bus system.

	Intact System	Outage of Line 2-4
Without UPFC	5.1	3.8
With First UPFC	6.2	5.3
With two UPFCs	8	6.3

6.2. IEEE-30-BUS

Voltage profile of bus 15 is drawn in two cases of no fault and line 12-15 outage, in order to analyze the existence of one and two UPFCs in IEEE-30-bus system. Fig. 7 shows the system's voltage profile in case of no fault. The system's voltage stability margin has increased using the first UPFC and also its downward slope is lessened. The use of two UPFCs has increased the voltage stability margin compared to the case of no UPFC and one UPFC. Also the downward slope of voltage profile in this case is lessened more than the case of one UPFC.

Fig. 8 shows the IEEE-30-bus system's voltage profile in case of line 12-15 outage. Increase in voltage

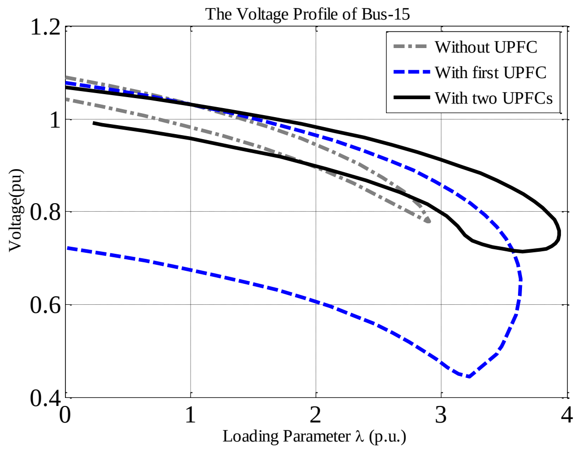

Fig. 7. Voltage profile of IEEE 30-bus system for the outage of line 12-15.

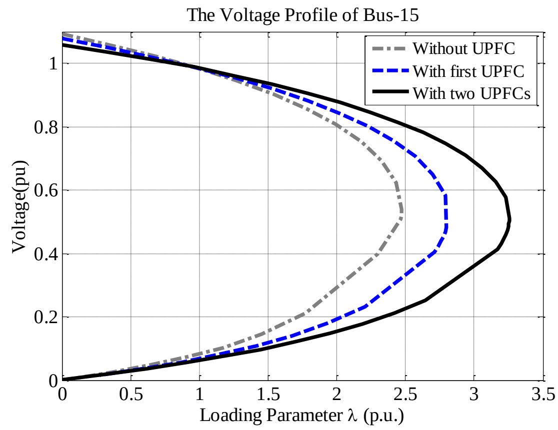

Fig. 8. Voltage profile of IEEE 30-bus system for the outage of line 12-15.

Table 4
Maximum loading factor(λ) of IEEE 30-bus system.

	Intact System	Outage of Line 12-15
Without UPFC	2.9	2.5
With First UPFC	3.6	2.8
With two UPFCs	3.9	3.25

7. Conclusion

One way to increase the voltage stability margin is using UPFC. But the appropriate operation of this device is depended on its proper placement. Different methods for placing this device are presented. But just a few papers have discussed the placement of multi

UPFCs. The major goal of this research is to place multi UPFCs in order to improve the voltage stability margin. For this purpose, placement of multi UPFCs with the help of power system's loading factor is done. This placement is done by introducing the loading factor sensitivity respect to the reactive power flow of lines, which effectiveness is certified by the results. To analyze the proposed method and impact of the placed UPFCs, voltage profile is plotted in different conditions for IEEE 5-bus and IEEE 30-bus systems.

The results for IEEE 5-bus shows that using one located UPFC has increased the voltage stability. But using the second UPFC in the mentioned system, significantly increases the voltage stability margin. Also the system's voltage stability margin, with line 2-4 outage and by using one and two UPFCs is even greater than the system's voltage stability margin in case of no fault and using no UPFC.

The results for IEEE-30-bus shows that using a located UPFC has increased the voltage stability margin. Also the voltage reduction due to increase of system's loading is less than the case of no UPFC. Using the second located UPFC, the voltage stability margin has improved even more and the downward slope of the voltage profile is lessened compared to the systems with no or one UPFC. According to the analyses done on the voltage profile of the two systems, the impact of the located UPFCs on improvement of the power system voltage stability margin was proved.

References

1. Kundur. Pai,Power System Stability and Control, McGraw Hill, 1994.
2. Prof.C.Udhaya Shankar, Nimmi Sreedharan, Dr.Rani Thottungal , "Stability Enhancement of Electrical Power System By Optimal Placement of UPFC",International Journal of Advanced Engineering Research and Studies,India,pp.146-151,March 2012.
3. Husan I.Shaheen, Ghamgeen I,Rashed, S.J. Cheng, "Optimal Location and Parameter setting of UPFC for Enhancing Power System Security Based on Differential Evolution Algorithm",ELSEVIER Electrical Power and Energy Systems, p.p.94-105, 2011.
4. M.Saravan ,S.Mary Raja Slochanal, P.Venkatesh, J.Prince Stephen Abraham, "Applocation of Particle Swarm Optimization Techniqe for Optimal Location of FACTS Devices Considering Cost of Installation and System Loadability", ScienceDirect Electric Power Systems Research, pp.276-283, 2007.
5. S. A. Taher, M.K. Amooshahi, "Optimal Placement of UPFC in Power Systems Using IMMUNE Algorithm", ELSEVIER Simulation Modelling Particle and Theory, p.p.1399-1412, 2011.
6. H.I. Sheen, G.I Rashed, S.J. Cheng, "Application and Comparison of Computational Intelligence Technies for Optimal Location and Parameter Setting of UPFC", ELSEVIER Engineering Applications of Artificial Intelligence, p.p.203-216, 2010.
7. T.Nireekshana, Dr.G.Kesava Rao, Dr.S.Siva Naga Raju, "Incorparation of Unified Power Flow Controller Model for Optimal Placement using Particle Swarm Optimization Technique" , IEEE Electronics Computer Technology,pp. 209-214, 2011.
8. R.Jabani, A.Safari, J.Olamaei, H.A. Shayanfar, "Using A New Hybrid Method for Optimal Placement of Unified Power Flow Controller in Power System", International Journal of Electrical and Power Engineering, p.p.169-176, 2010.
9. S.N.Singh,A.K.David,"A New Approach for Placement of Facts Devices in Open Power Markers", IEEE Power Engineering Review, September 2001.
10.J.G.Singh,S.C.Srivastava,"Enhancement of Power System Security through Optimal Placement of TCSC and UPFC",IEEE Power Engineering Society General Meeting,pp1-6, 2007.
11.R.W. Chang ,T.Kuo,T.K.Saha,"Mixed-Integer Method for Optimal UPFC Placement based on Line Flow-Based Equations ", IEEE Universities Power Engineering Conference (AUPEC) ,pp1-6،2010.
12.Sreekanth Reddy Donapati , M.K.Verma , " An Approach for Optimal Placement of UPFC to Enhance Voltage Stability Margin under Contingencies" , Fifteenth National Power System Conference(NPSC), IIT Bombay, pp 541-546, December 2008.
13.Hadi Saadat, "Power System Analysis", 2006.