MPSO BASED DG AND CAPACITOR PLACEMENT FOR LOSS REDUCTION

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Abstract

Optimal placement of DG and capacitors has been proposed in this work. This paper describes an effective Modified Particle Swarm Optimization (MPSO) approach to determine optimal placement and sizing of DG and capacitors in distribution systems for sake of enhancement in voltage profile and power loss reduction. Here seven different cases are considered and the results are validated on IEEE-34 and IEEE-69 bus distribution test systems and discussed in detail. The result shows that the placement of DG and capacitor will effectively improve voltage profile and reduces power loss in the system.

Key words: *Distributed Generation (DG), Radial Distribution System (RDS), Modified Particle Swarm Optimization (MPSO), Optimal Placement and Sizing.*

1. Introduction

In recent years, due to rapid growth in population and industries there is a deficit of power to the consumers, even in such scenario 13% of total generated power is wasted as I^2R loss in distribution network level [1, 2]. Majority of the distribution systems are having inductive loads, this leads to lagging power factor, hence the system voltage will be poor and the system power loss is more. In order to overcome the above glitches it is required to use compensating devices in the network which boosts the voltage level to the acceptable limits and also helps to minimize the system power loss. Also, Introduction of DG in the system will take care extra load in the network, as the load demand in the network is increasing. DG is also known as dispersed generation [3, 4], which is usually generated in small scale near to the load centers.

Now a days renewable DG's like solar, wind etc. are becoming more predominant because of its eco-friendly nature. DG and capacitor placement in the distribution system has proven that it will increase voltage stability and improves the performance of the network by reducing losses [5-7]. Proper care should be taken while placing the DG and capacitor in the network, otherwise it leads to further increase in voltage drop and power loss that will leads to poor system quality and poor reliability of the network. Many researches have been carried out in placing capacitors and DG's optimally in the distribution network.

Few researchers use classical method for placement of capacitor in distributed system [8-10]. Mohamed Imran A et al. presented Bacterial Forging optimization technique for multiple DG placements in distribution network [11]. Khodr HM et al. presented Mixed Integer linear optimization algorithm for sizing and optimal placement of shunt capacitors in distributed system [12]. Genetic Algorithm based approach [13-16] has been presented in order to obtain proper sizing and placement of capacitors for loss reduction. Oliveira LW et al. [17] presented MINLP approach for placement of switched capacitor in radial distribution system. Prakash K et al [18] used PSO method for finding optimal sizing and placement of capacitor for loss reduction. Improved Analytical (IA) approach was developed for finding ideal size and location of DG in [19, 20]. Artificial Neural Network (ANN) based method was presented in [21] to find size and best location of DG. B. Sravan Kumar, et.al [22] used Harmony Search Algorithm approach for optimal placement of unified power flow controller for loss minimization and voltage profile improvement.

The present work is intended to develop an algorithm to find optimal place and size of DG's and capacitors for various cases considering loss minimization and enhancement in voltage profile as objectives.

2. Problem formulation

The objective defined is minimizing power loss in the distribution network by placing capacitors and DG optimally subject to the constraints mentioned

Nomenclature

P_p	Real power at bus p.	ω_{min} ω_{max}	Initial and final value of inertia weight.
Q_p	Reactive power at bus p.	C	constraint co-efficient
R_p	Resistance at bus p.	C_1 , C_2	Weighing co-efficient.
X_p	Reactance at bus p.	$rand_1$ $rand_2$	Random numbers between [0, 1].
V_p	Voltage at bus p.	S_p	Current searching point.
V_{min}	Minimum voltage (0.9 p.u.)	S_{p+1}	Modified searching point.
V_{max}	Minimum voltage (1.05 p.u.)	V_p	Current velocity.
I_p	Line current at bus p.	V_{p+1}	Modified velocity.
I_L	Load current at bus p.	ω	Weighing function.
P_{DG}	Real power generation of DG.	δ	Constriction factor.
Q_{cap}	Reactive power generated by capacitor.	P_{best} G_{best}	Local and Global best of each particle.
$P_{total\ loss}$	Total power loss in the system.	$\emptyset$, $\emptyset_1$	Acceleration co-efficient limits.

in the equations (2), (3) and (4).

Objective function: - $\text{Min } F = \min(P_{Total\ loss})$ (1)

Subject to the following operating constraints:
Voltage limits:

$$V_{min} \leq V \leq V_{max} \quad (2)$$

Real power limits for DG:

$$0 \leq P_{DG} \leq P_{load} \quad (3)$$

Reactive power compensation limits for capacitor:

$$0 \leq Q_{cap} \leq Q_{load} \quad (4)$$

3. Power flow calculations

Load flow analysis is done by using forward backward sweep method [23] and power flow calculations are carried out by the following sets of equations given below, derived from the diagram shown in fig.1.

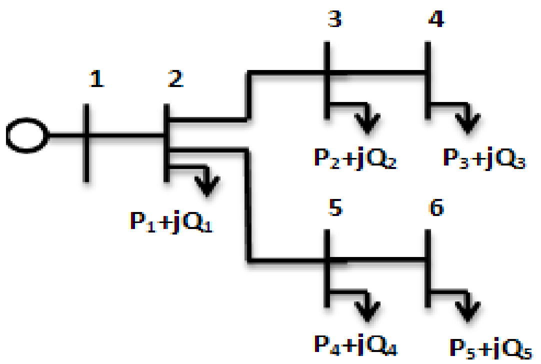

Fig.1. Simple radial distribution network.

Load current can be calculated by using equation (5):

$$I_L = \left[\frac{P_L + jQ_L}{V_P}\right]^* \quad (5)$$

Line current can be calculated by using equation (6):

$$I_P = I_{p-1} - I_L \quad (6)$$

Bus voltage can be calculated by using equation (7):

$$V_{p+1} = V_p - I_p * (R_p + jX_p) \quad (7)$$

Real and reactive power losses in the line are calculated by using equations (8) and (9):

$$P_{loss}(p+1) = \left[\frac{P_p^2 + Q_p^2}{|V_p^2|}\right] * R_p \quad (8)$$

$$Q_{loss}(p+1) = \left[\frac{P_p^2 + Q_p^2}{|V_p^2|}\right] * X_p \quad (9)$$

Total active and reactive power losses are calculated by summing all the respective losses in the line of the feeders and it is given in equations (10) and (11):

$$P_{Total\ loss} = \sum P_{loss}(p+1) \quad (10)$$

$$Q_{Total\ loss} = \sum Q_{loss}(p+1) \quad (11)$$

4. Particle Swarm Optimization (PSO)

PSO is an intelligence algorithm based on population called swarm and it is first introduced by Eberhart and Kennedy [24]. Swarm consist a group of individuals called particles and each particle moves in N-dimensional search space with randomly generated velocity. Each particles position and velocity is updated by using below equations (12) and (13):

$$V_{p+1} = \begin{bmatrix} \omega V_p + C_1 rand_1 * (P_{best} - S_p) \\ +C_2 rand_2 * (G_{best} - S_p) \end{bmatrix} \quad (12)$$

$$S_{p+1} = S_p + V_{p+1} \quad (13)$$

Where

$$\omega = \omega_{max} - \frac{(\omega_{max} - \omega_{min}) * \text{current generation number}}{\text{Maximum generation number}} \quad (14)$$

Where $\omega_{min} = 0.9$ $\omega_{max} = 0.04$.
$C_1, C_2 = 2$

4.1. Modified Particle Swarm Optimization (MPSO)

The above generalized velocity equation (12) and position updating equation (13) are modified as given in equations (15) and (16) to improve the solution [25, 26].

$$V_{p+1} = C * \begin{bmatrix} \omega V_p + C_1 rand_1 * (P_{best} - S_p) \\ +C_2 rand_2 * (G_{best} - S_p) \end{bmatrix} \quad (15)$$

$$S_{p+1} = S_p + \delta V_{p+1} \quad (16)$$

Where $c = \frac{2}{(2-\emptyset-\emptyset_1)}$, $\emptyset_1 = \sqrt{(\emptyset^2 - 4\emptyset)}$ and $\delta = 0.729$

Fig.2. shows the flow chart of the proposed algorithm.

5. Simulation results and Discussions

The effectiveness of the proposed algorithm is tested on IEEE-34 bus test system with load of 4.63 MW and 2.87 MVAr [27] and IEEE-69 with load of 3.79 MW and 2.69 MVAr [28]. The base voltage is 11 kV for IEEE-34 and12.6 kV IEEE-69 system and base power is 100 MVA for both the systems. Both systems are studied with different cases:-

Case 1: Without DG and Capacitor.
Case 2: System with single Capacitor.
Case 3: System with Multiple Capacitors.
Case 4: System with single DG with unity power factor.
Case 5: System with Multiple DG with unity power factor.
Case 6: System with single DG and single Capacitor.
Case 7: System with Multiple DG and Multiple Capacitors.

Coding has been done in MATLAB domain to run load flow, calculate losses and to determine optimal placement and sizing of capacitor and DG.

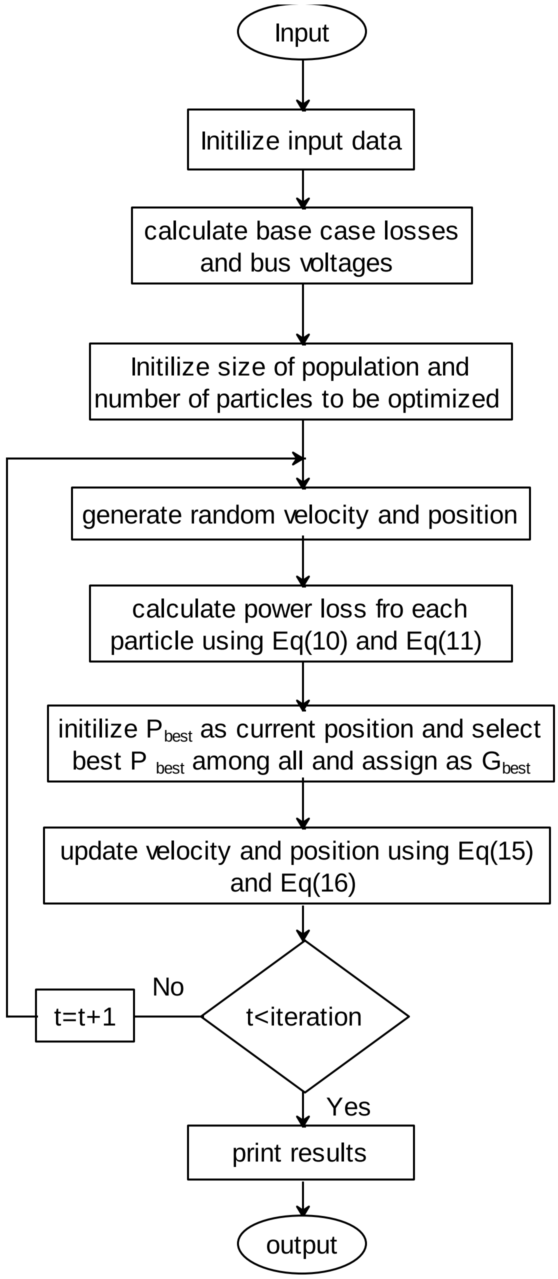

Fig.2. Flow chart of proposed algorithm.

5.1. Test System 1: IEEE-34 bus radial distribution system.

Case 1: Base case losses obtained are 221.67 kW and

65.1 kVAr and minimum voltage is 0.9417 pu.
Case 2: Single capacitor of size 1795.1 kVAr at bus number 21 reduces power loss to 173.36 kW.
Case 3: Optimal placement for multiple capacitors are obtained at buses 24, 19 and 9 with sizes 749.7 kVAr, 943.2 kVAr and 1615.1 kVAr will reduces the power loss by 27.55%.
Case 4: Single DG at bus 21 with size 2966.5 kW yields 93.74 kW power losses.
Case 5: DG's at buses 9, 26 and 20 with sizes 1278.6 kW, 917.6 kW and 1615.1 kW yields 71.43% reduction in power loss.
Case 6: 75.37% reduction in power loss is obtained when a single DG and capacitor is connected at buses 21 and 6 respectively with sizes 2955 kW and 2535.9 kVAr.
Case 7: Optimal places obtained are buses 9, 21 and 26 for DG's with size 1311.4 kW, 952.2 kW and 930 kW respectively and buses 8, 5 and 24 with sizes 1065.9 kVAr, 530.5 kVAr and 930.8 kVAr respectively. Figure 3 shows voltage profile and Table 1 discuss in detail about the performance of the suggested method for different cases on IEEE-34 bus radial distribution test system.

Table 1:
Performance analysis of the proposed algorithm on IEEE-34 bus system.

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7
DG size kW (Bus)				2966.5(21)	1278.6 (9) 917.6 (26) 1615.1(20)	2955(21)	1311.4(9) 952.2(21) 930.0(26)
Capacitor size kVAr (Bus)		1795.1(21)	749.7(24) 943.2(19) 881.4 (9)			2535.9(6)	1065.9(8) 530.5(5) 930.8(24)
Ploss (kW)	221.67	173.36	160.6	93.74	63.33	54.6	13.27
% reduction in Ploss		21.793	27.55	57.71	71.43	75.37	94.01
Qloss (kVAr)	65.1	50.05	46.96	25.33	18.29	12.53	3.56
% reduction in Qloss		23.11	27.86	61.09	71.90	80.75	94.53
V_{min} (p.u)	0.9417	0.9490	0.9506	0.9778	0.9908	0.9826	0.9921
V_{max} (p.u)	1.0000	1.0000	1.0000	1.0000	1.0000	1.0000	1.0000

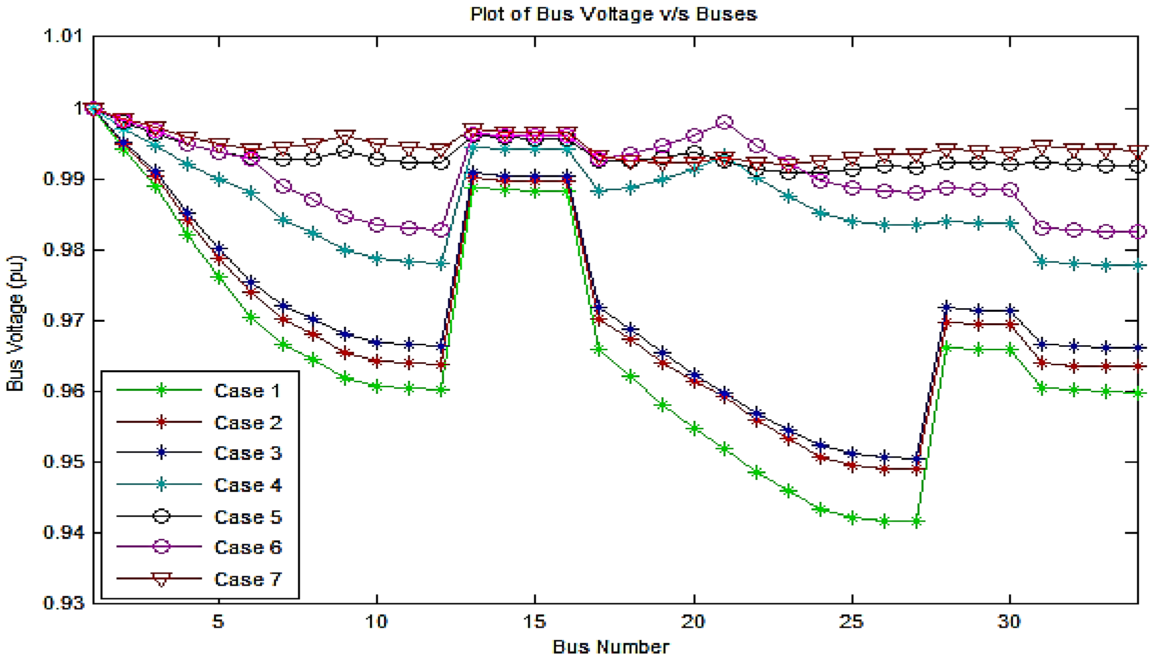

Fig. 3. Voltage profile for IEEE-34 bus system.

5.2. Test System 2: IEEE-69 bus radial distribution system.

Case 1: The total real and reactive power losses obtained are 224.92 kW and 102.13 kVAr respectively and minimum voltage is 0.9092 pu.
Case 2: After placing a single capacitor of size 1329.8 kVAr optimally at bus number 61, the losses are reduced to 151.91 kW and 70.44 kVAr and minimum voltage obtained is 0.9308 pu.
Case 3: Optimally placing multiple capacitors will result in 35.35% and 33.63% reduction in real and reactive power losses. Optimal placements for capacitors obtained are bus numbers 18, 12 and 61 with sizes 302.4 kVAr, 196.6 kVAr and 1277.1 kVAr respectively.
Case 4: Single DG at bus 61 with size 1872.5 kW yields 83.17 kW power losses.
Case 5: DG's at buses 11, 18 and 61 with sizes 501.2 kW, 482.2 kW and 1770.4 kW yields 68.92% reduction in power loss.
Case 6: 89.65% reduction in power loss is obtained when a single DG and capacitor is connected at buses 61 with sizes 1859.4 kW and 1357.2 kVAr.
Case 7: Placing multi DG and capacitors simultaneous yields 95.03 % reduction in power loss and optimal placement obtained are buses 62, 5 and 16 for DG's and buses 62, 13 and 47 for capacitors. Figure 4 shows voltage profile and Table 2 discuss in detail about the performance of the proposed method for different cases on IEEE-69 bus radial distribution test system.

Table 2:
Performance analysis of the proposed algorithm on IEEE-69 bus system.

	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7
DG size kW (Bus)				1872.5 (61)	501.2 (11) 482.2 (18) 1770.4 (61)	1859.4(61)	1658.2 (62) 941.9 (5) 694.2 (16)
Capacitor size kVAr (Bus)		1329.8 (61)	302.4(18) 196.6(12) 1277.1(61)			1357.2(61)	1171.6 (62) 673.0 (13) 215.0 (47)
Ploss (kW)	224.92	151.91	145.39	83.17	69.89	23.27	11.17
% reduction in Ploss		32.46	35.35	63.02	68.92	89.65	95.03
Qloss (kVAr)	102.13	70.44	67.78	40.51	35.10	14.32	9.38
% reduction in Qloss		31.03	33.63	60.33	65.63	85.98	90.81
V_{min} (p.u)	0.9092	0.9308	0.9316	0.9683	0.9812	0.9729	0.9943
V_{max} (p.u)	1.0000	1.0000	1.0000	1.0000	1.0000	1.0015	1.0060

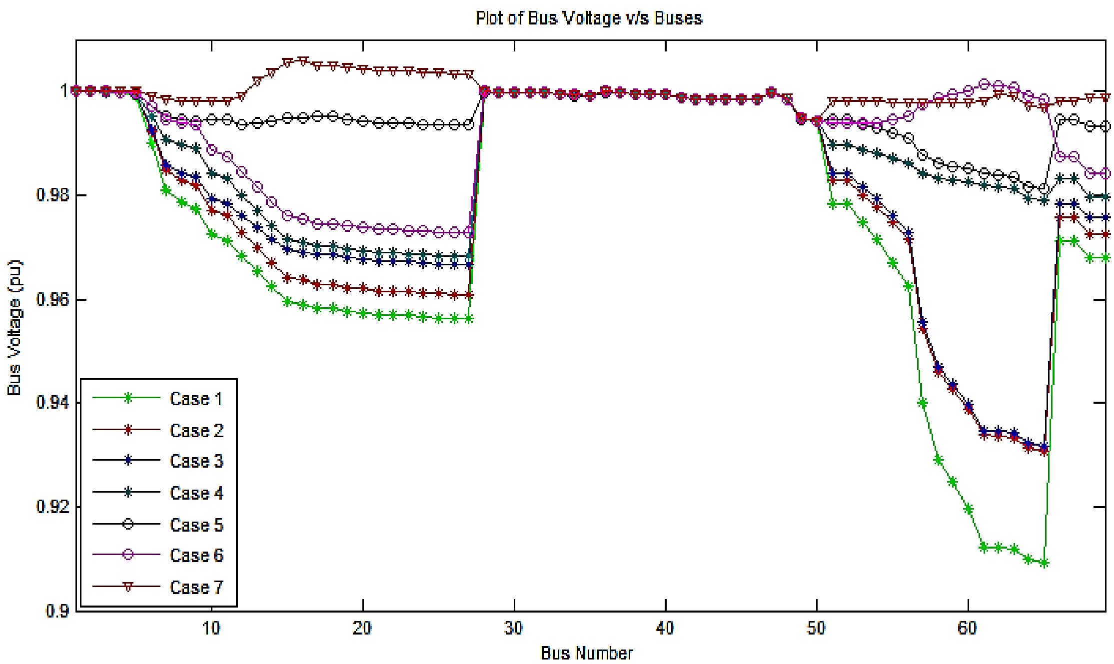

Fig. 4. Voltage profile for IEEE-69 bus system.

6. Conclusion

This paper presents an MPSO method for placement and sizing of DG and capacitors optimally in the distribution network for reduced power loss and voltage profile improvement. Two different test systems (IEEE-34 and IEEE-69) are considered with different cases to illustrate the effectiveness of the suggested algorithm and the result obtained shows that optimally placing DG and capacitor will reduce power loss, improves the voltage profile and also improves the voltages of tail end node in the system.

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