A Single-Phase T-Type Transformerless NPC- MLI for Grid-Connected PV Power System

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Abstract- Due to extraordinary aids, transformerless inverters (TLs) are shown significant developments with coupled inductor inverter concepts. Especially, transformerless inverter (TLI) topologies have given much interest in photo-voltaic (PV) power generation system (PGS) as it had high efficiency and less installation cost. This TLI highly suffered with leakage current flow through the ground path and the inverter power circuit. Hence, the TLI had a shoot-through (ST) problem in the inverter bridge legs and hence leakage current in the inverter should be suppressed through via their freewheeling or overwhelming conduction path. Neutral- point clamped -multilevel inverter (NCP-MLI) topologies based TLI design is being immensely used in PV PGS due to its enhanced performance as compared to two-level voltage source inverter. In NPC-MLI topology, compere to "I" type, "T" type has a great compatibility, since it is free from clamping diodes. Hence, in this paper a TL-"T" type NPC-MLI is developed and investigated for PV grid connected applications. The proposed inverter model, modes of operation and control for PV tie system is presented. The MATBAL/Simulink based software simulation study and FPGA based 1.5kW, 2kW PV tied laboratory scale experimental results study show that the proposed "T-type" TL NPC-MLI attains high efficiency operation for PV input, and parades leakage currents reductions, and fulfills the TL topology regulations and norms. The proposed "T-type" TL NPC-MLI topology confirms the zero common-mode voltage (CMV), near zero leakage-current and ST encumbrances, which are make sure the inverter fitting for the PV TL inverter market needs and consumer demands.

***Keywords*: Photovoltaic (PV) system; Neutral point Multilevel inverter (NP-MLI); Transformerless T-type Neutral-Point Multilevel inverter (TL-TNP-MLI; hysteresis current control (HCC), PV tied grid connected system.**

I. INTRODUCTION[1]

Renewable energy sources (RES), such as hydroelectricity, biomass, wind power, wave energy, and photo-voltaic(PV) power are a present asset for the electric power generation with zero CO_2 emissions. Particular, PV and wind based power generations comprised roughly 15% of global energy consumption in 2017 [1]. The world PV plant installed capacity is over 430 GW, and is increasing at a rate of 24% per year to year. Amongst the sources that use renewable-energy, photo-voltaic based power generation systems have involved the superlative interest, since of their dependability and comfort of right to use. The technology is being attractive for the PV tied PGS. Next to PV panels design and installation, the inverters are placed a direct role to strategy the cost factor and sizing for the PV plant. The two-level inverter is normally recommended for conventional PV system and the generated PV panels DC-power converted through AC-power through inverter and connected to local utility load or grid via transformer. Considering any typical PV-based PGS layout, it consist of the solar panels, DC to DC converters and DC to AC inverters), and interfacing controllers such as maximum power point tracker and current controllers [2]. Here, in PV modules generate earth parasitic capacitance and it has a range about 1-4μF/kW, between PV panels' modules and ground (G). As a result, in any PV system, when high frequency inverter used means, it produces high-leakage current on the PV system [3]. To avoid these problems, the transfer used to connect between inverter and grid, which make isolation between inverter and grid. However, this method demands high space and cost. The importantly, sue to the transformer core losses; the efficiency of the system is not compatible.

Hence, the power electronics research is found solution to abolish the transformer through split inductor connecting in the inverter output side and make inverter to produce sine mode output voltage [4]. Nevertheless, the burden of these method is it had leakage-current problem due to the split inductors [5]. This leakage-current affect the system reliability and efficiency. Additionally, the leakage current causes the EMI issues and electric hazard to humans. Therefore, this leakage-current problem is a huge human's safety risk. Thus, the German establishes a standard – DIN-VDE-0126-1-1 for the PV plant leakage current premises. According to that, it should not exceed 300 mA [6].Another essential factor is for the PV inverter is efficiency, which is expected near around 98% [7]. Further increase of 1%, the researchers are improving the switching characteristics of the power semiconductor switch and soft-switching technologies, which can reduce the conduction and switching losses of the switching devices.

Neutral- point clamped -multilevel inverter (NCP-MLI) topologies based TLI design is being immensely used in PV

PGS due to its enhanced performance as compared to two-level voltage source inverter. In NPC-MLI topology, compere to "I" type, "T" type has a great compatibility, since it is free from clamping diodes. Hence, in this paper a TL-"T" type NPC-MLI is developed and investigated for PV grid connected applications. In [8] Xiao *et.al* examined the exhaustive analytical-model of leakage-current for single-phase PV tied TLI. Followed by, Gonzalez *et.al*, modelled a single-phase NPC-MLI based TLI topology for mitigating the leakage-current system [9]. After, H-bridge-type, NPC-MLI topology with shoots-through options to hitch the leakage-current for appearance [10,32]. Nevertheless, in this topology operation the zero-vectors and non-zero vector switching vectors the current paths contain two-power devices. This creates a long current path, and hence it suffers with a high conduction loss, and stray inductance. The "I"- type NPC_NMLI used by Bharatiraja *et.al* with innovative control algorithm. However, this topology uses clamping diodes and diodes are used, when zero-vector is used. As results, even though this method has an accepted one, due to the larger reverse recovery losses on the diode, the system efficiency is losing unnecessarily 2%. Instead, "I"–type NPC-MLI another inverter called "T"-type is compromising these 2% clamping diode losses, and it has studied by Schweitzer et.al, in [11] for the stand alone load. The same research results are arrived in [12] and this paper is valued the system performance in detail with hardware prototype with DC-link balancing [13].

Based on the above discussion, the "T"-type based transformerless inverter is a better choice for PV connected application. With this aim, the papers present the five-level single- phase "T"-type NPC-MLI tied PV. The paper presents the proposed inverter design and leakage-current mitigations and mode of operation. The proposed inverter model, modes of operation and control for PV tie system is presented. The MATBAL/Simulink based software simulation study and FPGA based 1.5kW, 2kW PV tied laboratory scale experimental results study show that the proposed "T-type" TL NPC-MLI attains high efficiency operation for PV input, and parades leakage currents reductions, and fulfills the TL topology regulations and norms. The proposed "T-type" TL NPC-MLI topology confirms the zero common-mode voltage (CMV), near zero leakage-current and ST encumbrances, which are make sure the inverter fitting for the PV TL inverter market needs and consumer demands..

II. ANALYSIS OF T- TYPE NPC-MLI

A. Single-phase transformerless T- TYPE NPC-MLI power circuit

The Fig. 1 shows the circuit of the proposed single-phase transformerless T- TYPE NPC-MLI. It is two legs A and B both has a high–voltage switch (1200V) and it is considered as H-bridge structure. The DC-link is connected with low – voltage (600V) bidirectional power switch for connecting the DC-link capacitors (C_1 and C_2) and mid pint (N). The leg-A and B is built with switch S_{A1} , $S_{A2,}$ and $S_{B1,}$ $S_{B2.}$ This allows generating multilevels with bidirectional switches. Two-antiparallel freewheeling-diodes (D_{C1}-D_{C2}) power switches (S_{C1}, and S_{C2}) is connected with DC-link capacitors. Unlike "I" type NPC-MLI, due to the lesser blocking-voltage, the switches, S_{C1} and S_{C2} experience very conduction losses and less switching, there is block the DC-link voltage V_{dc} [CBR].

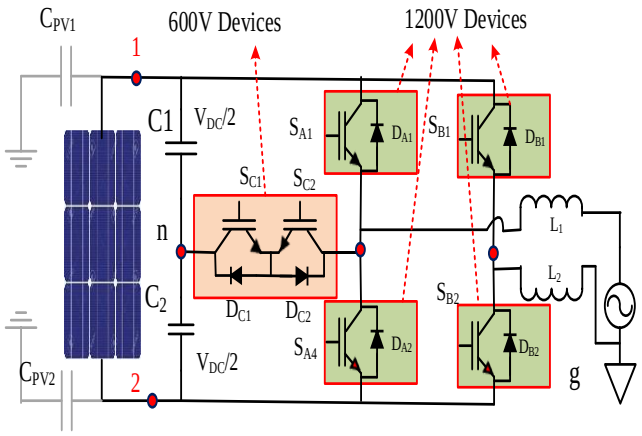

Fig.1. The PV tied power circuit of single-phase TL-TPC-MLI.

For considering the "T"-type NPC-MLI as a TLI, the front side of the inverter is connected PV panels with DC-link capacitors. The output side of the inverter H-bridge is connected with split inductors, which is equal values of inductors (L_1 =L_2=L) and provide the sinusoidal current to the grid. The ground connection (G) is the essential one for any TL inverter topologies, while the center of PV cluster does not ground [14]. Hence, the DC-link capacitors mid-point (N) is connected to PV panels cluster midpoint.

B. Modes of operation proposed single-phase transformerless T- TYPE NPC-MLI:

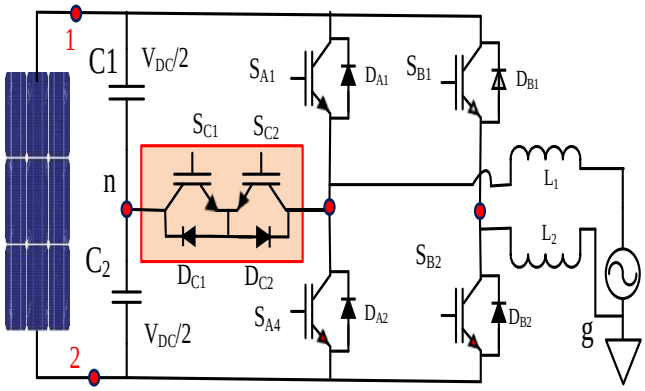

Fig.2. power circuit of single-phase TL-TPC-MLI.

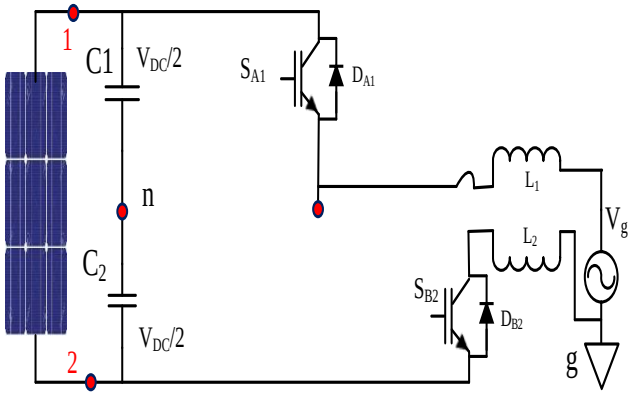

Fig. 3. Single-phase TL-TPC-MLI operation mode-1: $V_O = V_{PV}$

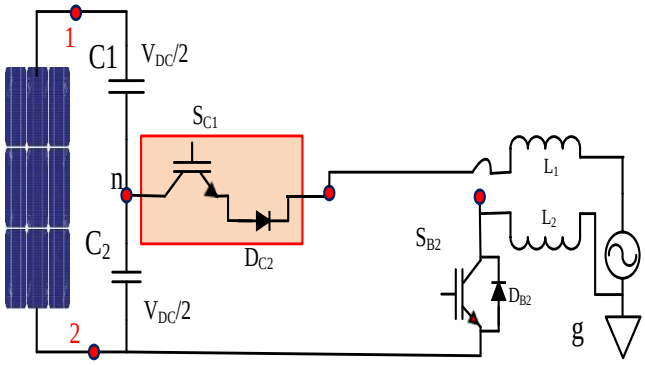

Fig. 4. Single-phase TL-TPC-MLI operation mode-2: $V_O = V_{PV}/2$

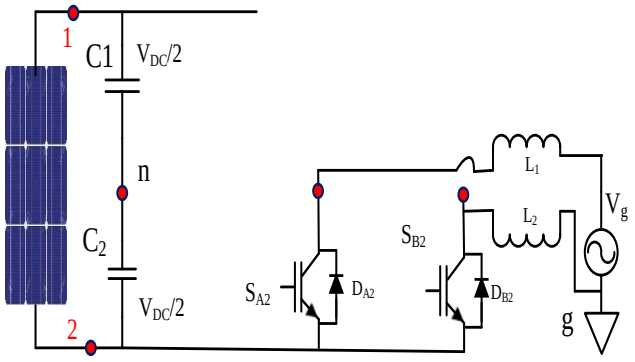

Fig. 5. Single-phase TL-TPC-MLI operation mode-3: freewheeling the leakage current

Proposed TL-TPC-MLI shown in the Table-1. According to the mode of operations, the inverter producing the V_{DC} and $-V_{DC}$ and zero voltage, such a way to produce five-level output in the inverter output side. The inverter mode-3 and mode-6 are operating as a freewheeling mode and suppressing the inductor leakage current via circuit power switches itself. Hence, the inverter free from leakage current and protecting the PV panels. The equivalent circuit of common-mode voltage (CMV) proposed TLI is illustrated in Fig.2

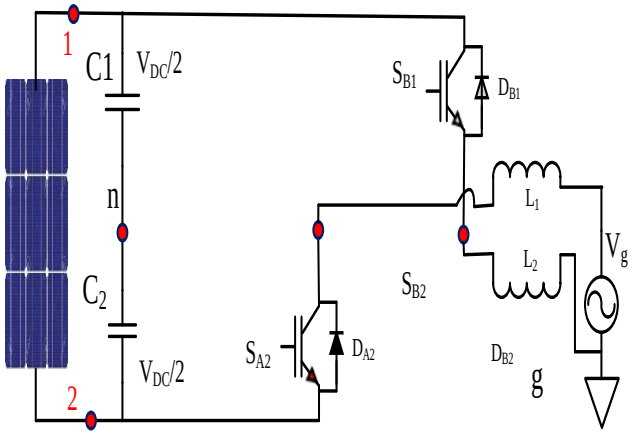

Fig. 6. Single-phase TL-TPC-MLI operation mode-4: $V_O = V_{PV}$

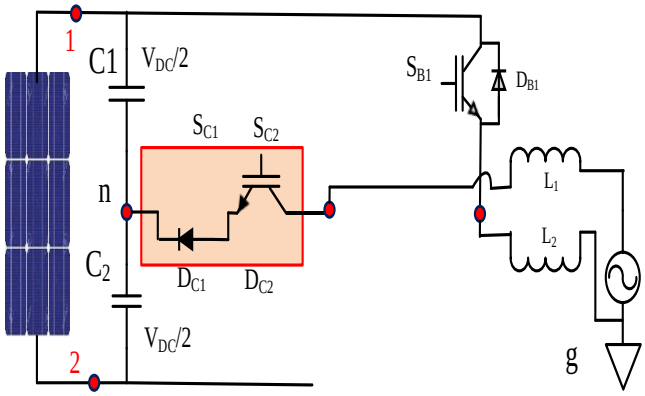

Fig. 7. Single-phase TL-TPC-MLI operation mode-5: $V_O = V_{PV}$

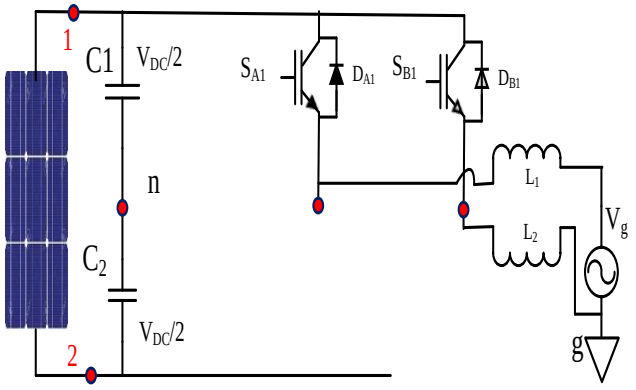

Fig. 8. Single-phase TL-TPC-MLI operation mode-6: freewheeling the leakage current

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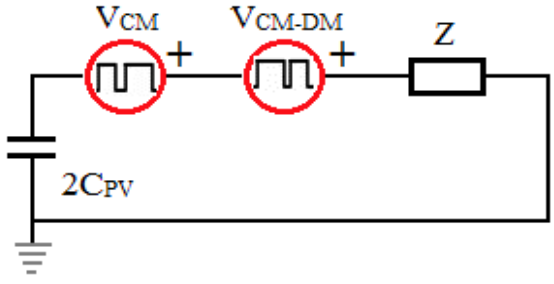


Fig. 9. CMV equivalent circuit of proposed TLI

Here, the DMV-V_{DM} to CMV-V_{CM} influence by V_{CDM}, is equal to -V_{DM}/2.

$$V_{CDM} = \frac{V_{DM}}{2} \quad (1)$$

During positive half-cycle

$$V_{CDM} = \frac{V_{A1} + V_{C1}}{2} \quad (2)$$

$$V_{DM} = V_{A1} - V_{C1} \quad (3)$$

During negative half-cycle

$$V_{CM} = \frac{V_{B1} + V_{C1}}{2} \quad (4)$$

$$V_{DM} = V_{B1} - V_{C1} \quad (5)$$

The total CMV including V_{CM-DM}

$$V_{TCM} = V_{CM} + V_{CDM} \quad (6)$$

TABLE 1
Mode of operation for proposed TLI

Mode of operation	Switches Involved	Inverter output, V_o
Mode-1	V_{PV}	V_{PV}
Mode-2	S_{C1},S_{B2}	$V_{PV}/2$
Mode-3	S_{A2},S_{B2}	V_o =0 ; freewheeling the leakage current
Mode-4	S_{A2},S_{B1}	-V_{PV}
Mode-5	S_{C2},S_{B1}	-$V_{PV}/2$
Mode-6	S_{B1},S_{B2}	V_o =0; freewheeling the leakage current

The various possible switching operation of PV tied TL-TNP-MLI is investigated for the positive and negative half-cycle of the grid voltage as shown in Fig .3 to 8. Before going to the modes of operation, the following assumptions are made: (1) All IGBTs are considered as ideal devices; (2) DC-link capacitors are equally dividing the DC-link voltages; (C_1 = C_2 =$V_{PV}/2$),and 3) the TLI operates at the unity power factor (PF), i.e., the inverter current, (i_L) and grid voltage,(V_g) are in zero-degree phase-shift.

TABLE 2
Mode of operation for proposed TLI

Mode of operation	V_{DM}	V_{CM}	V_{TCM}
Mode-1	$V_{PV}/2$	$3V_{PV}/4$	$V_{PV}/4$
Mode-2	0	0	$V_{PV}/2$
Mode-3	0	0	0
Mode-4	-$V_{PV}/2$	-$3V_{PV}/4$	-$V_{PV}/4$
Mode-5	0	0	-$V_{PV}/2$
Mode-6	0	0	0

During the switching commutation mode operations, unlike 'I-type' NPC-MLI, there are no "short -commutation" or "long commutation" commutation paths for 'T-type' TNP-MLI topology; all paths are having same geometric length and inherit one outer-switch and two inner -switches In normal mode operations, the 'T-type' TNP-MLI topology affects outer and inner switches. The commutation mode is represented in the Table-III.

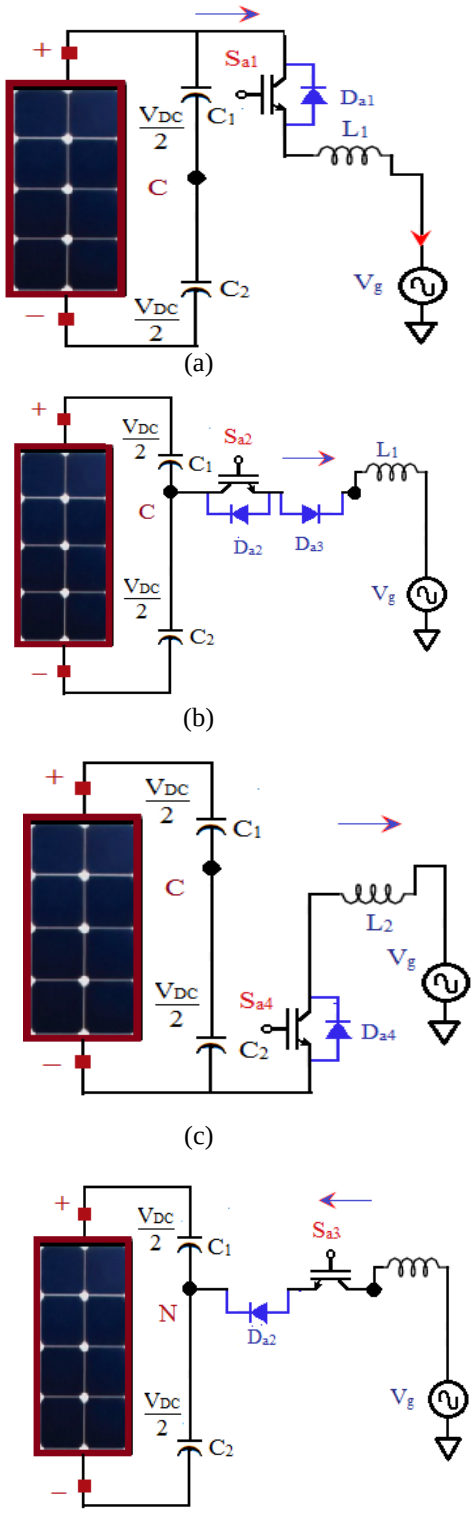


Fig.10. Mode of operation of TL-TNP-MLI.

TABLE 3
COMMUTATION INTERVAL, VOLTAGE AND CURRENT PATH FOR TNP-MLI

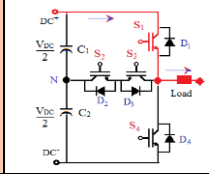
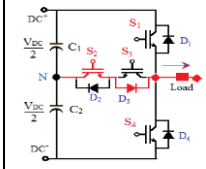
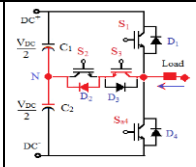
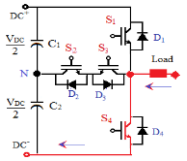
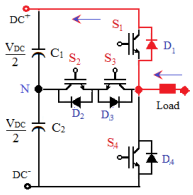
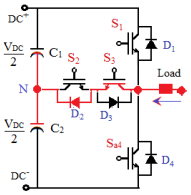
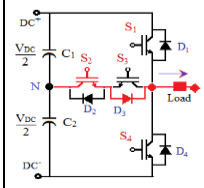
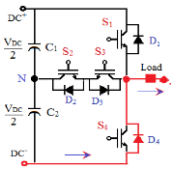
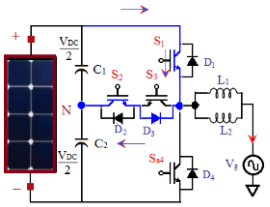
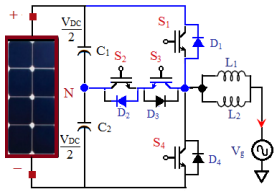
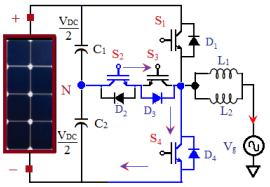
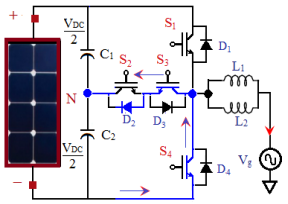
Mode of operation	Grid reference - 0 to 180^0		Grid reference - 180^0 to 360^0	
	$V_g = +V_{dc}/2$	$V_g = 0$	$V_g = +V_{dc}/2$	$V_g = +V_{dc}/2$
Inverting operational mode				
Rectifying operational mode				

TABLE 4
. COMMUTATION INTERVAL, VOLTAGE AND CURRENT PATH FOR TL-TNP-MLI

Mode of operation of single phase TNP-MLI	Positive voltage	Negative voltage
Positive current		
Negative current		

The proposed TLI providing voltage transition between their zero voltage to $+V_{PV}/2$ and zero voltage to zero $-V_{PV}/2$ according to positive half-cycle and negative half-cycle of the grid voltage, which diminishes the current ripple of the inductor naturally, and maintaining half and quarter symmetry and also its requires less inductance range compared to dual-buck half-bridge inverter [15]. Besides, form the common-mode voltage generation in table-3, the proposed MLI topology maintains the common-mode voltage constant in their every mode operation. Hence, leakage current suppression is uniform in the positive and negative freewheeling mode. This benefit comes about since the MLI topology structure naturally produces less CMV compared to other inverters [16,17]

III. Control strategies for proposed TLI with grid

From the section-1 discussion, the proposed TLI is a good choice for using the PV died grid interface. However, in order to ensure the grid interface and current quality improvement, the inverter need to control through the control circuit with grid voltage and frequency variations. In this work, the current control method is used using hysteresis current controller for improving the current and grid interfacing. In this section, the proposed current controller strategies and its function with close loop grid connected PV tied TLI.

C. Hysteresis current control (HCC)

The HCCs are the unique current control method for gird connected system, where the reference current and actual current compared and operated with in the given fixed or

variable frequency band [18]. Fig. 11 displays the structure block diagram of HCC. Here, the reference current, i_{ref} is associated with the actual current i_{act} to create the error current, $(\vec{\varepsilon_i}) = (i_{Lref} - i_{Lact})$, which will produce the error gain (control input u (t)) between two hysteresis bands BU and UL (upper and lower hysteresis bands) [15]. This control input *u(t)* drives the PWM block to give the perfect interface between inverter and grid. The challenge here is to retain the actual load current near to the reference load current within the hysteresis boundaries .

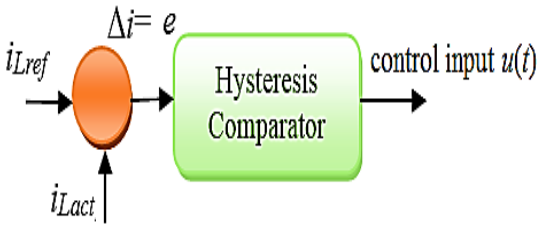


Fig.11 basic block diagram of Hysteresis current control

D. Closed loop PV tie grid connected control strategy of proposed TL-T-MLI

To ensure that, the proposed grid connected TL-TNP-MLI interface is investigated with HCC to confirm zero i_L (inverter current) sooner than the zero crossing of the grid voltage 'V_g'. Here high frequency inverter pulses are stopped in the inverter switching to avert the shoot through hitch. Fig.12 illustrates the hysteresis switching assortment for the proposed HCC. Based on the slit inductor current and reference current with in the inductor current upper (iL1) and lower limit (iL1) current boundaries. According to the gird current frequency and bandwidth of hysteresis current control (H), inverter high switching frequency is floating and given to the inverter [15].

The hysteresis current control, H values is generated though PV output, gird voltage, inductor values and switching frequency. For a fixed frequency, f_s , the H bandwidth of HCC is calculated as ,

$$H = \frac{V_g(V_{PV}-2.V_g)}{V_{PV}.L.f_s} \qquad (7)$$

Here, the inductor value is related to the inverter and PV power carrying capacity. The design method is considering a fast dynamic response. On the other hand, due to the unfixed switching frequency, the output current is widely distributed in the energy of spread-spectrum [33].

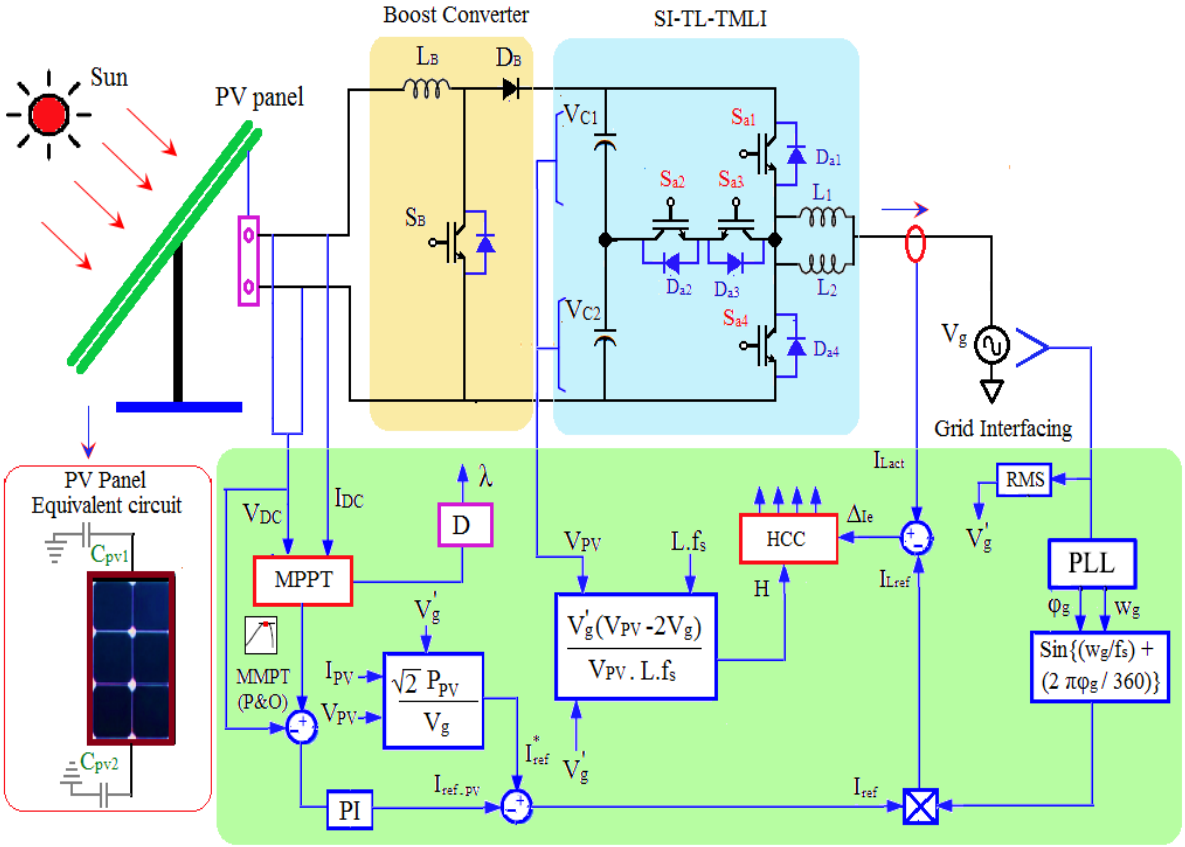


Fig.12 closed loop PV tied grid connected single-phase TLI

The Fig.12 shows the closed loop PV tied grid connected single-phase TLI. The proposed PV, grid interface closed loop control system consists of four main parts, which are; PV side converter, single-phase TLI, HCC, grid side measurement unit. The PV panel is directly connected to the inverter DC-link and the V_{PV} and I_{PV} are measured using voltage and current sensors. The P&O technique based MPPT is used for calculating the maximum power-point location and capturing the V_{PV} giving to the PV side control system and generating the current reference. The current reference, I_{ref}* is given to comparator for comparing the grid reference current to calculate HCC band. In the grid side, the PLL is measuring the grid angle, Θ_g and utility grid nominal operating frequency, f_o for the grid synchronization. The H values is measuring using Eq (7) and calculating the switching pulses for the inverter.

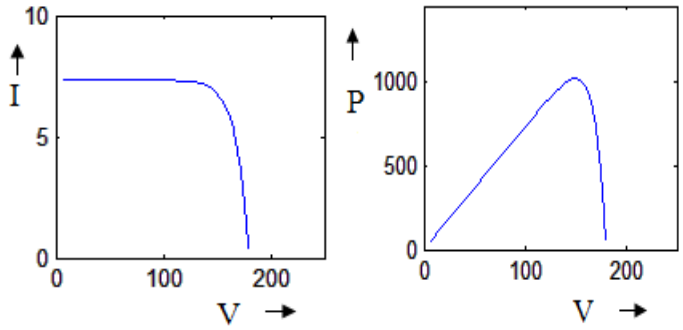
III. Simulation Study

To verify the proposed inverter with PV tied grid connected system. The inverter and the PV modules are modelled using MATLAB/Simulink. The buck-boost DC to DC connected to 1250W PV module and suppling the DC-link voltage to single-phase five level MLI. The other closed loop modules are modeled and interfaced with PWM controller. The Table-5 shows the simulation parameters for the proposed grid interface. The P&O MPPT is validated to give 250V DC supply to inverter DC-link to meet the grid voltage requirements.

TABLE 5
Simulation Parameters

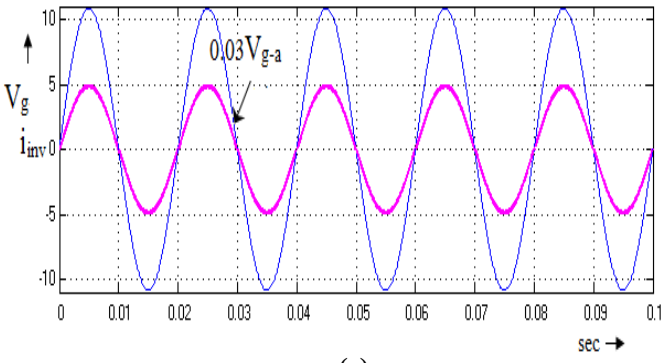
parameters	Values
PV module design/W	1250W
Grid voltage/V and grid frequency /Hz	250V/50Hz
Inverter power rating/W	1000W
DC-link capacitors (C_1 &C_2)/µF	470 µF/500V
Filter inductors (L1 & L2)/mH	4.4 mH
CM Capacitance (C_{Y1} & C_{Y2})/nF	2.8nF
Parasitic Capacitance, µF	0.25 µF

The Fig.13(a) and (b) show the PV panel module P-V and V- I curve receptively.



(a) (b)

Fig.13. PV characteristics; (a) P-V. (b) I-V.



(a)

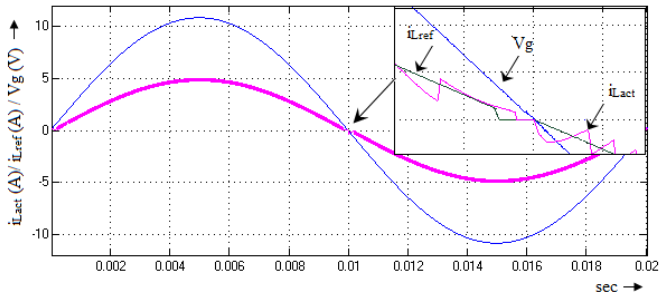


Fig. 14 (a) gird voltage and inverter current. (b). zoomed view on i_L verse V_g.

Fig. 14 (a) shows the gird voltage and inverter current. From the result is can see that, the inverter feeding the current to grid with zero -phase shift angle. When the grid voltage and inverter current are observing in zoomed view from the Fig.14 (b), it could see that, at zero crossing point the hysteresis current controller avoiding the high-frequency signal between grid voltage and inverter current meeting point. From this result, I could see that the inverter mitigating the leakage current. Fig. 915 illustrates the split inductor current also the Fig. 16 shows the inverter current (actual current), I_{Lact} and reference grid current, I_{Lref}. From the results, it is proven the actual current tracking with reference current. The Fig.17show the inverter leakage current. From the results, it is proven the leakage current is maintained as 0.3milliapms, which is 2 times lesser then the recommended leakage current value. By comparing with TL-NPC-TLI presented in [7, 19], the common-mode characteristics for the proposed TL-TNP-MLI could be the same.

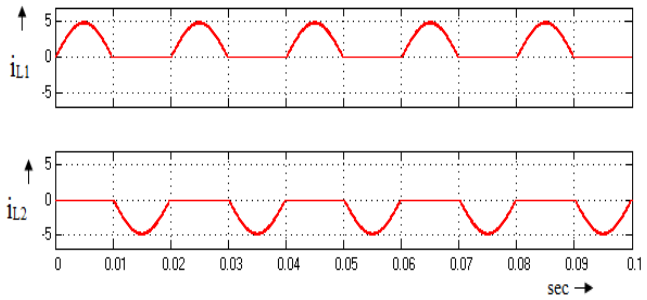


Fig. 15. Inductor current (i_{L1} and i_{L2}) of TLI

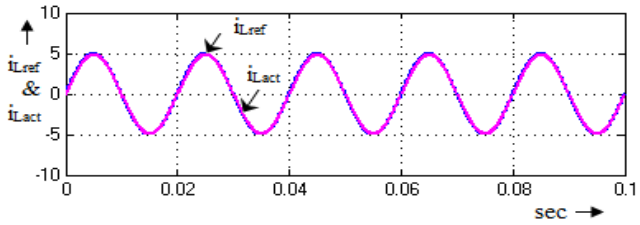


Fig. 16 actual current, and reference grid current

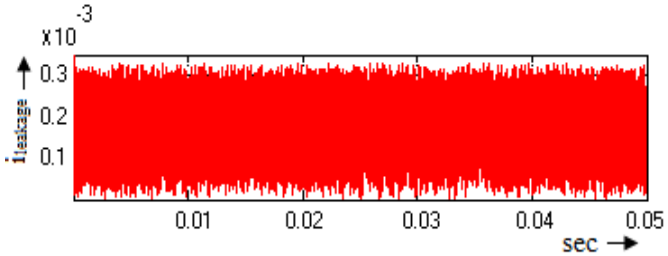


Fig.17 inverter leakage current.

Next, the simulation is performed for fixed and variable hysteresis band. The Fig.18 and Fig.19are showing the fixed and variable band HCC controlled inverter harmonics spectrum. The spectrums results are performed up to 500th harmonics order, since switching frequency of the inverter is 25kHz. From the spectrum it can see that, the proposed HCC controller is attainting the current harmonics to 5% for fixed frequency and 8% for variable frequency.

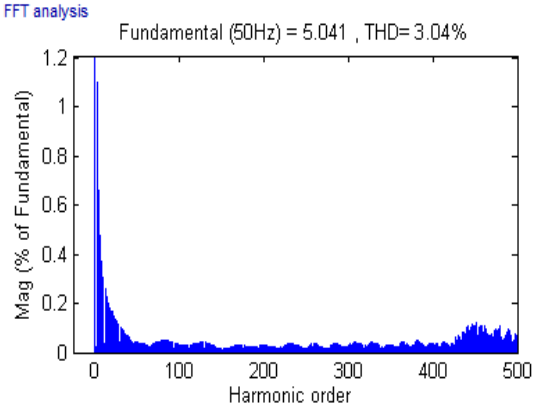


Fig.18 Fixed HCC controlled inverter harmonics spectrum.

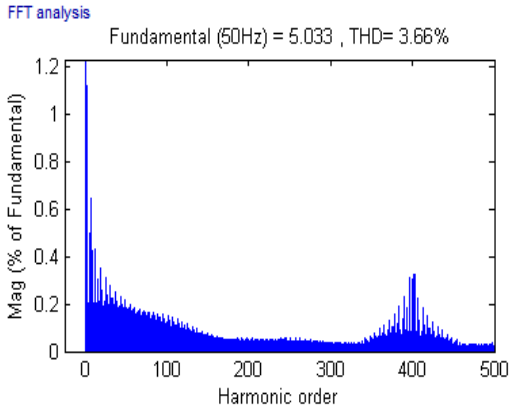
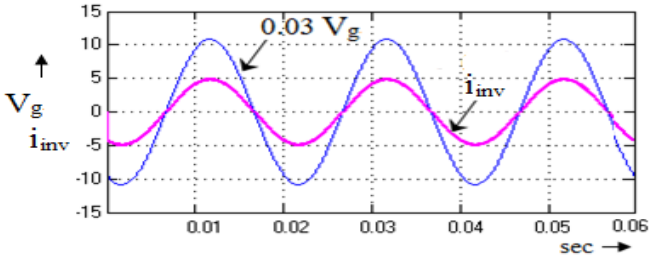
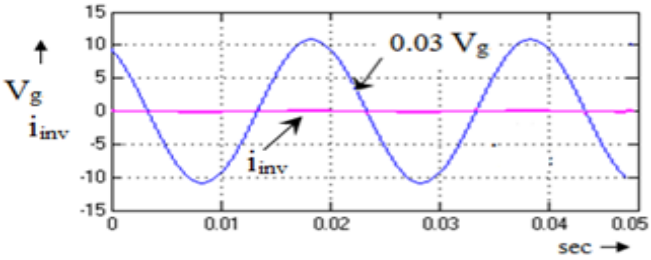


Fig.19 Variable band HCC controlled inverter harmonics spectrum.

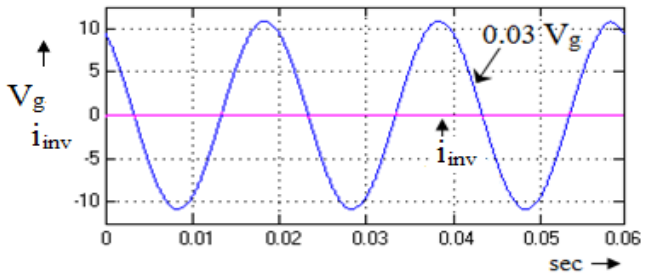
To vary the different steady state and transients condition, the proposed PV grid interface is tested for different PV and grid variations and the same conditions simulation results are showed in Fig. 20 From results iot can seen that the proposed controller is gave the turned OFF switcing signale to inverter , when there is no yeild in PV and isolating the inverter and grid, which secure the inverter and PV from the shgort citcuit issues.



(a)



(b)



(c)

Fig.20. Inverter performance under PV supping and landing conditions: (a) inverter feeding current to grid, (b) no inverter current, when there is no PV yield. (c) inverter is fully islanded.

To validate the proposed inverter efficiency, the invert is operated in it full range of operating rage (modulation index) and calculated efficiency versus the output power. The efficiency calculation is derived from paper [23], the inverter losses is calculated and plotted. Here, the calculated inverter efficiency is larger than simulated one (which is due to the unaccounted losses on cabling and screw resistances). Further measurements revealed additional loss components caused by cabling resistances (due to technical reasons, a four-wire measurement was not possible). If these extra losses are incorporated in this efficiency formula, then the calculated and measured

efficiencies confirm a good agreement. Next, the proposed MLI and other comparable inverters efficiency performance is considered with different switching frequency ranges from 2 kHz to 25 kHz and plotted in fig.21. Noteworthy the low-voltage application like PV-grid connected system, the proposed TNP-MLI is the best choice with respect to cost and efficiency. Fig. 22. Shows the Proposed inverter efficiency comparisons with other reported transformerless inverter

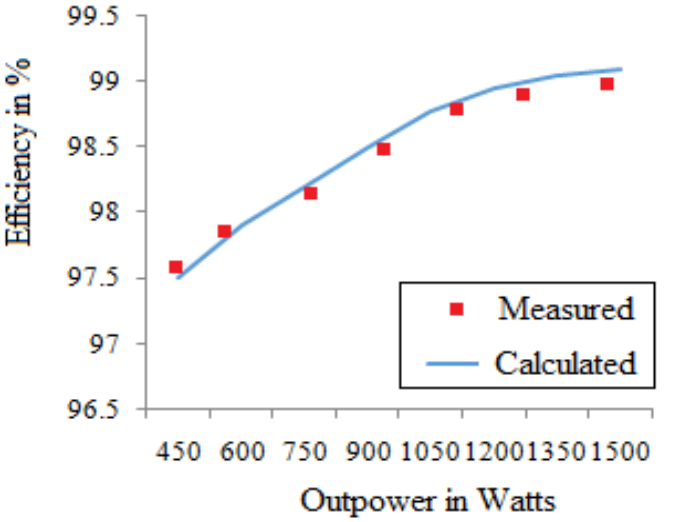


Fig. 21. Proposed inverter efficiency calculation for calculated and measured

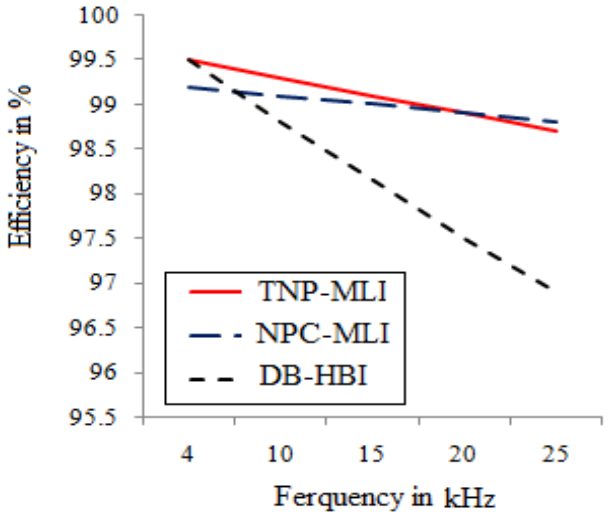


Fig. 22. Proposed inverter efficiency comparisons with other reported transformerless inverter topologies

IV. Experimental Study

A 1.5 kW Experimental inverter power module is designed for the PV tied grid connected systems. The inverter power module is uses the six power switches which are from IGBTCT60AM-18F. The experimental set is shown in the Fig.23.

The 2kW roof-top PV plane setup (250W*8=2.5kW) is used to provide a DC -link voltage for the inverter. The PV modules are connected with DC-DC boost converter with MMPT controller. The MMPT controller uses the voltage and current sensors to measure the V_{PV}, and I_{PV}. The inverter DC-link is split half of V_{DC} using two identical 330 µF/450 V DC-link capacitors. The inverter operating frequency is set as 40Hz to 60Hz and the inverters' switching frequency is chosen 25 kHz. The two-channel digital-oscilloscope Tektronix MDO4034B and four-channel YOKOGAWA-power analyzer.

Initially, the proposed TLI is validated with the full range of PV supply (1.5kW to 2kW) system and the DC to DC boost converter with PIC-microcontroller based MMPT controller is used to provide a constant 300V DC-link voltage to inverter. After the HCC and other grid interface control logic using field programmable gate array SPARTAN controller through MATLAB/Simulink system-generator [28,29]. All measured results are corresponding to digital oscilloscope (DSO)) Tektronix MDO4034B-3 and Yokogawa power analyzer.

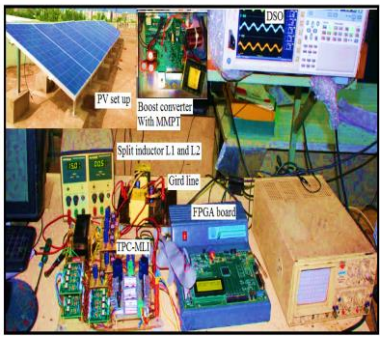


Fig. 23 Photo of the experimental model; (a) proposed FPGA-based PV tied grid connected TL- TNP-MLI

The Fig. 24 and 25 are specifies the TLI gate pulses of switches (S_1 and S_4) via Tektronix DSO. All the inverter pulses are continually monitored and verified for the reliable operation of the inverter. Fig. 25 illustrates the experimental waveforms of inverter voltage and current of PV tied grid-connected single-phase three-level TLI. Fig. 26 illustrates the experimental numerical harmonics value for inverter output voltage Fig. 28 illustrates the inverter voltage and current harmonic spectrum. Form the results it could see that the voltage and current %THD is maintained in the minimal value. The harmonic spectrum of is witnessed to be much similar to simulation value. Fig. 29 illustrates the TLI current, i_L and grid voltage, V_g. The Fig.30 show the inverter leakage-current. From the results, it is proven the leakage current is maintained as like simulation results as 0.3milliapms, which is 2 times lesser then the recommended leakage current value. To prove the grid voltage and inverter current synchronization, the Fig.29 results shows the grid voltage, *Vg* and inverter current, I_L in the same scope. From the results, it is proven the V_g and I_L both are meeting in the zero-processing point on the X-scale with ant high frequency mismatching issues.

Figs. 29 confirmations the inverter DC-link two capacitor voltages balancing with PV, which is the main factor of maintain the inverter output voltage and current THD. Since the DC-link capacitors are maintain it DC voltage distribution to the inverter equally, there is no much distortion in the inverter current and voltage waveform.

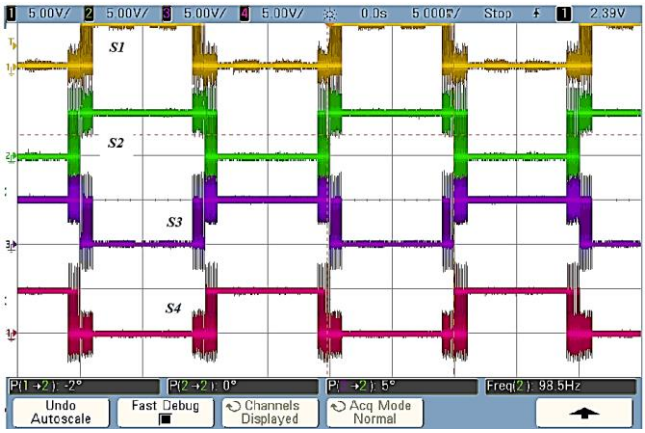


Fig. 24. The PWM pulses for top and bottom switch (S_1 to S_4).

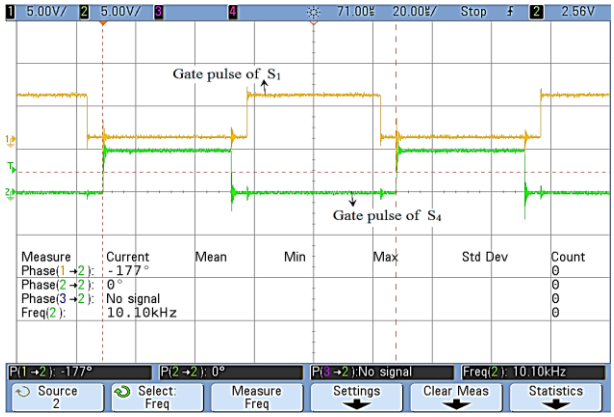


Fig. 25. The PWM pulses for top and bottom switches (S_1 and S_2).

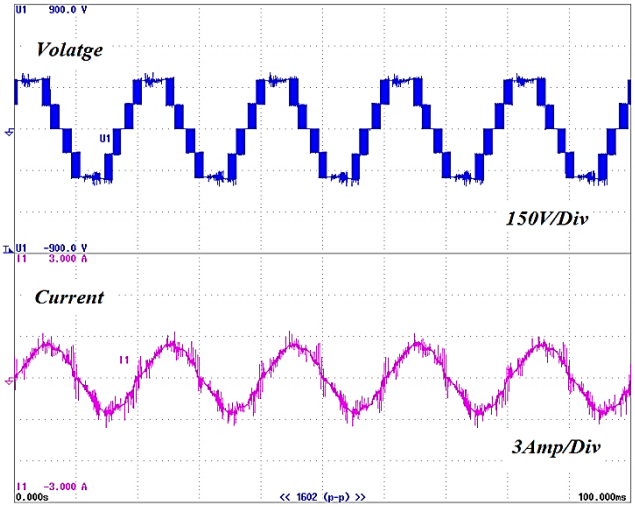
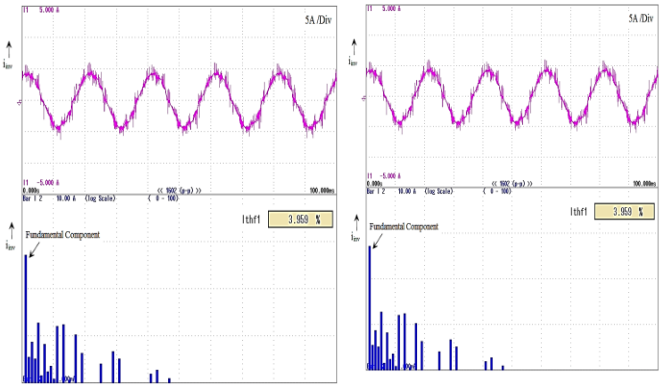


Fig. 26. experimental waveforms of inverter voltage and current of PV tied grid-connected single-phase three-level TLI

		Order	U1 [V]	hdf[%]	Order	U1 [V]	hdf[%]
fPLL1:U1	49.902 Hz	Total	293.51		dc	---------	-------
fPLL2:U2	49.894 Hz	1	288.69	98.357	2	0.54	0.183
		3	3.14	1.068	4	0.40	0.138
Urms1	297.76 V	5	43.20	14.717	6	0.19	0.064
Irms1	0.6413 A	7	21.29	7.253	8	0.41	0.141
P1	123.89 W	9	0.55	0.188	10	0.31	0.107
S1	190.95 VA	11	4.45	1.515	12	0.06	0.020
Q1	145.30 var	13	1.56	0.531	14	0.11	0.037
λ1	0.6488	15	0.52	0.176	16	0.15	0.050
Φ1	G49.55 °	17	1.19	0.406	18	0.19	0.066
		19	2.36	0.806	20	0.20	0.069
Uthd1	18.051 %	21	0.40	0.138	22	0.11	0.037
Ithd1	10.251 %	23	7.02	2.391	24	0.18	0.061
Pthd1	2.340 %	25	8.38	2.855	26	0.24	0.083
Uthf1	11.581 %	27	0.25	0.084	28	0.22	0.075
Ithf1	2.517 %	29	9.50	3.236	30	0.23	0.079
Utif1	---0 F---	31	8.71	2.968	32	0.25	0.085
Itif1	---0 F---	33	0.07	0.025	34	0.11	0.038
hvf1	7.286 %	35	5.69	1.939	36	0.30	0.101
hcf1	4.419 %	37	3.95	1.344	38	0.36	0.121
Kfact1	1.6793	39	0.10	0.033	40	0.14	0.047
PAGE 1/11					PAGE 1/13		

Fig. 27..Experimental numerical harmonics value for inverter output voltage



(a) (b)

Fig. 28. Experimental harmonics Spectrum of inverter voltage and current.

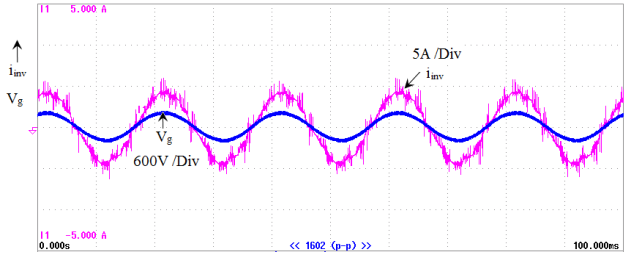


Fig. 29.Experimental waveforms for inverter current and grid voltage

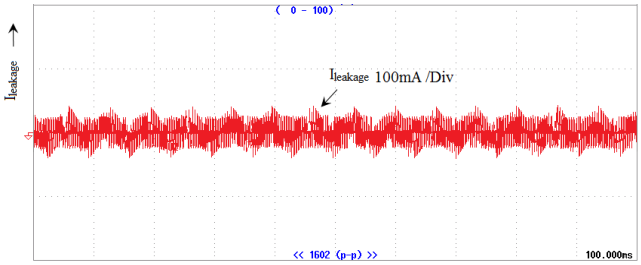


Fig. 30.Experimental waveforms for inverter leakage current.

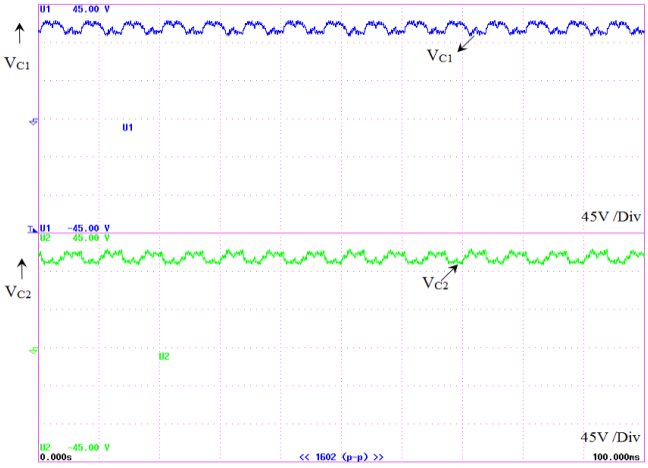


Fig. 29. Experimental waveforms for dc-link capacitors (C_1 and C_2).

V. Conclusion

In this paper, an effective single-phase PV tied three-level multilevel transformerless topology T-type TLI and its grid connected system were proposed. The topology was based in the conventional NPC-MLI inverter with DC -link capacitors. This proposed T-type TLI demonstrations better performing than conventional topologies such as Active - NPC, I-type NPC-MLI, and other same groups topologies. Both inverter and its PWM were aimed to overcome the leakage current issue in PV tied systems. The hysteresis current controller based grid PV tied grid connected TLI is established and verified in MATLAB-Simulations and laboratory scale Experimentations.

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