# SELECTIVE HARMONIC ELIMINATION ALGORITHM FOR A BOOST H BRIDGE INVERTER WITH REDUCED SWITCH CONFIGURATION

**S.Srinivasan[1], R.Ganesan[2]**
[1]EEE Dept., Sethu Institute of Technology, Kariapatti, Tamil Nadu, India.
[2]EEE Dept., Shanmuganathan Engineering College, Arasampatti, Tamil Nadu, India.
[1]Email id: sree_seenu@yahoo.co.in

***Abstract***

*Harmonic free voltage and high modularity makes multilevel inverters with Selective Harmonic Elimination (SHE) is the key method in medium power and high power inverter which is employed in renewable energy sources. However finding optimal switching angles for the nonlinear transcendental equation of the multilevel waveform is a most tedious thing in implementing this algorithm. This work have proposed a new topology called Boost H Bridge Inverter (BHBI) with selective harmonic elimination PWM algorithm for the switching angle using evolutionary based algorithms. The proposed topology is compared with the asymmetric/symmetric configuration and Cascaded H Bridge (CHB) configurations. Simulation and hardware circuits are designed and results were verified with conventional methods.*

***Keywords:*** *Selective Harmonic Elimination, Asymmetric/Symmetric, Cascaded H Bridge, Boost H Bridge Inverter, Genetic Algorithm (GA), Flower Pollination Algorithm(FPA).*

## 1. Introduction

Multilevel inverters are cemented their places in industrial drives as well as in renewable energy sources due to its manifold advantages [1-15]. The performance characteristics of inverter/converter depend on the pulse width modulation scheme adapted. Out of three popular PWM schemes available, SHE PWM is used to suppress low order harmonics by changing the square wave output of the inverter into staircase waveform by adding several switching angles. Later many mathematical methods are introduced in order to express this staircase form. Fourier series is one of the ways to express this waveform mathematically [2- 4, 8]. This equation forms the non-linear and transcendental equations. The switching angles which are main parameter of this equation are solved in such a way that keeping the fundamental voltage at a predefined value while keeping the low order harmonics to zero [2-10]. SHE PWM has the advantages of elimination of low-order harmonics, high voltage gain and wider bandwidth, smaller filter component requirements and low switching losses [3-7]. There are several literature have been reported in the past using Selective Harmonic Elimination (SHE) or minimization for fundamental frequency operation of cascaded multilevel inverters with separate DC sources. SHE-PWM exploited the Fourier theory to decompose the PWM voltage or current waveform. This formulation is based on the given waveform and its properties such as bipolar, unipolar, and stepped or PWM multilevel waveforms. There are other important waveform properties such as symmetry, and the number of levels, equal or un-equal voltage levels considered in the analysis. The form and complexity of the solution space depends on the above parameters. Finding suitable solving algorithm for SHE-PWM waveform is an up-hill task .This highly relies on the formulation of the waveform. Several approaches have been reported in the past such as iterative approaches Newton-Rapson (N-R), numerous numbers of optimization techniques including Particle Swarm Optimisation (PSO), Genetic Algorithm (GA) [2, 7], Differential Evolutionary (DE) [2], Artificial Bee Colony (ABC) algorithm [8] and classical resultant theory. Initially it was applied for conventional two and three-level converters but later it was extended to various multilevel and hybrid multilevel converters for various applications. In the above NR method requires initial guess to arrive the exact solution. The other optimisation algorithms have their own merits and demerits. Helder Zandonadi et al, have solved switching angles for 11-levels cascaded multilevel inverter using Artificial Neural Network (ANN) [10]. Author [2] have applied Flower Pollination based Algorithm (FPA) for solving SHE PWM switching compared the results with other algorithms such as GA and PSO [4]. Taghizadeh et al, solved the transcendental equations for un-

equal voltages for an 11- level inverter using PSO [4] algorithms. These results have been taken for comparing with FPA algorithm [2]. This paper proposes Selective Harmonic Elimination applied to new converter topologies called Boost H Bridge Inverter with reduced number of components. The proposed inverter scheme is compared with symmetric/asymmetric and Cascaded H Bridge multilevel converter. This design is explained in detail in section 2.1. Further section 2.2 deals with the switch optimization with asymmetric/symmetric multilevel inverter in section 2.2.a. and Boost H bridge inverter in the next section. This proposed BHBI inverter provides the optimum number of switches for any level of output voltage. This design provides flexibility and optimizes design parameters such as minimizing the number of IGBT/MOSFET switches, requirement for gate driver circuits, number of DC voltage sources, and power diodes. Reduced number of the switches leads to the compactness in size, reliable and simpler control strategy with improved efficiency. It is obvious that the proposed converter topologies can produce many levels with fewer components.

## 2. Problem Formulation

### 2.1 SHE PWM algorithm for Boost H Bridge Inverter

The DC voltage for multilevel staircase wave is obtained from a single DC capacitor link voltage instead of using separate DC sources unlike CHB inverter. For N level of output voltage needs an (N-1)/2 number of duty ratio $\alpha_{(N-1)/2}$ and the $V_{dc}$ is given in equation (1) and duty ratio in equation (2)

$$V_{dc} = \sum_{j=1}^{\frac{N-1}{2}} \alpha_j V_{in} \qquad (1)$$

Where j=1, 2 …5

$$\alpha = \frac{T_{on}}{T_{on} + T_{off}} \qquad (2)$$

Where $\alpha$ – duty ratio

$V_{in}$ – DC input voltage

$T_{on}$ – on period of MOSFET chopper

$T_{off}$ – off period of MOSFET chopper

The staircase voltage of multilevel inverter is expressed as Fourier series expansion [2-3] and using equation (1) and (2) the output voltage is expressed as

$$V(\omega t) = \sum_{n=1,3,5}^{\infty} [\frac{4}{n\pi} (\sum_{j=1}^{\frac{N-1}{2}} \frac{V_{dcj}}{1-\alpha_j} \cos(n\beta_j))] \qquad (3)$$

Switching angles $\beta_1 - \beta_j$ must satisfy the following condition:

$$0 \le \beta_1 \le \beta_2 .... \le \beta_5 \le \frac{\pi}{2} \qquad (4)$$

$$0 \le \alpha_j \le 0.9 \qquad (5)$$

$$\alpha_1 \cos(\beta_1) + \alpha_2 \cos(\beta_2) + ... + \alpha_5 \cos(\beta_5) = \frac{\pi}{2} M \qquad (6)$$

$$\alpha_1 \cos(5\beta_1) + \alpha_2 \cos(5\beta_2) + ... + \alpha_5 \cos(5\beta_5) = 0 \qquad (7)$$

Where, ‘M’ is Modulation index defined as $M = V_1 / 5V_{dc}$ and $V_1$ is the fundamental voltage.

Equations (4)-(7) are working equation of multilevel inverter, these nonlinear transcendental equations are solved using evolutionary based algorithms GA and FPA [2] are tabulated in Table 1. For a 11-level inverter the angle needed is $\beta_1 .... \beta_5$ and duty ratio is $\alpha_1 ..... \alpha_5$.

### 2.2 Switch Optimization

Increased number of switches in an inverter always increases the number of driver circuits needed, increase the on state losses and cost and more complexity. Reduced number of switches on the other hand makes the inverter compact in size and system become more reliable.

### 2.2. a. Asymmetric Inverter Configuration

As seen from fig.1 this configuration requires single H Bridge and five switches for getting the multi leveled DC input for the inverter. Each level of voltage needs one switch to conduct while other non-conducting switches the connection is made through anti-parallel diode.

Table 1 Switching Angles for Genetic Algorithm/ Flower Pollination Algorithm

| Modulation Index | GA | | | | | FPA | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\beta_1$ | $\beta_2$ | $\beta_3$ | $\beta_4$ | $\beta_5$ | $\beta_1$ | $\beta_2$ | $\beta_3$ | $\beta_4$ | $\beta_5$ |
| 0.50 | 38.93 | 53.50 | 66.25 | 86.34 | 89.59 | 38.08 | 56.42 | 66.43 | 81.39 | 88.12 |
| 0.70 | 36.66 | 52.49 | 64.52 | 82.45 | 89.98 | 12.21 | 34.04 | 50.50 | 68.94 | 90.00 |
| 0.80 | 6.79 | 18.42 | 33.02 | 89.91 | 89.94 | 8.24 | 21.99 | 38.38 | 59.01 | 88.86 |
| 1.00 | 8.76 | 22.51 | 38.76 | 59.08 | 88.53 | 3.20 | 15.12 | 20.71 | 32.85 | 51.84 |
| 1.075 | 6.48 | 15.69 | 25.39 | 38.50 | 57.95 | 3.97 | 10.33 | 23.44 | 30.42 | 42.60 |

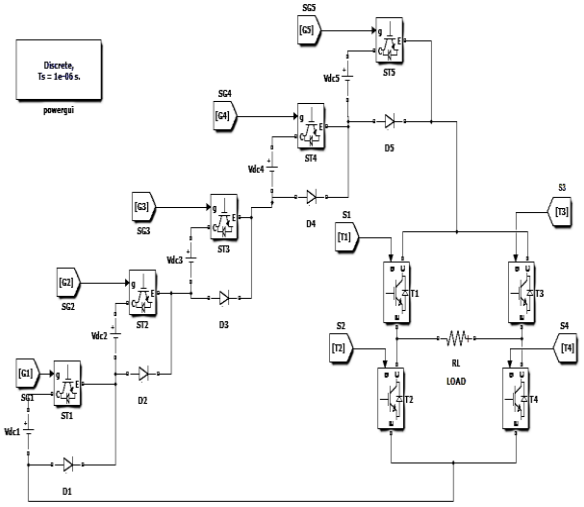


Fig.1.Simulation diagram of Asymmetric/ Symmetric inverter for an 11-level inverter

In asymmetric voltage configuration the DC voltage is unequal while in the symmetric configuration $V_{dc1}=V_{dc2}\ldots=V_{dc5}$.

### 2.2. b. Boost H Bridge Inverter (BHBI)

The switches in the above scheme require (N-1)/2 number of switches for N level of output voltage. However the proposed Boost H Bridge Inverter (BHBI) given in fig.2 requires single MOSFET switch (for any level) for its converter stage and four IGBT for its H bridge inverter arm. The multilevel voltage is obtained by varying the modulation index of the boost converter's DC-link voltage.

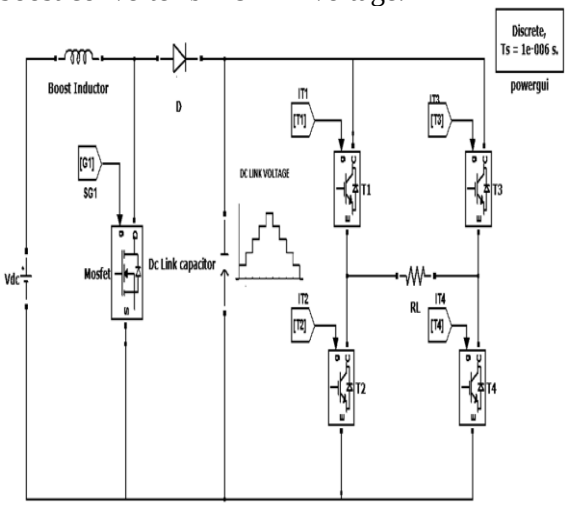


Fig.2.Simulation diagram of Boost H Bridge 11-level inverter

Table 2 Comparison of Different Inverter Configurations

| S. No. | Type of inverter | No of H Bridges | No of switc-hes | No of Driver Boards |
|---|---|---|---|---|
| 1 | Cascaded HB Inverter | 5 H Bridges | 20 | 10 |
| 2 | Symmetric/ Asymmetric | 1 H Bridge | 9 | 5 |
| 3 | Boost H Bridge Inverter | 1 H Bridge | 5 | 3 |

Table 3 Hardware Components

| S. No. | Components | Details of Components |
|---|---|---|
| 1 | IGBT | FGA25N120 ANTD |
| 2 | Driver IC | TLP 250 |
| 3 | MOSFET | IRFP 250N |
| 4 | Boost Inductor core | EE55 |
| 5 | Input DC Capacitor | 1000$\mu$F/250 V |
| 6 | Floating supply Gate driver | 12-0-12/200mA |
| 7 | Gate drive voltage | +15 V/0 V |

## 3. RESULTS AND DISCUSSION

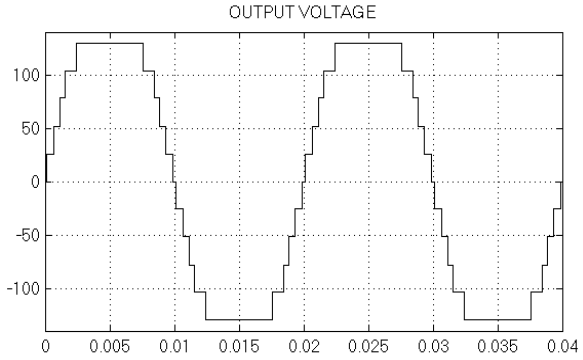


Fig.3.Simulation result for CHB11-level inverter

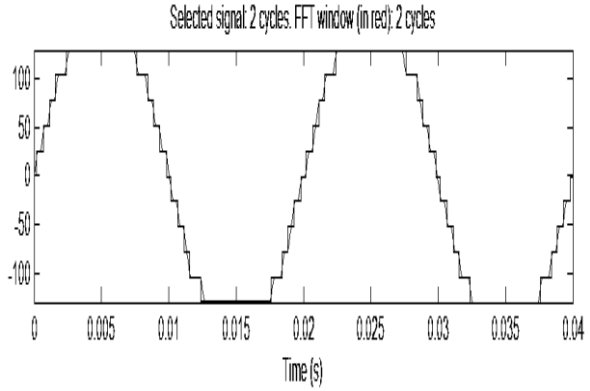


Fig.4.a Selected Waveform of CHB11-level inverter for FFT analysis

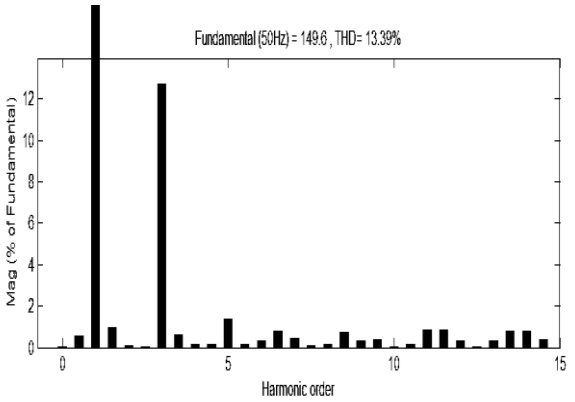

Fig.4.b. FFT analysis for CHB11-level inverter

The Table 2 shows the different inverter configurations. It is clear that the proposed Boost H bridge inverter have much reduced number of switches as well as number of driver circuits needed comparing CHB and Symmetric/Asymmetric inverter. The $r_{dson}$ of MOSFET IRF840 is 0.850Ω, for the CHB inverter for a either half cycle there are 10 switches comes in series which will present on resistance of 8.5Ω. A much higher value of resistance which will be seen from the output and this will provide on state losses of ($i^2$X8.5) Watts, an appreciable amount of losses. This reduction in voltage due this high on state resistance is evident from the result shown in fig.3.The Hardware components required for the proposed work is tabulated in Table 3. The MOSFET IRFP250N is used for boost stage, whose $r_{dson}$ is only 0.075Ω. Each half cycle only two switches come in series so the on state resistance of 0.15Ω will be seen by the output which is 57 times lesser than the CHB inverter. And hence the IGBT used for the inverter arm which greatly reduces the on state losses and the reduction in voltage across the inverter arm.

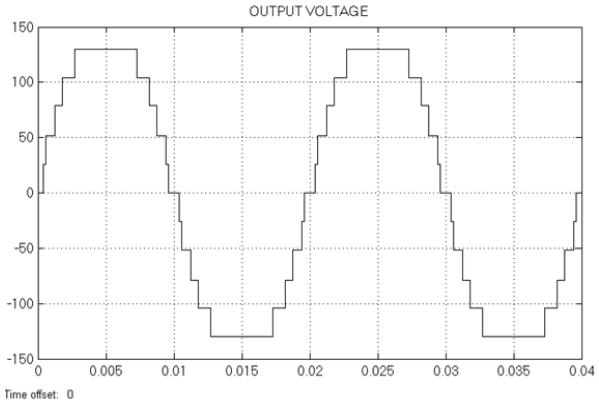

Fig.5. Simulation result for Asymmetric 11-level inverter

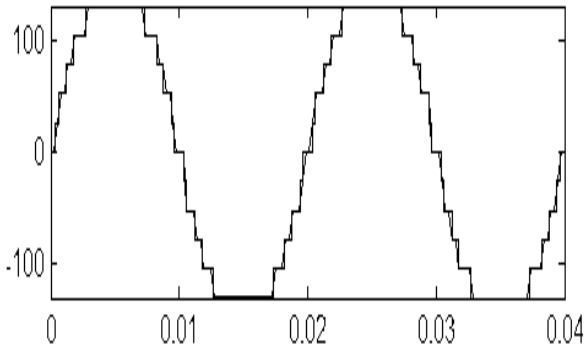
Fig.6.a. Selected waveform of Asymmetric 11-level inverter for FFT analysis

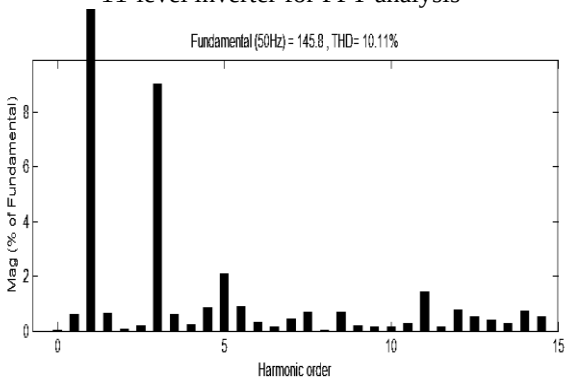

Fig.6.b. FFT analysis for Asymmetric 11-level inverter

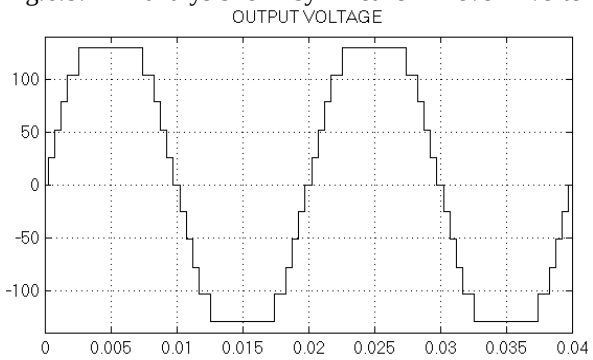

Fig.7. Simulation result for Boost H Bridge11-level inverter

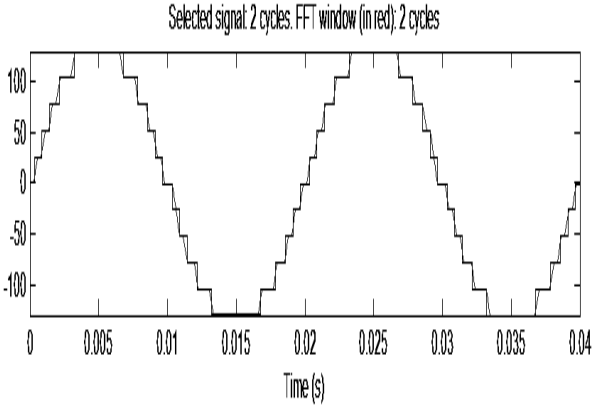

Fig.8.a. Selected waveform of Boost H Bridge 11-level inverter for FFT analysis

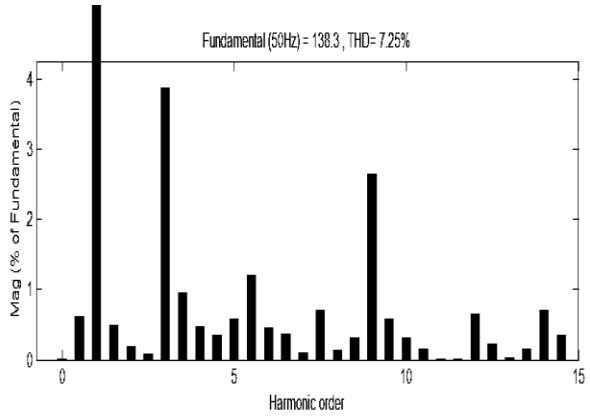


Fig.8.b. FFT analysis for Boost H Bridge11-level inverter

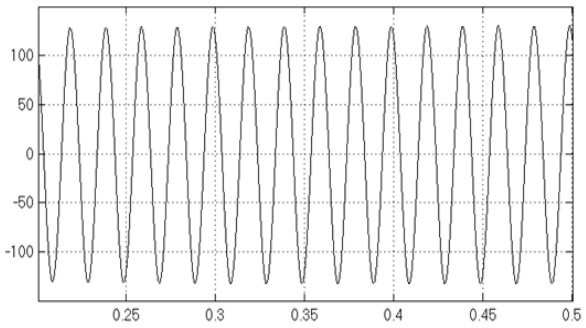

Fig.9.Voltage waveform for Boost H Bridge 11-level inverter with filter

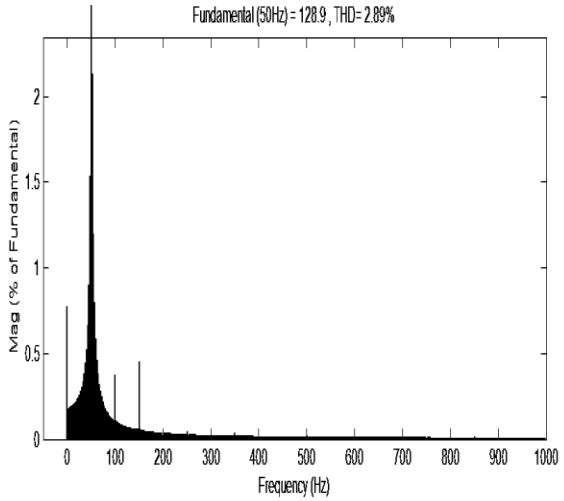


Fig.10. FFT analysis for Boost H Bridge 11-level inverter with filter

Simulation results as well as hardware results for various configurations are documented in fig.3-fig.12. CHB inverter outputs are given in fig.3 and FFT analysis of this waveform is shown in fig.4.a and 4.b. The asymmetric output voltage waveform is given in fig.5 and fig.6.a and 6.b gives the corresponding FFT analysis. It is obvious from the diagram the harmonics 5, 7, 11, 13 have been well removed and the triplen harmonic 3rd harmonics deliberately left which will be removed when it is connected in 3 phase [2]. Figures.7 -10 shows results of the proposed BHBI inverter. The THD levels gradually reduced from CHB to BHBI configuration. BHBI gives the lowest THD level compared to other two circuits for the same level of output voltage. Switch reduction and driver circuits benefits have been given in Table 2.The hardware results given in fig.11 and fig.12 shows switching transients which are evident from each level. Compared to other configuration this will be predominant high in this circuit. A suitable L C filter connected across output will reduce this effect which is shown in fig.9 and fig.10.

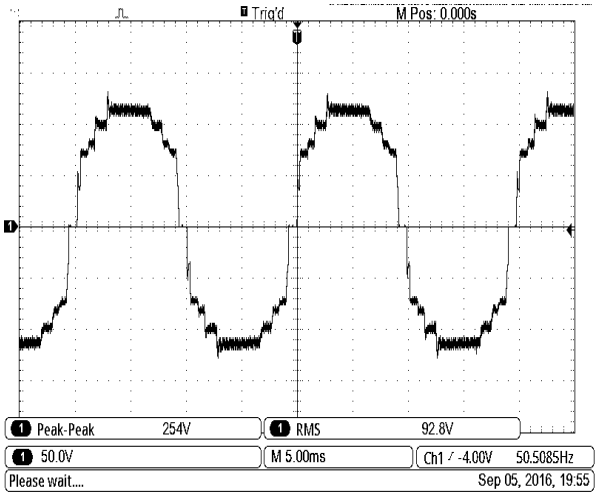


Fig.11. Hardware results for Boost H Bridge Inverter

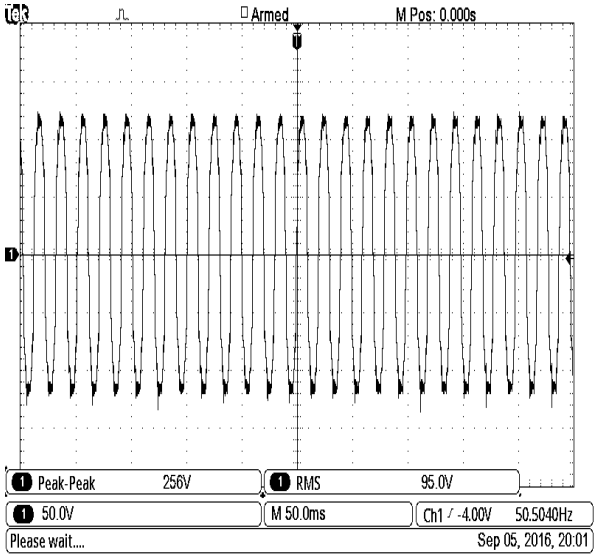


Fig.12. Voltage waveform for Boost H Bridge Inverter

## 4. CONCLUSION

The proposed work has implemented Selective Harmonic Elimination using the evolutionary based Genetic Algorithm (GA) and Flower Pollination Algorithm (FPA) to two configurations asymmetric/symmetric inverter and Boost H Bridge Inverter (BHBI). This switching algorithm and this proposed scheme have effectively reduced the on state losses in the H Bridge. This algorithm with inverter configuration has given design flexibility and parameters such as the minimizing the number of IGBT/MOSFET switches, requirement for gate driver circuits, number of DC voltage sources, and power diodes are optimized. Reduced number of the switches leads to the compact in size, reliable and simpler control strategy with improved efficiency.

**References**


[1] B.Reddy, Dastagiri, et al., "Embedded Control of n-Level DC–DC–AC Inverter", *IEEE Transactions on Power Electronics*, vol.30, no.7, pp. 3703-3711, 2015.

[2] S.Srinivasan and R.Ganesan, "Flower Pollination Algorithm based Selective Harmonic Elimination PWM for an Eleven Level Inverter", *Asian Journal of Research in Social Sciences and Humanities*, vol.6, no.6 special, pp.69-84, June 2016.

[3] H.Taghizadeh, and M. Tarafdar Hagh, "Harmonic Elimination of Cascade Multilevel Inverters with non-equal DC Sources using Particle Swarm Optimization", *IEEE Transactions on Industrial Electronics*, vol.57, no.11, pp.3678-3684, 2010.

[4] Alishah, Rasoul Shalchi, et al., "Novel Topologies for Symmetric, Asymmetric, and Cascade Switched-Diode Multilevel Converter with Minimum Number of Power Electronic Components", *IEEE Transactions on Industrial Electronics*, vol.61, no.10, pp.5300-5310, 2014.

[5] José Rodríguez and Jih-Sheng Lai, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, August 2002.

[6] Mariusz Malinowski and K. Gopakumar, "A Survey on Cascaded Multilevel Inverters", *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, July 2010.

[7] Khaled El-Naggar and Tamer H. Abdelhamid, "Selective Harmonic Elimination of New Family of Multilevel Inverters using Genetic Algorithms", *Energy Conversion and Management*, vol.49, pp.89–95, 2008.

[8] Kavousi, Ayoub, et al., "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", *IEEE Transactions on Power Electronics*, vol.27, no.4, pp.1689-1696, 2012.

[9] Fei, Wanmin, Xiaoli Du, and Bin Wu, "A Generalized Half-Wave Symmetry SHE-PWM Formulation for Multilevel Voltage Inverters", *IEEE Transactions on Industrial Electronics*, vol.57, no.9, pp.3030-3038, 2010.

[10] Maia, Helder Zandonadi, et al., "Adaptive Selective Harmonic Minimization based on ANNs for Cascade Multilevel Inverters with Varying DC Sources", *IEEE Transactions on Industrial Electronics*, vol.60, no.5, pp. 1955-1962, 2013.

[11] Ahmadi, Damoun, et al., "A Universal Selective Harmonic Elimination Method for High-Power Inverters", *IEEE Transactions on Power Electronics*, vol.26, no.10, pp.2743-2752, 2011.

[12] Pulikanti, R.Sridhar and Vassilios G. Agelidis, "Hybrid Flying-Capacitor-based Active-Neutral-Point-Clamped Five-Level Converter Operated with SHE-PWM", *IEEE Transactions on Industrial Electronics*, vol.58, no.10, pp.4643-4653, 2011.

[13] Chivite-Zabalza, Javier, et al,. "A Large Power, Low-Switching-Frequency Voltage Source Converter for Facts Applications with Low Effects on the Transmission Line", *IEEE Transactions on Power Electronics*, vol. 27, no.12, pp.4868-4879, 2012.

[14] Flourentzou, Nikolas, and Vassilios G. Agelidis, "Multi Module HVDC System using SHE-PWM with DC Capacitor Voltage Equalization", *IEEE Transactions on Power Delivery*, vol.27, no.1, pp.79-86, 2012.

[15] Lee, Kevin, and Geraldo Nojima, "Quantitative Power Quality and Characteristic Analysis of Multilevel Pulse Width-Modulation Methods for Three-Level Neutral-Point-Clamped Medium-Voltage Industrial Drives", *IEEE Transactions on Industry Applications*, vol.48, no.4, pp.1364-1373, 2012.