PERFORMANCE COMPARISON OF SINGLE-PHASE 19- AND 21-LEVEL ASYMMETRICAL CASCADED REDUCED SWITCH MULTILEVEL INVERTER TOPOLOGIES FOR THD REDUCTION

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Abstract – *This paper presents an asymmetrical cascaded multilevel H-Bridge inverter topology with reduced number of switches for increasing the number of output voltage levels. The proposed topology reduces the Total Harmonic Distortion (THD) level to below that of IEEE standard. Here, Phase Disposition (PD) and Alternate Phase Opposition Disposition (APOD) multi-carrier pulse width modulation (PWM) techniques are used to control the gating pulses. To produce the different pulse pattern for each switch, the decimal to binary conversion technique is employed. The proposed circuit is quite simple to analyze and it is suitable for medium and high power applications. Time domain simulations are carried out in Matlab/Simulink platform for 19- and 21-level multilevel inverter topologies. The results demonstrate that the THD level has been reduced drastically for 21-level inverter compared to 19-level inverter and the voltage wave form closely resembles sinusoidal which is the desired one.*

Keywords: **APOD, Multilevel inverter, PD, Pulse pattern, PWM, THD.**

1. Introduction

Nowadays, renewable energy sources are the most preferable research area, because day by day the non renewable energy sources are reduced. The renewable energy sources do not have that problem, among these the solar power is one of the most effective and alternative energy source. The photovoltaic array produces DC voltage. But most commercial applications require AC supply. However, when the basic inverters are used to convert the DC to AC, it produces symmetrical square wave. The square wave has infinite harmonics. So, this harmonic injection reduces the life time of the equipment and pollutes the power system. When the level of inverters output voltage increases, the THD reduces and the voltage waveform closely resembles sinusoidal waveshape.

The multi-level inverter (MLI) system is very promising in AC drives, where both reduced harmonic contents and high power are required [1]. A multi-level inverter topology not only used to achieve high power ratings, but also enables the use of renewable energy sources [2]. The concept of multi-level inverters was first introduced in 1975. The term multilevel began with the three-level inverter. Subsequently, several multi-level inverter topologies have been developed [3]. Up to now, several topologies of multi-level inverter system have been introduced. The main topology used to generate a high voltage waveform using low voltage devices are the series H-bridge inverter, diode clamped inverter system and flying capacitor inverter system respectively. The diode clamped inverter has the least number of capacitors among the multilevel inverter topologies but it requires additional clamping diodes [1]. The flying capacitor topology uses floating capacitors to clamp the voltage levels [4]. The H-bridge inverter topology does not need either clamping diode or floating capacitor but isolation transformer is needed to isolate the voltage source [5]. Decreasing the number of switches in a MLI configuration has been an ultimate aim in recent days and many topologies have been invented for doing so [6]-[11].

This paper deals with the development of a single phase 19-level and 21-level H-bridge inverter topologies that have five front end control switches S_1, S_2, S_3, S_4, and S_5, and a single H-bridge inverter. A carrier based PWM technique has been implemented which makes use of 21 carrier signals compared with a reference signal which are fed to a 21-5 priority encoder to control the five front end switches. The proposed multi-level inverter topology has more advantages than the existing topologies as both the number of switching devices and THD are reduced. Therefore, the switching losses are

also reduced and the efficiency of the overall system is improved.

The structure of the research work presented in this paper is organized in the following sequence. The proposed multilevel inverter topology with reduced number of switches for various modes of operation has been presented in section 2. The concept of PWM techniques employed in our work is presented in section 3. The simulation results and discussions are given in section 4. This is followed by the conclusion in the concluding section 5.

2. The proposed multilevel inverter topology

The proposed MLI is capable to generate twenty-one level output without using bidirectional switches and capacitors. It consists of five sources diodes connected in between the switches S_1, S_2, S_3, S_4 and S_5 as shown in the Fig.1. The switches are of IGBT (Insulated Gate Bipolar Transistor) type. The DC voltage sources of different cells are non-equal. The asymmetric inverter provides an increased number of voltage levels for the same number of cells than its symmetric counterpart.

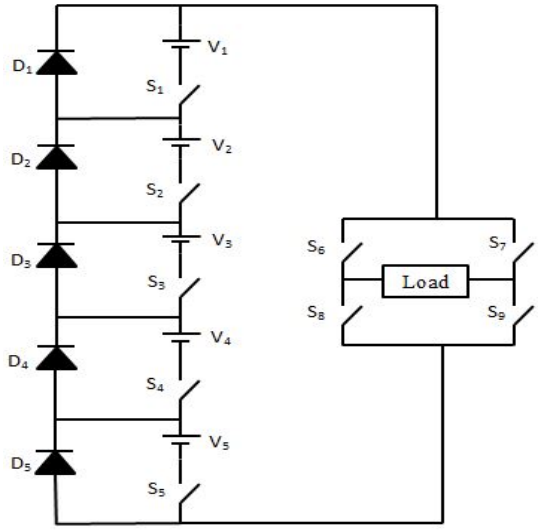
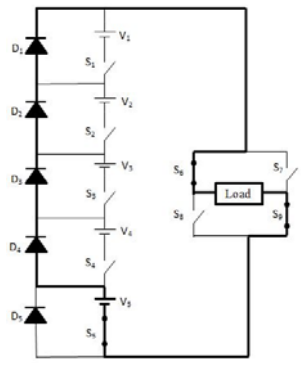


Fig. 1. Proposed multilevel inverter topology

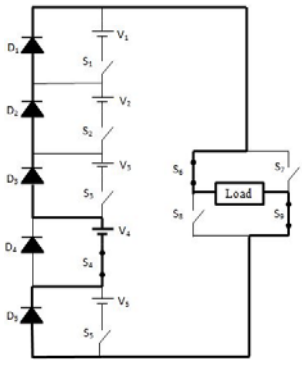
The DC sources V_1, V_2, V_3, V_4 and V_5 generate the voltages in the ratio 16:8:4:2:1 respectively. The H-bridge inverter uses the five sources in series as its voltage source. The sources V_1-V_5 can be connected or disconnected using the switches S_1-S_5 respectively for producing different voltage levels. Switches S_6-S_9 are used to control the direction of current flow thereby producing alternating output across the load. For the generation of 19- and 21-level output voltages, the proposed system consists of nine switches, whereas the existing cascaded multilevel inverter consists of twelve switches to produce fifteen level output voltages [8].

Considering the maximum DC link voltage level as V_{dc}, the proposed inverter produces twenty-one output voltage levels such as $V_{dc}/21$, $2V_{dc}/21$, $3V_{dc}/21$, $4V_{dc}/21$, $5V_{dc}/21$, $6V_{dc}/21$, $7V_{dc}/21$, $8V_{dc}/21$, $9V_{dc}/21$, $10V_{dc}/21$, $11V_{dc}/21$, $12V_{dc}/21$, $13V_{dc}/21$, $14V_{dc}/21$, $15V_{dc}/21$, $16V_{dc}/21$, $17V_{dc}/21$, $18V_{dc}/21$, $19V_{dc}/21$, $20V_{dc}/21$, and V_{dc} respectively from the DC supply voltage. The operation is divided into 21 modes having different voltage levels. Considering the variable ‘m’, mode m will have the voltage level of (m-1)/21. The switching states of 21 levels are illustrated in Fig. 2. The same voltage levels are obtained on negative side as well. The proposed H-bridge topology is significantly advantageous over other topologies, in terms of less number of power switches, power diodes, and reduced THD.

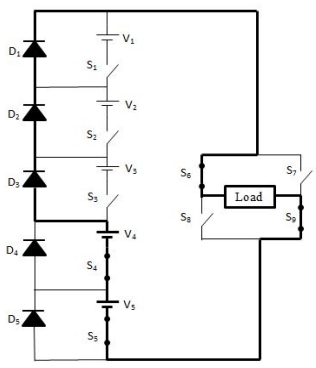
The switching sequence to the switches S_1, S_2, S_3, S_4 and S_5 are given by a binary logic, in which the digits in the binary system are formed from 00000 to 10101. The ‘0’ indicates that the switch is in ‘off’ condition and ‘1’ indicates that the switch is in ‘on’ condition. Based on this switching condition, the front end IGBTs are fired to generate the multilevel waveforms. The switching pulses for the H-Bridge IGBTs are controlled by normal sinusoidal PWM technique (SPWM), in which a pair of IGBTs is fired simultaneously to obtain positive and negative cycle waveforms. The positive levels are



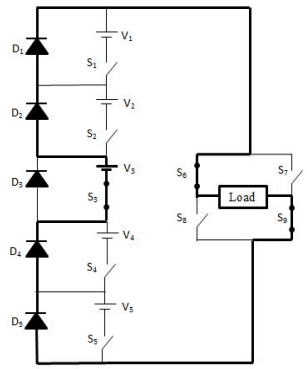
(a) Mode I



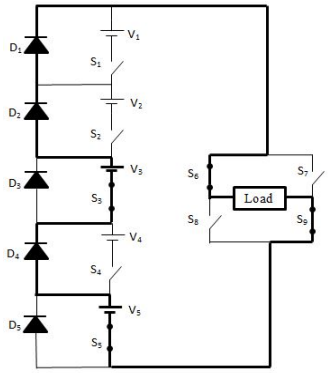
(b) Mode II



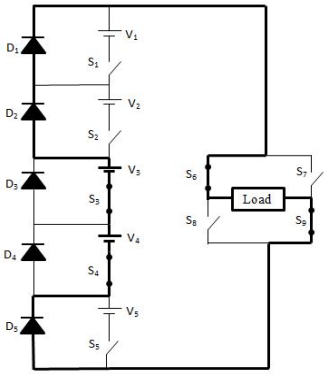
(c) Mode III



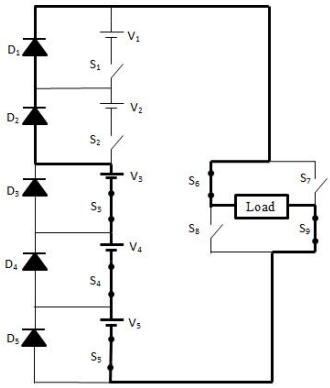
(d) Mode IV



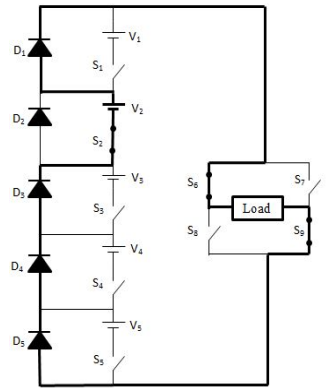
(e) Mode V



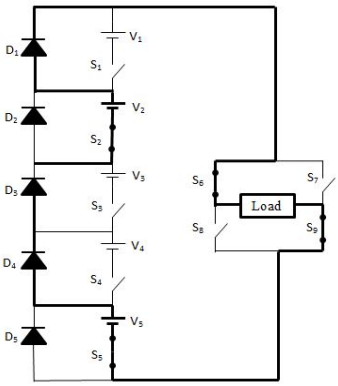
(f) Mode VI



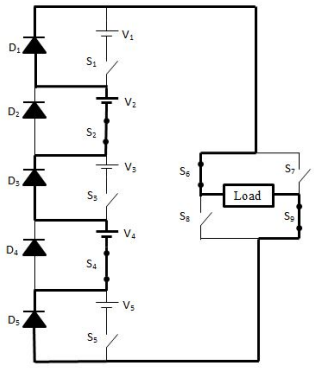
(g) Mode VII



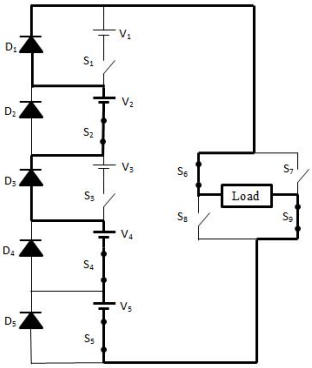
(h) Mode VIII



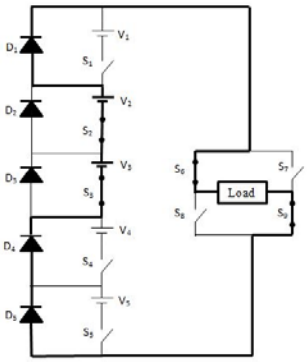
(i) Mode IX



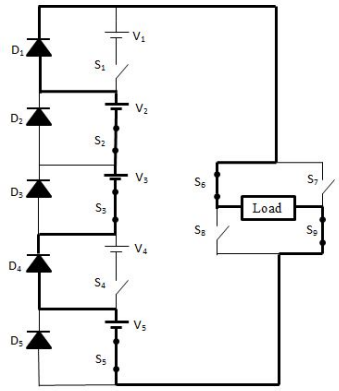
(j) Mode X



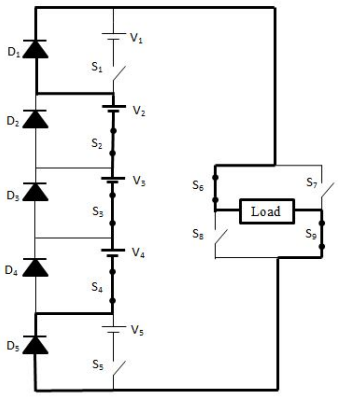
(k) Mode XI



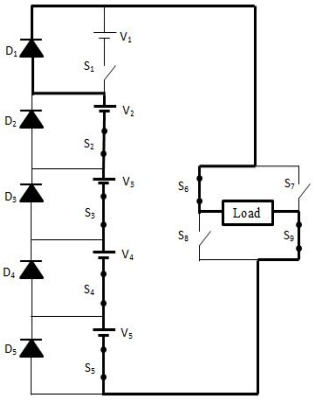
(l) Mode XII



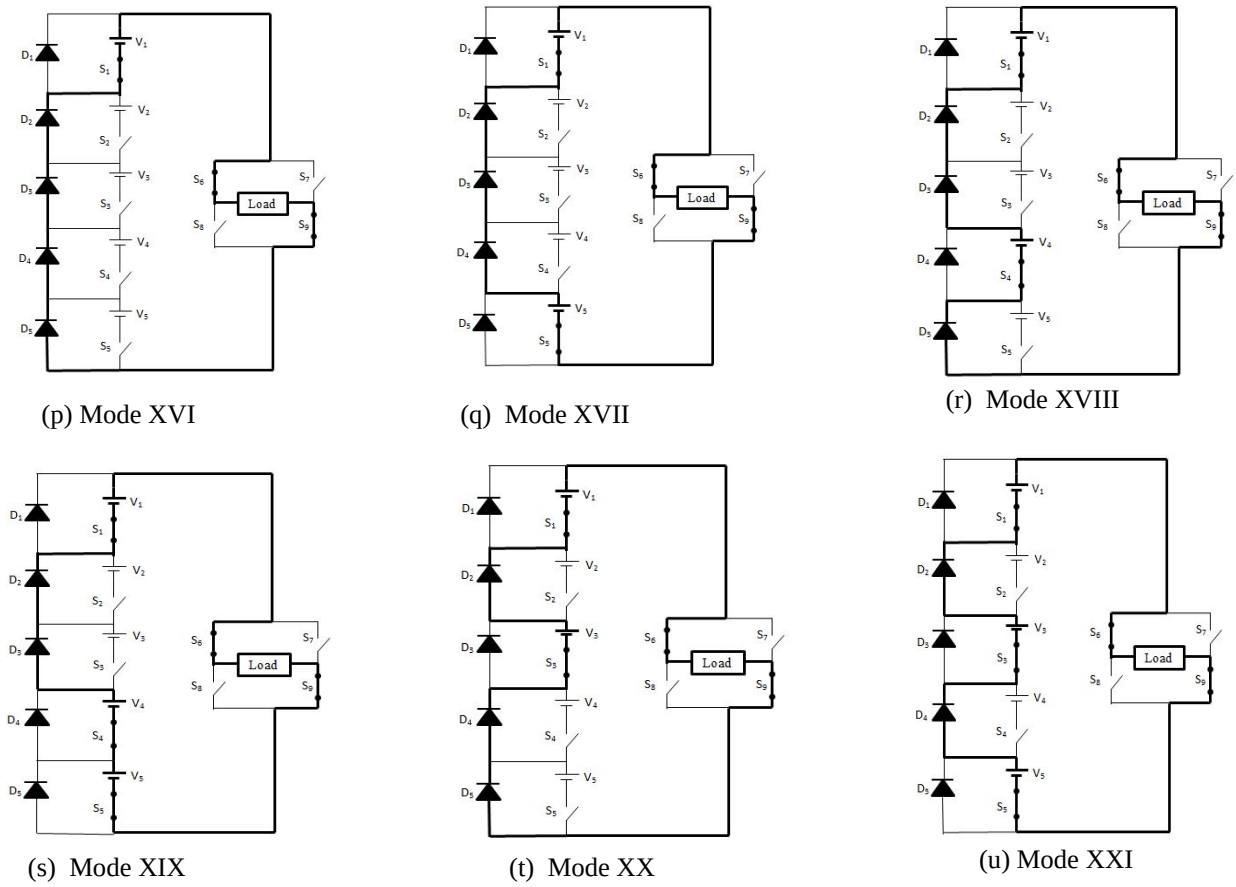
(m) Mode XIII



(n) Mode XIV



(o) Mode XV



(p) Mode XVI (q) Mode XVII (r) Mode XVIII

(s) Mode XIX (t) Mode XX (u) Mode XXI

Fig. 2 Various modes of operation of MLI for producing the DC link Voltage

obtained when switches S_6 and S_9 are in 'on' condition and switches S_7 and S_8 are in 'off' condition. Similarly, the negative levels are obtained when switches S_7 and S_8 are in 'on' condition and S_6 and S_8 are in 'off' condition respectively. The switching table is shown in Table I.

3. PWM technique

It is necessary to provide switching pulses for the nine switches in the MLI circuit shown in Fig. 1. Two different PWM techniques are used here. For switches S_6-S_9, the normal SPWM technique is used. For generating the firing pulses for the DC link switches (S_1-S_5), a carrier based PWM technique is preferred. In this modulation technique, there is one reference sine waveform V_{ref}, and N number of triangular waves, where N represents the number of output voltage levels. Hence, for producing 19- and 21-level output voltages, 19-carrier waves (V_{car1}-V_{car19}) and 21-carrier waves (V_{car1}-V_{car21}) are utilised, each having much higher frequency than the reference as shown in Fig. 3.

There are different carrier based pulse width modulation strategies as given below [12]:

A. Phase disposition (PD) multi-carrier pulse width modulation

In phase disposition strategy, where all carrier waveforms are in same phase.

B. Phase opposition disposition (POD) multi-carrier pulse width modulation

In phase opposition disposition strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 180^0 out of phase.

C. Alternate phase opposition disposition (APOD) multi-carrier pulse width modulation

In alternate phase opposition disposition strategy, each carrier waveform is out of phase with its neighbour carrier by 180^0.

D. Phase-shifted carrier (PSC) pulse width modulation

In phase-shifted multi-carrier strategy, all triangular carrier waves have the same frequency and same peak-peak amplitude. But, there is a phase shift between two adjacent carrier waves.

The APOD and POD techniques are more convenient than PD technique for single-phase inverters [4]. In this work, PD and APOD techniques are used.

In Fig. 3, the topmost carrier wave is V_{car21} and the bottommost is V_{car1}. Each of the carrier wave is compared with the reference wave V_{ref}. If the carrier wave's instantaneous value is less than that of the reference value, the comparator output is high. The outputs of the comparator values are tabulated in Table II. These outputs are fed to a 21 to 5 bit priority encoder. This binary logical conversion is done as a decimal to binary conversion. The output bit acts as the trigger pulses for switches S_1 to S5 as shown in Table II.

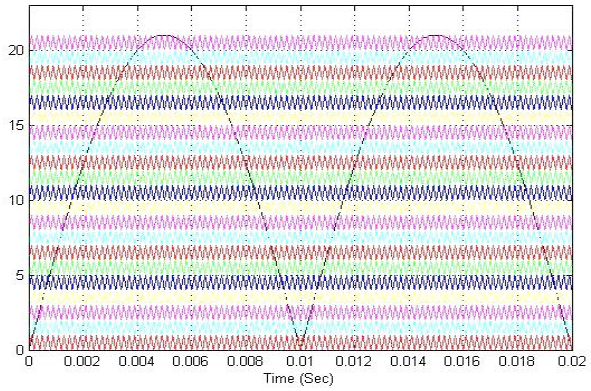


Fig. 3. Carrier and Reference Waveforms

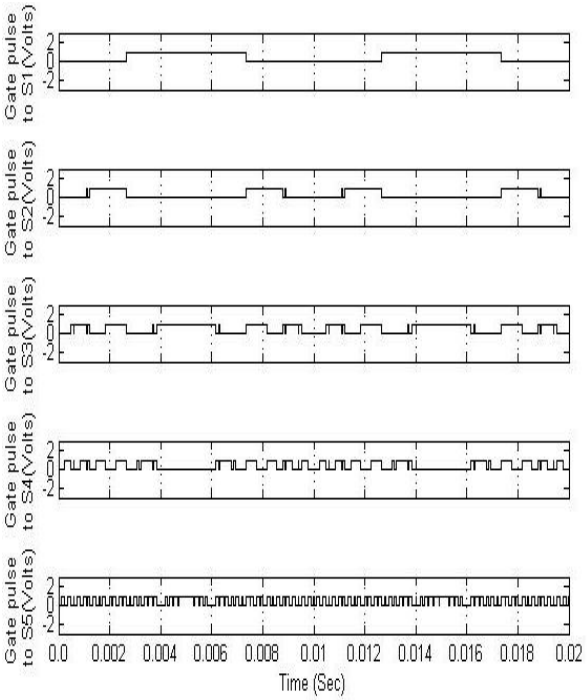


Fig. 4. Firing pulses to switches S_1, S_2, S_3, S_4

Table I
Switching states for various voltage level using Binary Code (0 is OFF and 1 is ON)

Voltage level	State of switches S_1 to S_9								
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$V_{dc}/21$	0	0	0	0	1	1	0	0	1
$2V_{dc}/21$	0	0	0	1	0	1	0	0	1
$3V_{dc}/21$	0	0	0	1	1	1	0	0	1
$4\ V_{dc}/21$	0	0	1	0	0	1	0	0	1
$5\ V_{dc}/21$	0	0	1	0	1	1	0	0	1
$6\ V_{dc}/21$	0	0	1	1	0	1	0	0	1
$7V_{dc}/21$	0	0	1	1	1	1	0	0	1
$8\ V_{dc}/21$	0	1	0	0	0	1	0	0	1
$9\ V_{dc}/21$	0	1	0	0	1	1	0	0	1
$10\ V_{dc}/21$	0	1	0	1	0	1	0	0	1
$11\ V_{dc}/21$	0	1	0	1	1	1	0	0	1
$12\ V_{dc}/21$	0	1	1	0	0	1	0	0	1
$13\ V_{dc}/21$	0	1	1	0	1	1	0	0	1
$14\ V_{dc}/21$	0	1	1	1	0	1	0	0	1
$15\ V_{dc}/21$	0	1	1	1	1	1	0	0	1
$16\ V_{dc}/21$	1	0	0	0	0	1	0	0	1
$17\ V_{dc}/21$	1	0	0	0	1	1	0	0	1
$18\ V_{dc}/21$	1	0	0	1	0	1	0	0	1
$19\ V_{dc}/21$	1	0	0	1	1	1	0	0	1
$20\ V_{dc}/21$	1	0	1	0	0	1	0	0	1
$21\ V_{dc}/21$	1	0	1	0	1	1	0	0	1
$-1\ V_{dc}/21$	0	0	0	0	1	0	1	1	0
$-2\ V_{dc}/21$	0	0	0	1	0	0	1	1	0
$-3\ V_{dc}/21$	0	0	0	1	1	0	1	1	0
$-4\ V_{dc}/21$	0	0	1	0	0	0	1	1	0
$-5\ V_{dc}/21$	0	0	1	0	1	0	1	1	0
$-6\ V_{dc}/21$	0	0	1	1	0	0	1	1	0
$-7\ V_{dc}/21$	0	0	1	1	1	0	1	1	0
$-8\ V_{dc}/21$	0	1	0	0	0	0	1	1	0
$-9\ V_{dc}/21$	0	1	0	1	1	0	1	1	0
$-10\ V_{dc}/21$	0	1	0	1	1	0	1	1	0
$-11\ V_{dc}/21$	0	1	0	1	1	0	1	1	0
$-12\ V_{dc}/21$	0	1	1	0	0	0	1	1	0
$-13\ V_{dc}/21$	0	1	1	0	1	0	1	1	0
$-14\ V_{dc}/21$	0	1	1	1	0	0	1	1	0
$-15\ V_{dc}/21$	0	1	1	1	1	0	1	1	0
$-16\ V_{dc}/21$	1	0	0	0	0	0	1	1	0
$-17\ V_{dc}/21$	1	0	0	0	1	0	1	1	0
$-18\ V_{dc}/21$	1	0	0	1	0	0	1	1	0
$-19\ V_{dc}/21$	1	0	0	1	1	0	1	1	0
$-20\ V_{dc}/21$	1	0	1	0	0	0	1	1	0
$-21\ V_{dc}/21$	1	0	1	0	1	0	1	1	0

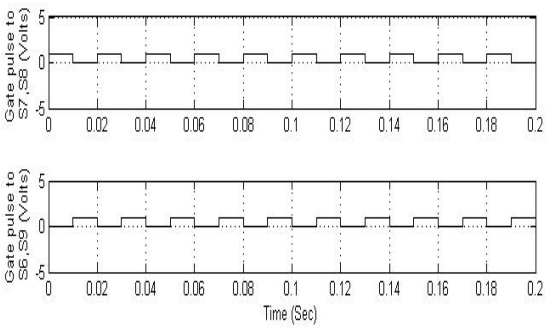


Fig. 5. Firing pulses to switches S_6, S_7, S_8 and S_9

For example, consider the instant of time at which the output is $17V_{dc}/21$ for which the switching states are: S_1-ON, S_2-OFF, S_3-OFF, S_4-OFF, S_5-ON. This is the instant at which the value of V_{car17} becomes lesser than V_{ref}. Therefore, the encoder produces the value "10001", fed to the switches. Thus the switches S_1-S_5 switch at the rate of carrier frequency. The same is applicable for the 19-level also. The firing pulses to the switches S_1-S_5 for 21 level are shown in Fig. 4.

The switching pulses given to the H-Bridge IGBTs are controlled by normal SPWM. When a pair of switches is ON, the other switches are OFF and vice-versa. When S_6 and S_9 are ON, the positive half of the waveform is generated, and when S_7 and S_8 are ON, the negative half cycle of waveform is generated. The firing pulses to the switches S_6-S_9 are shown in Fig. 5.

4. Simulation results and discussion

The proposed MLI topology is simulated in Matlab / Simulink environment as shown in Fig. 6. The simulation circuit consists of five front end IGBTs (S_1-S_5) which are connected with five DC voltage sources of rating $V_1 = 80V$, $V_2 = 40V$, $V_3 = 20V$, $V_4 = 10V$, $V_5 = 5V$ respectively and diodes D_1-D_5. It also consists of four IGBTs S_6-S_9 are connected in an H-bridge model as shown in the circuit.

The switching pulses are given to the H-Bridge circuit by normal sinusoidal pulse width modulation (SPWM) technique for the generation of positive and negative cycles. The switching pulses for front end IGBTs are given by the binary priority encoder logic as explained in section 2.

The Table II shows the various switching pulse values of the front end switches. These pulses are generated when the reference signal overlaps the carrier signals. The pulses are generated along with a delay which is given to each switch. The frequency of the reference sine wave is 50 Hz and those of the carrier waves are about 5 KHz each. The output voltage and current waveforms of the 19- and 21- level MLI are shown in Figs. 7 &10.

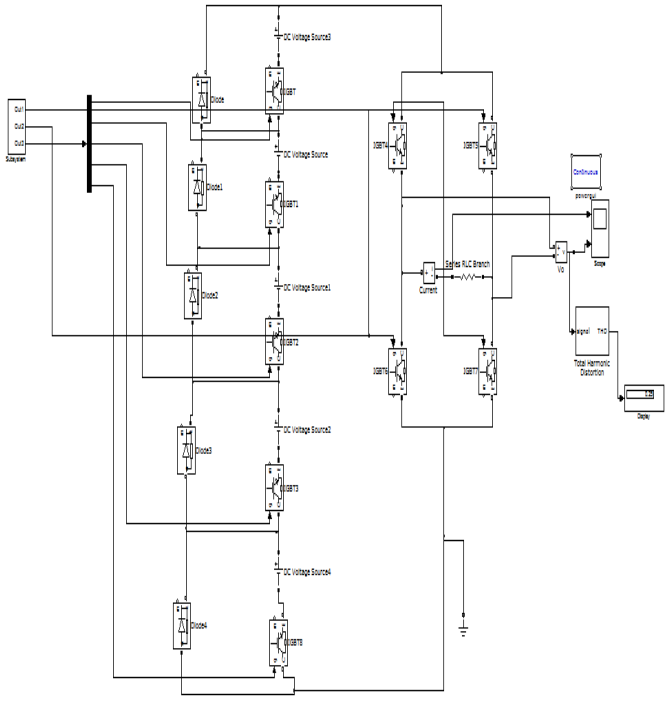


Fig. 6. Simulink circuit of the proposed MLI topology

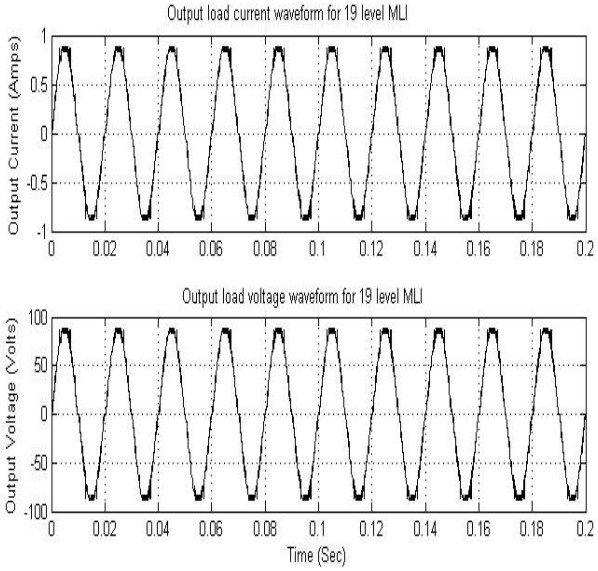


Fig. 7. Output current and voltage waveforms for 19-Level MLI

Table II

Truth table for 21-5 Priority Encoder - '×' represents a Don't care condition

Inputs (D_{21} to D_1)																					Outputs (S_1 to S_5)				
21	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**1**	**2**	**3**	**4**	**5**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	0	0	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	0	1	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	0	1	0	1	0
0	0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	0	1	0	1	1
0	0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	0	1	1	0	0
0	0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	0	1	1	0	1
0	0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	0	1	1	1	0
0	0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	0	1	1	1	1
0	0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	0	0	0
0	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	0	0	1
0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	0	1	0
0	0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	0	1	1
0	1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	1	0	0
1	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	×	1	0	1	0	1

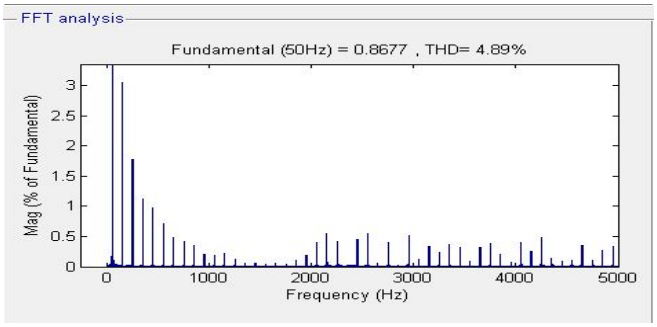


Fig. 8. FFT plot for output current of 19-level MLI

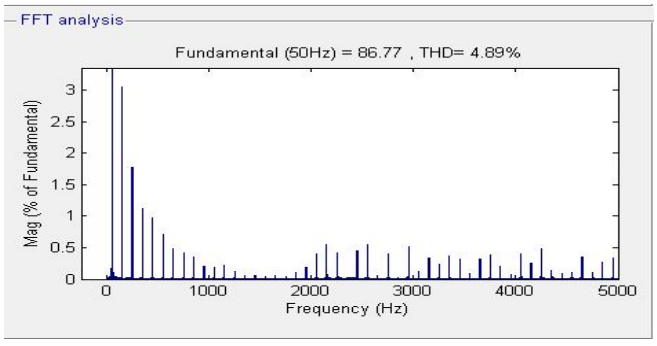


Fig. 9. FFT plot for output voltage of 19-level MLI

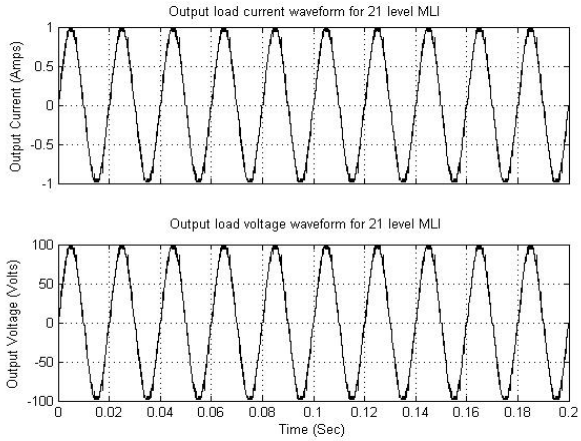


Fig. 10. Output current and voltage waveforms for 21-level MLI

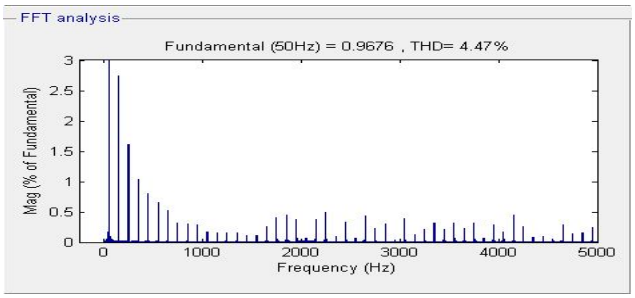


Fig. 11. FFT plot for output current of 21-level MLI

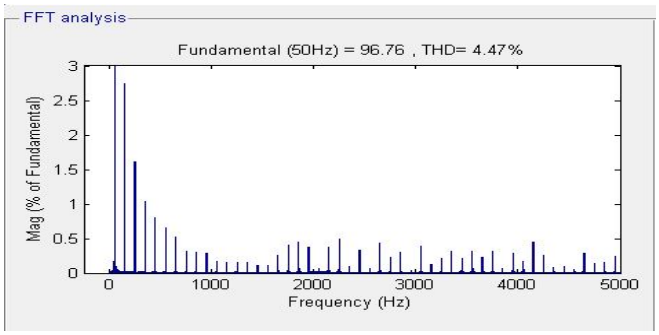


Fig. 12. FFT plot for output voltage of 21-level MLI

The FFT (Fast Fourier Transform) analysis of output current and voltage for 19-level MLI is shown in Figs. 8 & 9, for which the Total Harmonic Distortion (THD) obtained is about 4.89% for both current and voltage. The FFT analysis of output current and voltage for 21-level MLI is given in Figs. 11 & 12, for which THD obtained is about 4.47% for both current and voltage. Thus, when the number of level increases, the THD reduces gradually. The Table III shows the THD values for 19- and 21-level inverters employing PD and APOD PWM techniques.

Table III
Comparison of THD for various sinusoidal PWM techniques

Level of inverter	PWM technique used	THD
19	PD	5.04%
19	APOD	4.89%
21	PD	4.50%
21	APOD	4.47%

From the Table III, it is evident that the APOD based SPWM technique produces less harmonics than PD based SPWM technique for same level of inverter output waveforms.

5. Conclusion

A Single phase reduced switch asymmetrical multilevel inverter topology has been proposed in this paper. The 19- and 21-levels are used for the inverter. The PD and APOD based SPWM modulation approaches are presented and utilized in the proposed topology. This configuration of MLI topology results in the reduction of the number of switches, losses and cost of the inverter. The time domain simulation results verify that the APOD based SPWM technique applied to the proposed MLI topology is capable to produce near-sinusoidal output voltage which has very low harmonic content without using filter circuits. The 21-level MLI produces low THD of about 4.47% as compared to 19-level MLI for which THD is around 4.89%. One more advantage of this topology is that it can be extended to higher output levels without using bidirectional switches.

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