FPGA BASED SINGLE-PHASE CASCADED MULTILEVEL VOLTAGE SOURCE INVERTER FED ASD APPLICATIONS

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Abstract: *This paper presents Field Programmable Gate Array (FPGA) based Sinusoidal Pulse Width Modulation (SPWM) controller for single-phase cascaded multilevel inverter fed Adjustable Speed Drive (ASD) applications. The cascaded inverter is constructed using three conventional full H-bridges for a seven-level output that reduces the harmonic content. PWM Voltage Source Inverter (VSI) should maintain the variation of both voltages and frequency simultaneously and keep their ratio constant for the control of speed. In this investigation, a simple SPWM control circuit is adopted using FPGA device. It can be accommodated in a single chip that provides high computation speed and accurate control signals for higher output voltages and currents with less harmonics. VHDL language is used to model the inverter switching strategies. The proposed controller generates 12-control switching signals that cascaded multilevel inverter for 7- level output voltage. Matlab/System generator and ISE/XILINX tools are used with hardware-co-simulation to synthesize the digital-control architecture and the obtained architecture is embedded in FPGA.*

Key words: *Field Programmable Gate Array (FPGA), VHDL Hardware description language, cascaded multilevel inverter, Sinusoidal PWM, Digital controller.*

1. Introduction

Pulse width modulation technique based cascaded multilevel inverter is an important research area in electrical power systems. Many significant improvements have been noticed in this area in past few years. These power converters design implementation depends on industrial and commercial applications [1-3]. The literature has covered three cases of transformer less multilevel inverter topologies; these are (i) flying capacitor inverter, (ii) diode clamped inverter and (iii) cascaded H-bridge inverter. Among these inverters, the flying capacitor inverter is hard to realize because each capacitor must be charged with different voltages levels. Furthermore, the clamped inverter, also known as a neutral clamped converter is hard to enhance in multilevel because of the natural problem in the DC-link voltage unbalancing. Even though, cascaded inverter has disadvantage of separate dc-source requirement, these cascaded inverter has been widely applied to applications such as high-power motor drive, HVDC, variable speed drive, UPS and APLC and so on [4-7]. Mostly analog devices are used to implement PWM control schemes for switching strategies. It requires high sampling rate for wide-bandwidth performance and results in more complexity [8-10]. To overcome these problems digital control techniques are becoming the most widespread resolution in modern power electronics controllers. The microprocessors, DSP processor and Application Specific Integrated Circuits (ASICs) are responsible for better performance of the power converters. Yet the design of digitally controlled power electronics is affected by several problems, such as sampling rate, software portability, re-usability, peripheral devices, complicate design and specific register settings for each microprocessor [11]. Change of microprocessor or need of better performance requires a huge revision of the design to fit with the new system. These problems can be mitigated by designing the controller in Field Programmable Gate Array (FPGA) [12].

Very Large Scale Integration (VLSI) technology and Electronic Design Automation (EDA) techniques created an opportunity for the development of complex and compact high-performance controllers [11-12]. FPGA is a Programmable Device, compressing thousands of logic gates in a single chip and some of them can be combined to form a Configurable Logic Block (CLB). FPGA benefits of using portable high level Hardware Description Languages (HDLs) to encompass the holistic modeling of industrial FPGA design environment. It allows concurrent operation, reduced time, easy and fast circuit modification and low cost even for complex circuits. It also maximizes operational performance to achieve high efficiency and power quality while simultaneously allows the rapid prototyping of digital controllers in ASICs [13].

This article investigates a FPGA based controller for single-phase cascaded inverter fed adjustable speed of induction motor drives applications. The output of the inverter is controlled by sinusoidal PWM techniques. This SPWM is a most well known method for current-

controlled voltage source inverter, which uses a sawtooth carrier instead of triangular for increasing the switching frequency. In this investigation, 16-bit and 14-bit counter is used to generate digitized sinusoidal and sawtooth signals respectively. These signals are compared to generate the PWM pulses with required modulation index. This modulation index can be varied by changing the amplitude of the reference signal. The modulation ratio of the frequency is maintained at constant for speed control of motor drives. The proposed FPGA controller algorithm provides better modulation index range and reduces harmonic content. This digital-controller part is experimented with Xilinx/SPARTAN3E device FPGA-board using Matlab/System generator through hardware-co-simulation.

2. Cascaded Multilevel Inverter Topology

A single phase cascaded multilevel inverter is constructed by conventional H-bridges. Three H-bridges are connected in cascaded method for 7-level output voltage. Each H-bridge is connected to a battery or a fuel cell for dc supply source as shown in Fig 1. The basic principle is to generate the required AC-output waveforms from various voltage levels at reduced dv/dt. This cascaded multilevel inverter connected with resistive and inductive (R-L load) load instead of induction motor for testing the model. Digital sinusoidal PWM technique is used for generating gate switching pulses for driving the cascaded multilevel inverter. The SPWM techniques is most widely used method in voltage control inverters for motor drives, static var compensator and active power line conditioning applications [6-7].

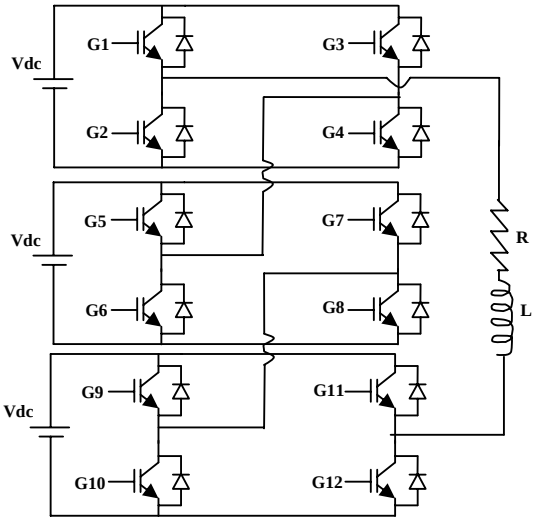

Fig 1 Cascaded multilevel PWM single-phase inverter

The sinusoidal PWM technique based cascaded inverter applies to motor control is a way of delivering energy through a succession of pulses rather than analog varying signals. By increasing or decreasing pulse width, the controller regulates energy flow to the motor shaft. The motor has own inductance that acts like a filter storing energy during the ON cycle while releasing it at a rate corresponding to the input or reference signal. The reference sinusoidal signals are produced from 16-bit up-down counter using VHDL program. These sinusoidal signals are compared with digitized sawtooth-signals to generate the PWM gate pulses to operate the cascaded multilevel voltage source inverter.

The adjustable speed drive applications are required to take energy from the AC-side of the cascaded inverter and send it back into the DC-side of the rectifier. ASDs motive is to either brake or slow down the motor speed, the kinetic energy is sent into the voltage DC-link as shown in Fig 2. This is known as the regenerative operation and in contrast to the motoring mode. The cascaded multilevel inverter output voltage of the first, second and third H-bridges are denoted by V_1, V_2 and V_3 respectively. The output voltage of the converter is written as

$$V_0(t) = V_1(t) + V_2(t) + V_3(t) \qquad (1)$$

By switching ON and OFF the first H-bridge, the output voltage V_1 can be made equal to three levels such as –Vdc, 0 and +Vdc. Similarly the second and third H-bridge output voltage can be made equal to –Vdc, 0 and +Vdc. Therefore, the output voltage of the inverter is a combination of first, second and third H-bridge supply voltage source.

The digital-control algorithm based 7-level fundamental switching scheme topology is used to regulate the output voltage and to guarantee the power quality. These switching patterns are used for a possible cycle output 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc and -3Vdc voltage levels. The transistor switches uses insulated gate bipolar transistors (IGBTs) at a PWM frequency to smooth the waveform. The 7-level fundamental frequency switching pulse is a good method for the hybrid cascaded H-bridge single-phase multilevel voltage source inverter. The switching signals and output voltage of the single phase cascaded inverter is shown in Table 1.

The widths of the pulses depend upon the amplitude of reference sinusoidal signal; if amplitude is increased width will also increase. The ratio of the reference amplitude sinusoidal waveforms (V_r) and carrier amplitude sawtooth waveforms (V_c) is called modulation index (m). It is defined as $m = V_r / V_c$.

The output of the inverter can be controlled by adjusting the modulation index. The modulation index can be varied by changing the amplitude of the reference sinusoidal signal. The rms value of the output voltage inverter depends upon the widths δ_m of the pulses and it is given as follows

$$V_{o(rms)} = Vs\left[\sum_{m=1}^{p}\frac{\delta_m}{\pi}\right]^{\frac{1}{2}} \quad (2)$$

Here the number of pulses p (per half cycle) depends upon frequency of the carrier signal. It is given as

$$p = \frac{f_c}{2f} = \frac{m_f}{2} \quad (3)$$

Here $m_f = f_c / f$ is the frequency modulation ratio. The sinusoidal pulse width modulation eliminates all the harmonics less than $(2p-1)$

Table 1 Gate switching signal for cascaded inverter

G 1	G 2	G 3	G 4	G 5	G 6	G 7	G 8	G 9	G 10	G 11	G 12	Output
1	0	0	1	1	0	0	1	0	1	1	0	3Vdc
1	0	1	0	1	0	1	0	0	1	1	0	2Vdc
0	1	1	0	0	1	1	0	0	1	1	0	Vdc
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	0	0	1	-Vdc
1	0	1	0	1	0	1	0	1	0	0	1	-2Vdc
0	1	1	0	0	1	1	0	1	0	0	1	-3Vdc

In the case of three pulses per half cycle (p=3), the lowest harmonics present will be (2x3-1) =5. Thus 2nd, 3rd, 4th harmonics will be absent. Thus it is desirable to use more number of pulses to eliminate more harmonics. But more number of pulses increases the switching losses in the devices. Hence, the optimum value of the pulses is selected.

3. FPGA based SPWM Controller

The proposed FPGA controller block diagram is shown in Fig 2. The single phase AC-main is connected with DC-link capacitor through diode bridge rectifier for DC-output. The DC-link capacitor maintains constant voltage and stores energy for supplying to the cascaded multilevel inverter. The output voltage of the inverter is fed to an adjustable speed induction motor drive. This section, presents a digital SPWM control method and its FPGA implementation for single-phase cascaded inverter.

The desired reference speed rpm value is applied to the Analog to Digital Converter (ADC) as shown in Fig 2. The digitized fixed reference speed value is 1500 rpm and it is multiplied with a gain of 1.666 to set the reference amplitude to 2500 V. The digitized fixed reference speed value combines with the accumulator operation to set the frequency range. The frequency range is divided by an 8-bit shift register and connected through a feedback loop. The feedback loop makes the amplitude and frequency ratio constant. These data are stored in a 14-bit ROM device and interfaced with black box (VHDL code) available in system generator tool to generate sinusoidal signal as shown in Fig 3. Another 180^0 phase shifted sinusoidal signal (or inverse sinusoidal signals) is generated from the above reference signal by applying 180^0 phase shift operation.

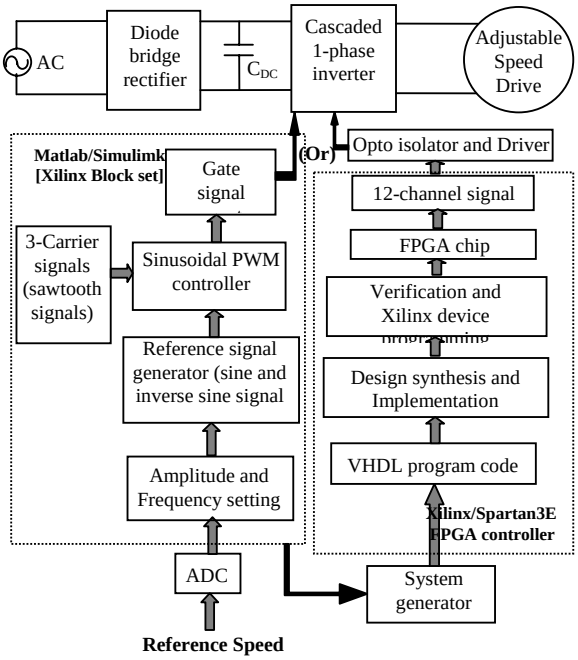

Fig 2 proposed block diagram of FPGA controller based cascaded multilevel inverter fed ASD

The three carrier signals (sawtooth waves) are generated using up-counter design. The first sawtooth carrier signal is generated from a 20-bit up-counter and this output signals is passed through 120^0 and 240^0 phase shift to form the second and third sawtooth carrier signals respectively. The two reference signals, sinusoidal wave and 180^0 phase shift sinusoidal wave are separately compared with three sawtooth carrier waves to generate 6-gate pulse signals. The widths of the pulses depend on the amplitude of the reference sinusoidal waves. The ratio of reference and carrier amplitude is called modulation index and it controls the output voltage of the inverter. This works as a sinusoidal PWM controller technique, so that the reference sinusoidal waves of frequency and amplitude can be easily adjustable according to the modulation index. The distribution unit of NOT gates deal with the

6-gate signals (produced from reference and carrier signals comparator) and it generates 12-gate signals [G1, G2, G3, G4, G5, G6, G7, G8, G9, G10,G11, and G12] for driving the cascaded multiple single-phase PWM inverter. The proposed digital controller can be tested and implemented in FPGA hardware by using two methods, (1) Matlab/System generator based Hardware-co-Simulation and (2) ISE/Xilinx-iMPACT [14-15].

Hardware-co-simulation:

System generator interfaces Xilinx/Spartan3E device FPGA hardware directly with simulink. The compilation target automatically generates a bit stream file of the design and dumps it into FPGA-kit. When the proposed controller design is simulated, the compilation portion is tested successfully through the JTAG connection of FPGA hardware in real time process.

ISE/ Xilinx-iMPACT:

The VHDL program code is generated from the system generator after the verification and simulation of the controller design. The VHDL program is synthesized using Xilinx-ISE 10.1 software. The ISE™ (Integrated Software Environment) based FPGA design flow comprises the following steps: 1) Design entry, 2) Design synthesis, 3) Design implementation, 4) Design verification, 5) Xilinx® device programming. The Xilinx device programming uses iMPACT to create a BIT file for debugging and downloads it into the target device XILINX/SPARTAN-3E FPGA.

Once the program is dumped to FPGA kit, it acts as a Sinusoidal PWM based FPGA controller and generates gate drive switching pulses. These pulses are connected to optoisolator circuit for preventing the ground sharing between the FPGA-processor and H-bridge power module. The output of optoisolator is connected through driver to each switching devices for controlling the PWM single-phase cascaded voltage source inverter.

4. Result and Analysis

The proposed single-phase cascaded multilevel PWM voltage source inverter is simulated using Matlab/Simulink power tools. The Xilinx Block set is a powerful graphical modeling tool which allows digital complex systems to be designed using a block diagram methodology. The system generator allows the modeling of digitized systems, which can be transformed into VHDL code and targeted at a Xilinx/Spartan3e FPGA board. Automatic generation of the bit stream is supported with the synthesis and implementation tools run within the simulink as well as Xilinx environment. The design is verified and tested both in Hardware-co-simulation and ISE/Xilinx -iMPACT. The system is investigated by resistive and inductive (RL-load) loads. The simulation results are investigated and the waveform of output voltage and load currents obtained contains fewer harmonic.

The desired reference speed rms value is converted to digital fixed point value for digital-design. The discrete reference value set the amplitude and the frequency according to voltage and frequency ratio. The amplitude and frequency with 14-bit ROM device are generated in two reference sinusoidal signals. These maintain the voltage to frequency ratio constant by controlling the output voltage of the cascaded inverter. Fig 3 shows the sinusoidal wave and 180^0 phase shift sinusoidal wave (inverse sinusoidal wave) as a reference signals.

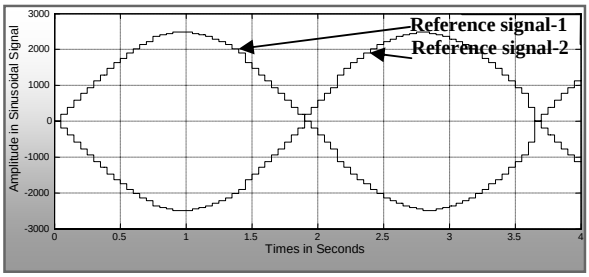

Fig 3 Reference sinusoidal signal

The three carrier signals (such as sawtooth waves) are generated using an up-counter design. The first sawtooth carrier signal is generated from 20-bit up-counter and these signals phase are shifted to 120^0 for second sawtooth carrier signals and 240^0 for third sawtooth carrier signals. Fig 4 shows each sawtooth wave starts from different amplitude with 120^0 phase shift. This sawtooth wave amplitude is -2500 V, -800 V, and +900 V to +2500 V.

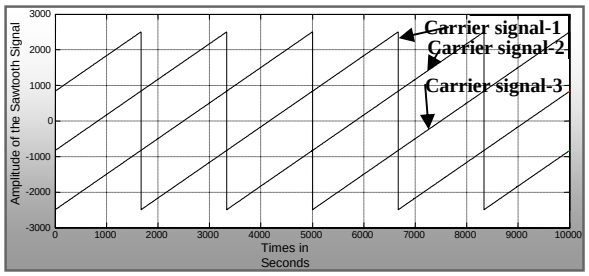

Fig 4 Three carrier sawtooth signals

The first reference sinusoidal signal is compared with the three sawtooth carrier signals, similarly the second 180^0 phase shift reference sinusoidal signal is also compared with the same three sawtooth carrier signals. Therefore, two sinusoidal signals are separately compared with three sawtooth signals to generate 6-gate signals. The distribution unit of NOT

gates deals with the 6- signals and generates 12-gate signals for driving the IGBTs switches. The Very high speed integrated circuits Hardware Description Language (VHDL) can be used to model a digital system at many levels of abstraction, ranging from the algorithmic level to gate level with high degree of complexity. Fig 5 shows the decimal value, bit waveforms of ADC reference speed value, amplitude and frequency. It also shows sinusoidal wave, 180^0 phase shift sinusoidal wave (inverse sinusoidal) for reference signals, up-counter, 120^0 phase shift up-counter and 240^0 phase shift up-counter for carrier sawtooth signals.

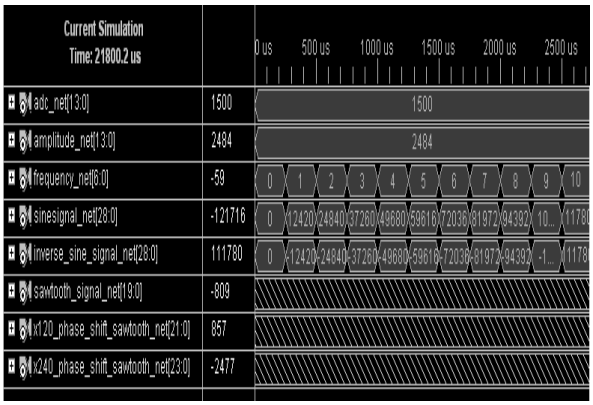

Fig 5 VHDL simulation result

The 12-channel gate control signals are generated from the comparison of two reference sinusoidal-signals and three carrier sawtooth-signals. The VHDL program generated from the system is generated using simulink platform. Fig 6 shows, 12-gate switching pulses and clock signals to drive the single-phase cascaded multilevel inverter for 7-level output voltage.

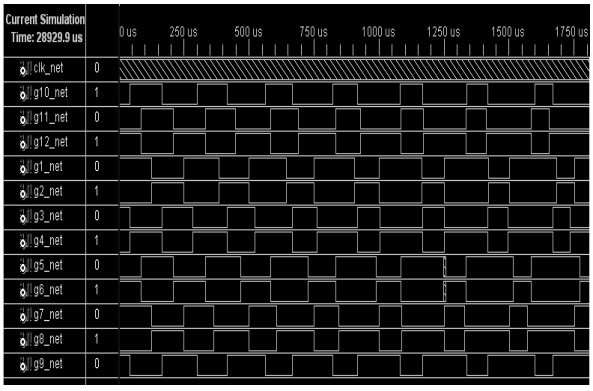

Fig 6 Twelve-channel gate drive pulses using VHDL code

The experimental setup using hardware-co-simulation is shown in Fig 7. The system generator provides the FPGA device interface through JTAG chain and USB. The JTAG options choose the boundary scan position as 1 and detect the IR length such as 6, 8 and 8. The platform USB cable speed is 12 MHz. The compilation target automatically generates a bit stream file and dumps it into FPGA kit. This hardware-co-simulation system clock frequency is set to 50 MHz at pin location C9. The proposed controller design is simulated and compilation portion is tested successfully through the FPGA hardware in real time process.

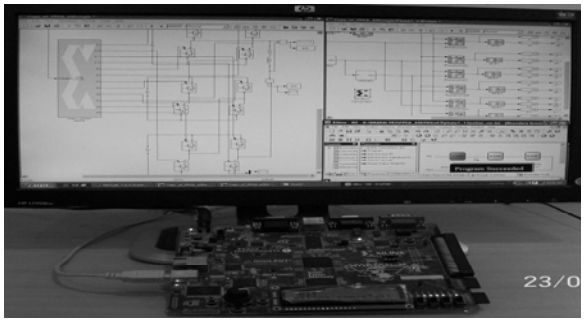

Fig 7 Experimental setup using Hardware-co-simulation

The FPGA board generates 12-channel gate signals that drives the cascaded single-phase multilevel voltage source inverter IGBT switches and produces 7-level output voltage as shown in Fig 8. The output voltage levels are 3Vdc, 2Vdc, Vdc, 0, -Vdc, -2Vdc and -3Vdc. Here each phase output voltage Vdc is 50 V.

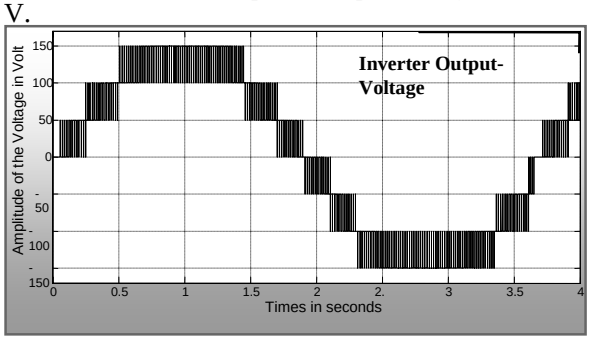

Fig 8 output voltage of 1-phase cascaded inverter

The 7-level cascaded single-phase multilevel voltage source inverter output current is shown in Fig 9. This topology provides nearly sinusoidal current waveforms that claim low distortion and less switching losses.

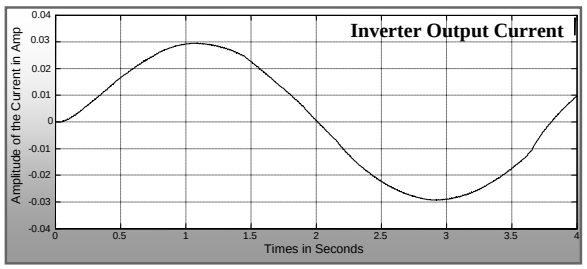

Fig 9 output current of 1-phase cascaded inverter.

The Fourier analysis of the cascaded multilevel inverter output voltage signal is observed in one cycle of the fundamental frequency. Fig 10 shows single-phase cascaded multilevel PWM inverter output voltage in order of harmonic content measured with respect to the fundamental frequency.

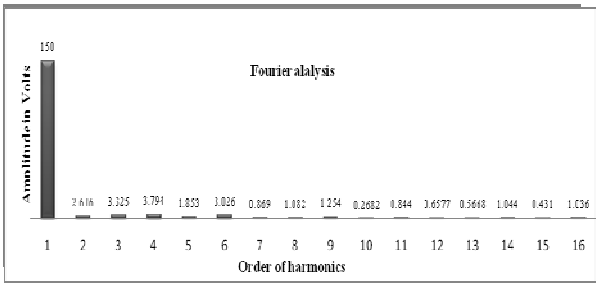

Fig 10 order of harmonic measurement

The single-phase cascaded multilevel voltage source inverter of the total harmonic distortion is calculated by periodic distorted signal. The current and voltage of the THD is measured and presented in Table 2.

Table 2 THD measured of the single-phase cascaded VSI

THD	cascaded multilevel VSI
Voltage	19.31%
Current	3.854%

5. Conclusions

The sinusoidal PWM technique is adopted with FPGA to generate switching patterns. These switching pulses are applied to the cascaded multilevel inverter to generate 7-level output voltage. This controller design is simulated and compilation portion is tested through FPGA in real time process using hardware-co-simulation. FPGA enables easy, fast and flexible implementation of the controller circuit in hardware. It can adjust effectively the modulation index range for varying speed control of induction motor drive. The effective controller maintains the voltage to frequency ratio constant. The simulation with experimental results demonstrates quality of voltage and current waveforms with less harmonic content at the output of the cascaded inverter. These inverter topologies with digital-control circuit can be used for speed control of induction motor and other medium scale industrial applications.

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