PWM CONTROL FOR HYBRID CLAMPED MULTILEVEL INVERTERS

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Abstract—A hybrid clamped multilevel inverter topology comprising active and passive clamping devices is presented in this paper. In this topology, the dc-link capacitor voltages can be balanced without additional circuitry or separated dc voltage sources, regardless of load characteristics. It can be used in real and reactive power conversion applications. The topology structure, operating principle and self-voltage balancing ability are analyzed. The PWM control method called higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) is employed for the hybrid-clamped multilevel inverter and it is based on the improvement of carrier phase disposition PWM (PDPWM). In this paper, the generated triangular carrier cells are made to have opposite phases with its neighbor carrier cells by 180˚. This method can effectively reduce the number of devices switching on or off within broad modulation index range, consequently reducing switching losses, and remarkably reduce the amplitude of lower harmonics. Simulation results of five-level inverter are also presented.

Keywords- Hybrid clamped multilevel inverters, pulse width modulation, switching.

I. INTRODUCTION

Multilevel inverters have been a research hotspot in high-voltage and high-power applications in recent years because of their advantages: low output total harmonic distortion (THD), low voltage stress of devices, and low system electromagnetic interference. The research on multilevel inverters focuses on two aspects: topologies and control methods. In this paper hybrid clamped multilevel inverter is employed and higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) control technique is implemented.

Multilevel inverter is an alternative structure to the conventional power converter that have been accepted and used in many applications such as motor drives and static power conditioning systems [1]. Multilevel inverter's operation depends on the structure and the number of the power switches in the inverter circuit. The level starts from three level and it can have unlimited number of voltage levels. By increasing the number of the power switches in the circuit, the performance of the inverter can be improved.

The number of power switches in the multilevel inverter will determine the number of level in the output voltage at the load. As the number of power switches used in the multilevel inverter increases, the staircase voltage level at the load also will increase. The main feature of the multilevel inverter is it has the ability to reduce the voltage stress on each of the power switches due to the utilization of the multiple levels in DC bus of the circuit [2]. This is important especially when a high DC side voltage is imposed by the load to be applied to the multilevel inverter [3].

Furthermore, smaller distortion in the multilevel inverter AC side waveform can be achieved even though at low switching frequency. The multilevel inverter has another benefit such that the switching losses in the inverter are reduced by the increased flexibility of the voltage waveform produced by increasing the number of voltage levels [4]. The circuit also permits the existing power switches to be used in systems where voltages higher than the individual switch rating are applied to the load [5].

PWM technique is used to generate the carrier cells in this paper. There are three alternative PWM strategies with different phase relationships namely APOD(Alternate

Phase Disposition), POD(Phase Opposition Disposition), PD(Phase disposition). In APOD, every carrier waveform is in out of phase with its neighbor carrier by 180˚. In POD, all carrier waveforms above zero reference are in phase and are 180˚out of phase with those below zero level. In Phase disposition (PD) method, all carrier waveforms are in phase. In this paper, the generated triangular carrier cells are made to have opposite phases with its neighbor carrier cells by 180˚ (APOD) thereby it reduces the switching transitions.

There are three main type of the multilevel inverter topology; Diode Clamped Multilevel Inverter (DCMI), Flying Capacitor Multilevel Inverter (FCMI) and Cascaded Multilevel Inverter (CMI). To synthesize multilevel output, voltage clamping is one of the most important issues. The meaning of clamping is to limit the switch's terminal voltage in a suitable range by using clamping devices. In the three existing multilevel-inverter topologies, it can be seen through their names that voltages are clamped by diodes in the diode-clamped multilevel inverter, by using capacitors in the flying capacitor multilevel inverter, and by the usage of separate voltage sources in the cascaded multilevel topology. However, the three topologies have some disadvantages in real applications.

The diode-clamped multilevel inverter needs separate dc source and requires complex control methods when real power is delivered [2], [3]. Although the flying-capacitor inverter can be used in both real and reactive power conversions, it is difficult to balance the capacitor voltages when it is used for reactive power compensation [4]. The cascaded multilevel inverter needs separate voltage sources and therefore, they are more suitable for renewable energy sources such as fuel cell, photovoltaic, biomass, etc. To overcome the above disadvantages, it is an instructive idea to find new multilevel-inverter topologies with higher performance by changing clamping devices. All the three existing multilevel inverters use only one type of clamping devices in one topology. If two or more types of clamping devices are used in one topology, a series of new multilevel-inverter topologies can be derived.

II. HYBRID CLAMPED MULTILEVEL INVERTER

A. STRUCTURE CHARACTERISTICS

Fig. 1 shows one leg of the proposed hybrid-clamped five level inverter. In this topology, switching devices Sa1–Sa4 and Sa1'–Sa4' are the main switching devices used to produce the desired output voltage. Sc1–Sc6 are the clamping switching devices, and Dc1–Dc12 are the clamping diodes. The switching devices Sc1–Sc6 and the auxiliary capacitors C5–C7 maintain the dc-link capacitor voltages in balance. It can be seen from Fig. 1 that only the clamping devices nearest to the dc side are active switches with anti-parallel diodes, while others are only diodes. Also, only the flying capacitors nearest to dc side exists. This topology is simple to be expanded to any voltage levels. For one leg of this M-level topology, (M − 1) dc-link capacitors, 2(M − 1) main switching devices, 2(M −

2) clamping switching devices, (M − 1) x (M − 2) clamping diodes, and (M − 2) auxiliary capacitors are needed. All the capacitors sustain the same voltage, and all the switching devices and diodes have the same voltage stresses.This is the concept of hybrid clamped method.

B. MULTILEVEL SYNTHESIS PRINCIPLE

The multilevel synthesis principle is explained in this section. The dc bus negative point is taken for reference. Redundant switching states exist for middle voltage levels in the hybrid-clamped topology. Five voltage levels are produced by the following switching states correspondingly.

1) For voltage level U1 = 0Udc, four main switches Sa4', Sa3', Sa2', Sa1' and three clamping switches Sc1, Sc3 and Sc5 are turned on.
2) For voltage level U2 = 1Udc, the following are the two switching states.
   a) Four main switches Sa4, Sa4', Sa3', Sa1' and three clamping switches Sc1, Sc3 and Sc5 are turned on.
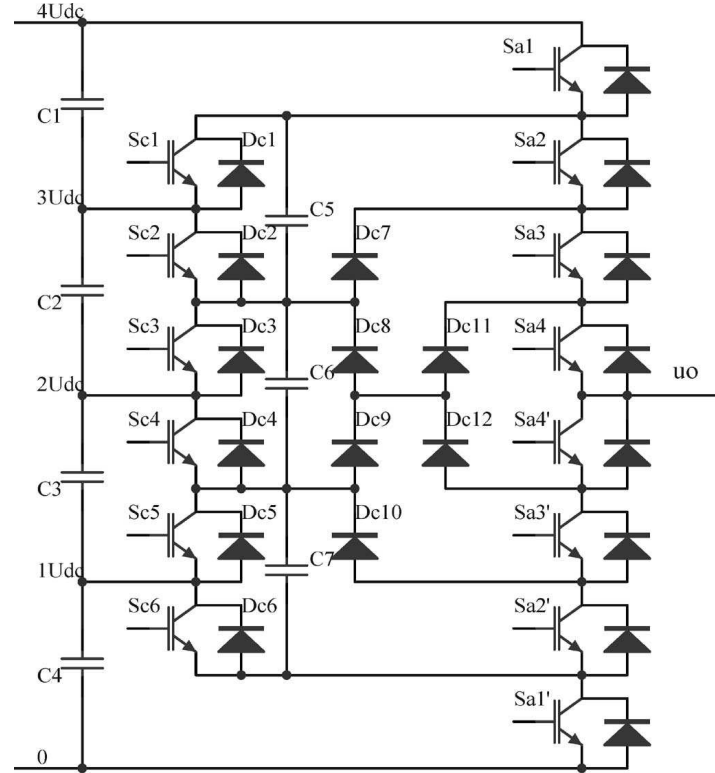   b) Four main switches Sa1, Sa4', Sa3', Sa2' and three clamping switches Sc2, Sc4 and Sc6 are turned on.

Fig. 1. One leg of five level hybrid clamped inverter

3) For voltage level U3 = 2Udc, the following are the two switching states.
   a) Four main switches Sa3, Sa4, Sa4', Sa1' and three clamping switches Sc1, Sc3 and Sc5 are turned on.

b) Four main switches Sa1, Sa4, Sa4', Sa3' and three clamping switches Sc2, Sc4 and Sc6 are turned on.

4) For voltage level U4 = 3Udc, the following are the two switching states.

a) Four main switches Sa2, Sa3, Sa4, Sa1' and three clamping switches Sc1, Sc3 and Sc5 are turned on.

b) Four main switches Sa1, Sa3, Sa4, Sa4' and three clamping switches Sc2, Sc4 and Sc6 are turned on.

5) For voltage level U5 = 4Udc, four main switches Sa1, Sa2, Sa3, Sa4 and three clamping switches Sc2,Sc4 and Sc6 are turned on.

The switches (Sa1, Sc1), (Sc1, Sc2), (Sc2, Sc3), (Sc3, Sc4), (Sc4, Sc5), (Sc5, Sc6), and (Sc6, Sa1') are in parallel with capacitors C1, C5, C2, C6, C3, C7, and C4, respectively. The switches should be complementary switching pairs, i.e., when one switch is on, the other is off, and vice versa.

It can be seen from the above analysis that the switching operation of a hybrid-clamped five-level inverter must comply with the following rules.

1) For each switching state, there must be four main switching devices and three clamping switching devices on.

2) Sa1 is complementary with Sa1'. Except for Sa1 and Sa1', any three adjacent main switching devices are on or off simultaneously. Therefore, (Sa1, Sa1'), (Sa2, Sa4'), (Sa3, Sa3'), and (Sa4, Sa2') are the complementary switching pairs, i.e., if one is on, the other must be off and vice versa.

3) Sa1 and Sc1 are complementary.

4) Any two adjacent clamping switching devices Sc1–Sc6 are complementary.

III. SELF VOLTAGE BALANCING

The self-voltage balancing ability of the hybrid clamped topology is realized through clamping switching devices and auxiliary capacitors. When the multilevel converter switches from one state to another, two different groups of capacitors are connected through clamping switching devices. All the states of the clamping switching devices can be determined from Sa1. It can be seen that there are two switching states for each of the middle voltage level. In one state, Sa1 is on, and in the other state, Sa1 is off. For the state that Sa1 is on, Sc2, Sc4, and Sc6 should also be on according to the switching operation rules specified under the multilevel synthesis principle. Then, capacitors C1 and C5, C2 and C6, C3 and C7 are in parallel, respectively, so the two parallel capacitors will be charged and discharged to keep their voltages equal: $U_{c1} = U_{c5}$, $U_{c2} = U_{c6}$, $U_{c3} = U_{c7}$; for the other state that Sa1 is off, capacitors C2 and C5, C3 and C6, C4 and C7 are in parallel respectively, so the two parallel capacitors will be charged and discharged to keep their voltages equal: $U_{c2} = U_{c5}$, $U_{c3} = U_{c6}$, $U_{c4} = U_{c7}$. That is to say, the clamping

capacitors can be charged or discharged according to the voltage difference between the two parallel capacitors. In addition, the objective of the clamping capacitor voltage is to maintain a stable voltage level so that all the dc-link capacitors can keep their voltages balanced through the auxiliary capacitors C4, C5, and C6.

This voltage balancing method is different from the one that utilizes redundant switching states. The redundant-switching state method means selecting two or more switching states in one period to produce one neutral-point voltage, in some switching states, the dc-link capacitors are charged and in other states are discharged. Then, in one particular period, the capacitor voltages can keep their balance by charging and discharging. The typical application of this method is the phase shift pulse width modulation (PWM) used in flying-capacitor multilevel converters [7]. However, it is difficult for the dc-link capacitor voltages to be balanced in pure reactive applications. In this topology, the auxiliary capacitors act as intermediate, which are in parallel with different dc-link capacitors in different switching states. Therefore, the neutral-point voltages can be kept balanced regardless of the load characteristics. In addition, this topology can be used in real and reactive power applications with simple control.

In this topology, all the main switches are clamped to the corresponding dc-link capacitors by active clamping switches and passive clamping diodes. Each of the main switches and clamping diodes are clamped to C5, C6, and C7, and then they are clamped to the corresponding dc-link capacitors according to the switching states of clamping switches. For example, if Sc1, Sc3, and Sc5 are on, the main switches and clamping diodes are clamped to C2, C3, and C4; if Sc2, Sc4, and Sc6 are on, the main switches and clamping diodes are clamped to C1, C2, and C3. When Sa1 is turned off, it is clamped to C1 directly through Sc1; when Sc1, Sc3, and Sc5 are turned off, they are clamped to C1, C2, and C3, respectively, through Sa1, Sc2, and Sc4; when Sc2, Sc4, and Sc6 are turned off, they are clamped to C2, C3, and C4, respectively, through Sc3, Sc5, and Sa1'; when Sa1' is turned off, it is clamped to C4 directly through Sc6. Thus, all the devices are clamped to the corresponding dc-link capacitors by active switches and passive diodes.

Active switching devices, diodes, and capacitors can be used for clamping. The main functions of the clamping devices are summarized as follows.

Diodes have the characteristics of unidirectional conduction, so they can be used for unidirectional clamping.

Active switches are controllable devices, so they are more flexible than diodes for clamping. A switching device with a parallel diode can provide a bidirectional path by itself, and it can realize main switch and flying capacitor clamping. Capacitors are electrical energy storage passive components and they participate in voltage synthesizing and sustaining the capacitor voltage by charging and discharging or by clamping.

All the three types of devices can be used for clamping. With the different places in the topology, they may change their effects correspondingly. Considering the functions replacement among different clamping devices and based on the concept of hybrid clamped, a series of novel multilevel converter topologies can be deduced.

IV. PRINCIPLE OF HLCCAPOPWM CONTROL

The PWM control method called higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) is employed for the hybrid-clamped multilevel inverter and it is based on the improvement of carrier phase disposition PWM (PDPWM) [1]. The carrier phase disposition PWM (PDPWM) method is a traditional control strategy for multilevel converters. The carrier waveforms of every switching device are positioned on the same carrier band. If the carrier waveforms are divided up according to the carrier period, then the individual triangle wave, which is called "carrier cell," can be obtained. In this method, the special carrier waveforms of switching devices are split into many triangle carrier cells according to the carrier period. By inverting some carrier cells, the new carrier waveforms can be constructed and a PWM control method called higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) can be obtained.
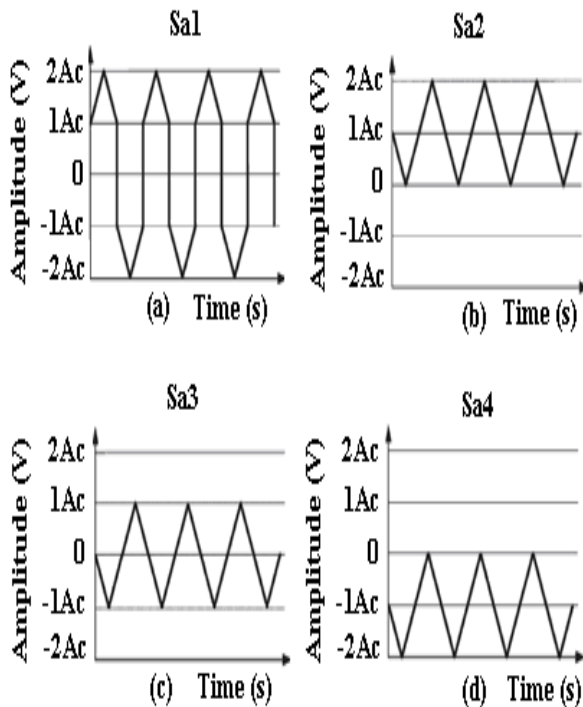

Fig. 2. Carrier waveforms for switching devices (a) Carrier of Sa1 (b) Carrier of Sa2 (c) Carrier of Sa3 (d) Carrier of Sa4

Combining two kinds of switching states, the carrier waveforms of the upper four main switching devices Sa1, Sa2, Sa3, and Sa4 as shown in Fig. 2, can be produced and Sa1', Sa2', Sa3' and Sa4' are complimentary with Sa1, Sa4, Sa3, and Sa2 respectively.

For Sa1, the higher carrier cells are positioned on the first carrier band and the lower ones on the fourth carrier band. For Sa2, the higher carrier cells are positioned on the first carrier band and the lower ones on the second carrier band. For Sa3, the higher carrier cells are positioned on the second carrier band and the lower ones on the third carrier band. For Sa4, the higher carrier cells are positioned on the third carrier band and the lower ones on the fourth carrier band.

V. ANALYSIS ON THE NUMBER OF SWITCHING STATES

With the HLCCAPOPWM control method, the number of device switching on or off in one unit of time can be reduced with broad modulation index range, thereby the switching losses are reduced and hence the efficiency is improved.

In the high modulation index i.e., m > 0.5, the modulation wave intersects every carrier band. For Sa1 and Sa2 with the HLCCAPOPWM method, the higher carrier cells are all positioned on the first carrier band, so the modulation wave intersects the higher carrier cells. Therefore, the number of device switching on or off with the HLCCAPOPWM method is much less than that with the PDPWM method. For Sa3 and Sa4 with the HLCCAPOPWM method, the higher carrier cells are, respectively, positioned on the second and third carrier bands. These two carrier bands intersect by only a little part of the modulation wave. However, compared with the PDPWM method, the number of devices switching on or off is still reduced.

In the low modulation index, i.e., m < 0.5, the modulation wave intersects the second carrier band and the third one. For Sa1 and Sa2, the modulation wave does not intersect any high carrier cells, so the PWM pulse waveforms with HLCCAPOPWM method and the PDPWM method are identical, which means that the number of device switching on or off with the HLCCAPOPWM method is the same as that with the PDPWM method. For Sa3, during the second half-modulation period, the modulation wave intersects the lower carrier cells, therefore the PWM pulse waveform with those two kinds of PWM methods are identical, then the number of device switching on or off with the two methods are also identical. During the first half modulation period, the modulation wave intersects the higher carrier cells, so the number of device switching on or off with the HLCCAPOPWM method is remarkably reduced, about half the number with the PDPWM method. For Sa4, during the first half-modulation period, the modulation wave does not intersect any carrier cells, so the number of device switching on or off with the HLCCAPOPWM method is the same as that with the PDPWM method. During the second half modulation period, the modulation wave

intersects the higher carrier cells, so the number of device switching on or off with the HLCCAPOPWM method is also remarkably reduced, about half the number with the PDPWM method.

VI. SIMULATIONS

In this section, the simulink diagram for carrier wave and PWM pulse generation is presented. Also the simulink diagram for hybrid clamped multilevel inverter and the obtained results are presented. The carrier waveforms for four main switches are shown in Fig. 3.

The simulink diagram for PWM pulse generation is shown in Fig. 4. The pulses for four main switching devices Sa1, Sa2, Sa3 and Sa4 are shown in Fig. 5. The pulses for the switching devices Sa1', Sa2', Sa3' and Sa4' are obtained from the pulses for Sa1, Sa2, Sa3 and Sa4 since Sa1 is complementary with Sa1' and Sa2 is complementary with Sa4' and Sa3 is complementary with Sa3' and Sa4 is complementary with Sa1'. The pulses for switching devices Sa1', Sa2', Sa3' and Sa4' are shown in Fig. 6.
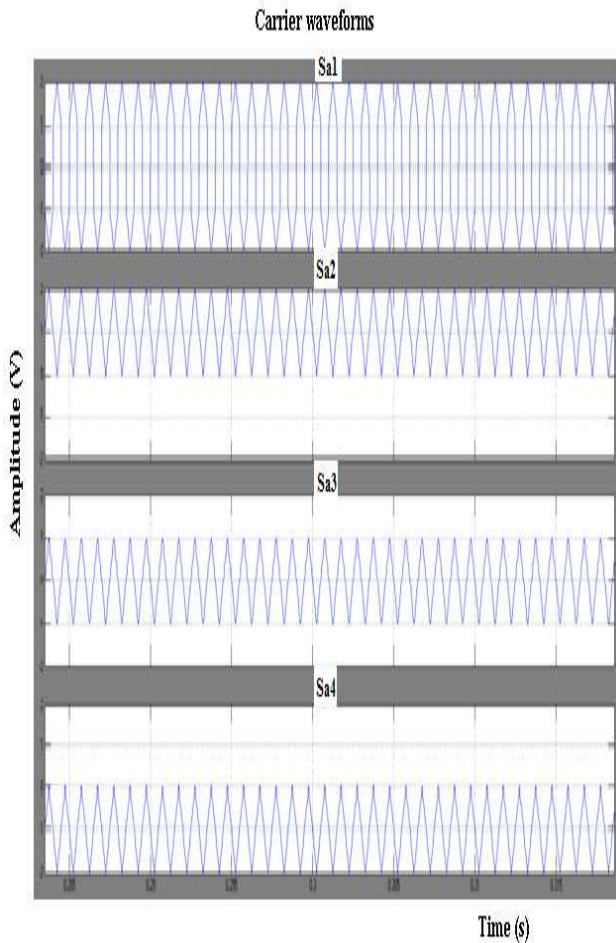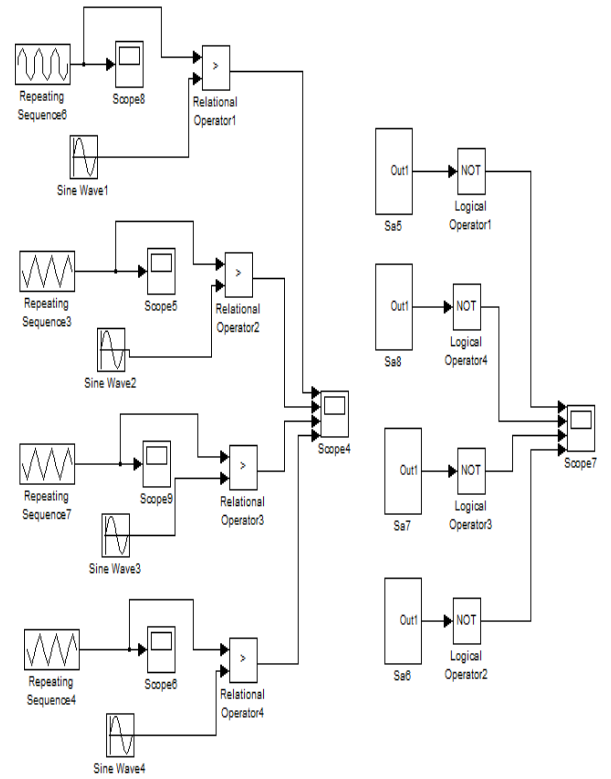

Fig. 4. Simulink diagram for pulse generation

Fig. 3. Carrier waveforms for Sa1, Sa2, Sa3 and Sa4
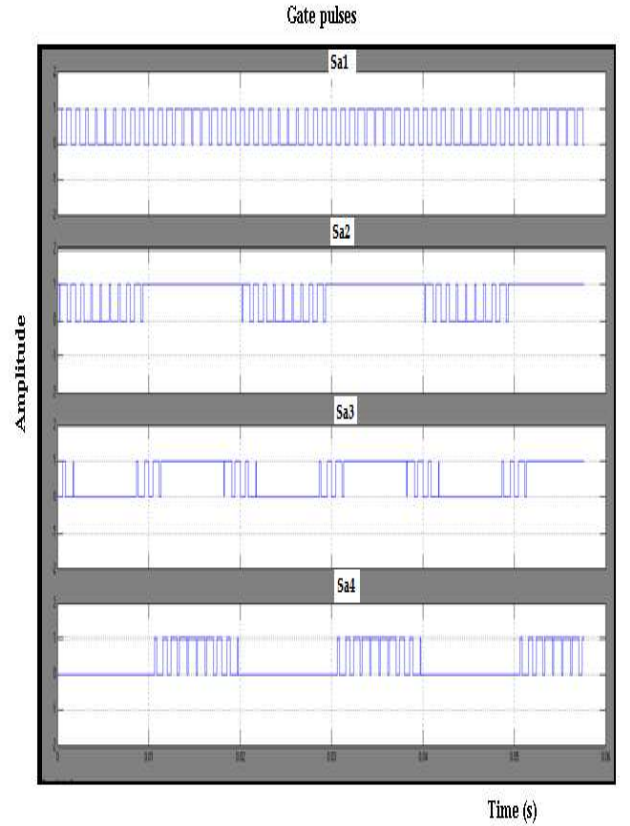

Fig. 5. Gate pulses for Sa1, Sa2, Sa3 and Sa4
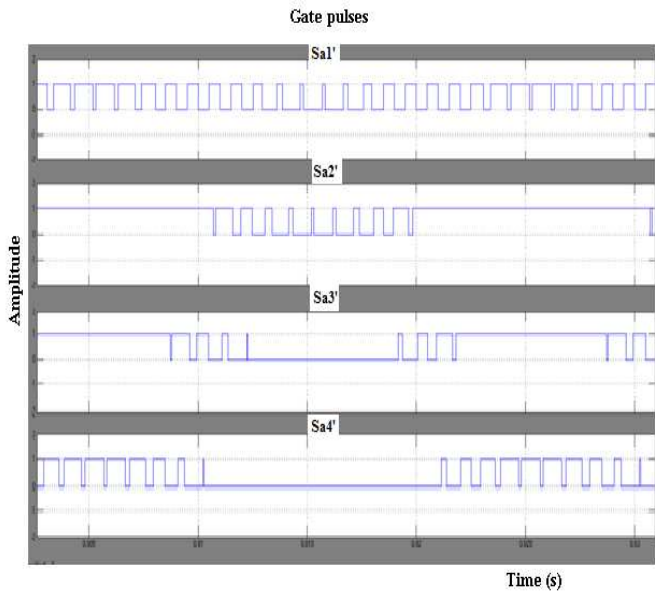
Gate pulses

Fig. 6. Gate pulses for Sa1', Sa2', Sa3' and Sa4'

The simulink diagram for hybrid clamped five level inverter is shown in Fig. 7 and the output voltage is shown in Fig. 8. The neutral point of dc-link capacitors is taken as the reference point, and the output terminal connects with load and the load considered here is 50Ω resistive load. All the capacitors have the same capacitance of 1100 μF.
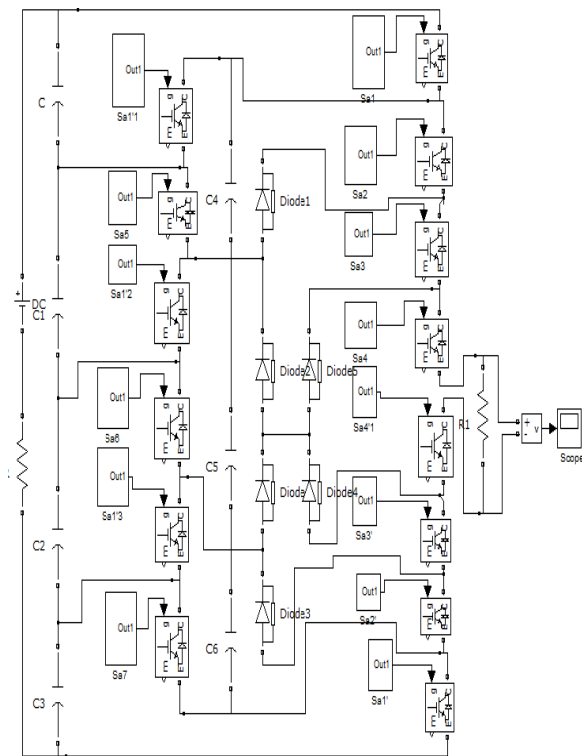

Fig. 7. Simulink diagram for hybrid clamped five level inverter

VII. CONCLUSION

Higher Lower Carrier Cells Alternate Phase Opposition Pulse Width Modulation (HLCCAPOPWM) control is employed for the hybrid clamped five level inverter. This control technique effectively reduces the switching transitions and hence reducing the switching losses, thereby improves the efficiency of the inverters. This technique can be applied to n-level inverters. The output voltage is obtained without any voltage spikes. The operating principle and dc-link capacitor voltage-balancing ability are studied, and the validity is proved by simulation results. Clamping mechanism of diodes and switches is also studied.
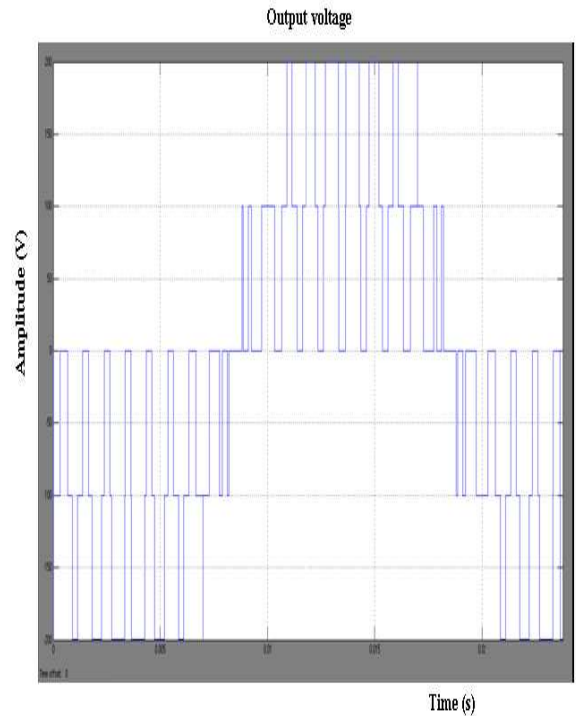

Fig. 8. Output Voltage

Diodes, active switches and capacitors are used for clamping purpose. With these devices in different places in the topology, they may change their effects correspondingly. Considering the functions replacement among different clamping devices and based on the concept of hybrid clamped, a series of novel multilevel inverter topologies can be deduced.

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