Design and Validation of a SOGI - PLL by Using a PR Controller based on Hardware-In-The-Loop Test-Bed

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Abstract - This paper discusses the improved performance of steady state accuracy in the estimation of frequency, phase of an input signal and amplitude. An approach of using a real time simulation for a second order generalized integrator - phase locked loop (SOGI-PLL) using a Proportional-Resonant (PR) controller as its loop filter with Hardware-In-The-Loop (HIL) testing is discussed. In order to enhance the performance of phase and frequency tracking, PR controller is suggested in this paper. The mathematical model and its analysis of single-phase SOGI-PLL with PR controller is developed along with the real time simulation that is built based on DSPACE platform. The I/O Interface and DSPACE itself meets the operational features of the proposed method. Various tests are performed under abnormal grid conditions like frequency deviations, voltage sag and phase jump by connecting them for a closed loop HIL testing. The HIL system validates the practicability of the propsed system and its functions. The simulation is carried out using MATLAB/Simulink.

Keywords — Phase - Locked Loop (PLL), Second Order Generalized Integrator (SOGI), Proportional-Integral (PI) Control, Proportional-Resonant (PR) Control, Hardware-in-the-Loop (HIL).

I. INTRODUCTION

Phase-Locked Loops are playing a major role in grid interconnection for efficient phase angle tracking capability in converters, active power filters, UPS applications, controlled rectifiers, distributed generation and also for FACTS devices [1]-[2]. The Phase-Locked Loops (PLL) will estimate the phase angle accurately because of its merits like speed of response for disturbances like phase, frequency and voltages, steady state phase angle error and harmonic rejection.

Many topologies on PLL's have been introduced for three - phase and also for single - phase systems [3]-[5] detecting the amplitude, frequency and phase angle for grid-tied systems. The synchronous reference frame (SRF) based PLL is performing well under ideal grid conditions but has poor performance under utility grid distortions [9]. *Saeed Golestan* and *Josep M. Guerrero* analyzed the structures of various Phase Locked Loops namely SOGI, Modified Power – based PLL and Park PLL [10]. But, the steady state error response is found slower. The PLL basic function is to respond effectively by detecting the phase angle and amplitude at a faster rate in distorted utility conditions. *S.M Silva* addressed the most recurrent algorithms on single-phase grid connected systems [11]. *Mihai Ciobotaru* has developed the most fundamental orthogonal signal generation structure based on SOGI. But, the tuning depends on frequency, hence problems occurs when there are frequency fluctuations. Phase angle estimation can be done by either open loop method or closed loop methods [12]-[14].

Due to the dynamic response of the integral term in the PI controller, It is unable to track the sinusoidal reference accurately and cannot perform under lower order harmonics due to the limitation in its bandwidth. This shortcome in the PI controller can be overcomed with the PR control which resonates at the resonant frequency because of no gain exists at other frequencies

[15]. In order to improve the performance of the PI controller, many changes in the controller like increasing the gain, multi state feedback and feed forward path are introduced. But, all these changes are increasing the bandwidth of the system and causing to violate the stability limits and also causing much more computational burden. A similar type of response with low cost, complexity and precise control can be achieved using a PR controller [16]-[17]. For eliminating the steady state error, the PR controller resonates at selected resonant frequency by introducing an infinite gain[18]-[19]. The PR controller has high computational efficiency with faster response. This controller performs well under system parameter variations and also less dependent on system model.

This paper focuses on the performance improvement of second order generalized integrator by using PR controller instead of PI control for achieving the better steady state accuracy under adverse grid conditions. Many PLL's are reported in the literature but, no comprehensive design procedure is found to fine tune the PD as well as Loop Filter parameters. Some design procedures are available in the literature but, the procedure is not synchronized with the PD, LF and VCO [29]-[30]. Therfore, these approaches are unable to extract the exact values out of PLL potentialities.

Therefore in this paper, a simple method is adopted which simplifies the paprameter design and stability analysis. The parameter guidelines are also suggested for fast transient response, stability, robust performance and high disturbance rejection capability.

MATLAB/Simulink platform is used for software simulation. If, accurate and real time simulation is required then the software simulation is not enough to prove the proposed method. In order to improve the accuracy, A Hardware – In – The – Loop testing is done with the help of Dspace.

The scope of this paper is to provide a real time Dspace based test platform for the proposed SOGI method. It increases the safety of entire system by avoiding the risk of damaging real time prototypes. Because, HIL testing allows tests beyond normal operation that can reveal if the system can safely operate. This paper presents both HIL simulation and MATLAB based Simulation.

This paper is further organized as follows: In Section II, A brief introduction to the Basic PLL is discussed, In section III, The proposed SOGI-PLL is analyzed in detail. In section IV, The design of Loop Filter i.e; Proportional – Resonant Controller is explained clearly. Section V explains the HIL simulation including the DSPACE based architecture with its advantages. Finally, MATLAB and HIL simulation results are presented and validated under abnormal grid conditions in section VI and the conclusions are made in section VII.

II. Basic Phase – Locked Loop

The block diagram of the basic PLL is shown in **Fig.1.** This system has simple structure with digital and analog simplifications based on feedback method and dq transformations and is mostly accepted. The output signal has information about fundamental positive sequence component, frequency and amplitude. Therefore, It is also called as Positive Sequence Detector **(PSD)**. The basic Phase Locked Loop comprises of three building blocks as shown in Fig.1. The Phase Detector (PD) shown in fig.1 generates a signal which is the difference in feedback signal and phase between the input and then it is supplied to the loop filter (LF). The Loop Filter is used to control and serves as input to the the Voltage Controlled Oscillator (VCO). The VCO the generates the estimated frequency from its nominal frequency signal [7]. Since the method is a closed loop system, the output signal is optimally matches with the fundamental input signal such that the phase and frequency can be estimated with high accuracy. This method have satisfactory performance in both steady state and dynamic conditions but the basic PLL suffers from the disadvantage in unbalanced / distorted grid conditions. Hence, an effective research is carrying out by many researchers to overcome the disadvantages.

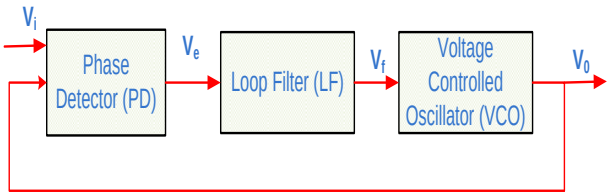


Fig. 1 Block Diagram of Basic PLL

In general, The tracking technique has to provide:

- The capability to detect and follow the grid voltage under Sag and Swell conditions.
- The ability to maintain accuracy under grid frequency step responses.
- Robustness with respect to transient and steady state disturbances.
- High filtering from harmonic distortions.
- Easy implementation in both software and hardware.

In this Paper, The PD stage is the main topological difference between several Phase Locked Loops. Hence, the research is diverted from PD to the LF for achieving high steady state accuracy. Furthermore, a PR controller based solution will be presented. The dynamic response of the SOGI PLL is also studied by taking into account aspects such as: Steady state error, disturbance rejection, settling time and overshoot [20].

III. Second Order Generalized Integrator

This paper presents a Phase-Locked Loop (PLL) based on SOGI that detects the positive sequence component from the input signal by involving the quadrature signal generation (QSG). The design of a Quadrature Signal Generation (SOGI-QSG) is shown in **Fig.2.** The input signal represents the grid voltage measured at the point of common coupling (PCC). The output signals are two sine waves that are generated with a phase shift of 90^0. The component V_α has the same magnitude and phase as that of the input signal and V_β has the phase difference of 90^0 w.r.t input signal.

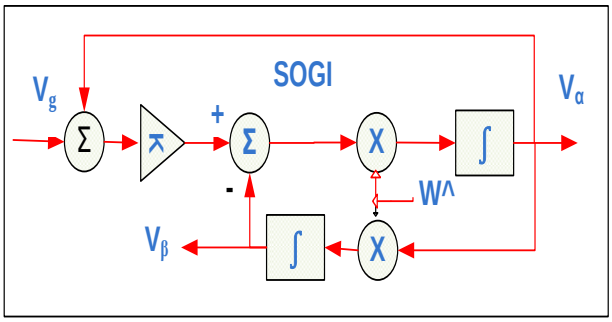


Fig. 2. Circuit Diagram of SOGI-QSG.

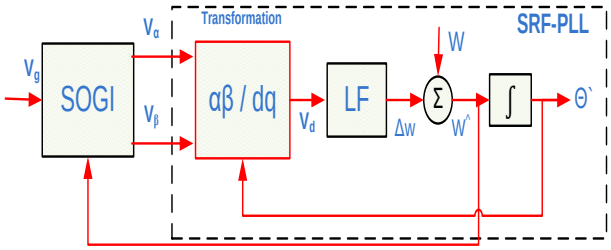


Fig.3. Closed Loop Diagram of SOGI-PLL

The *k* shown in **fig.2** is known as damping factor. The response and level of fitering is decided by the damping factor. The bandwidth of the closed-loop system is affected with the decrease in *k* and the dynamic response become slower. The bandwidth equal to two times of the damping ratio (2δ) is to be choosen for better response. The bandwidth response with unit signal for several values of *K* is shown in **Fig. 4.** For K=1.6 the response was good and fast (< 2ms). V_g (s) is the grid voltage, θ` and $\hat{W}$ is the estimated angle and frequency respectively and W is the reference frequency. The SOGI structure is frequency dependent, hence, problems may occur when the grid frequency has fluctuations. Therefore, the $\hat{W}$ of the SOGI structure is to be tuned according to the nominal frequency provided by the PLL structure as shown in **Fig. 3.**

Two sine waves V_α and V_β are produced with a phase difference of 90^0 as shown in **fig 3.** The SOGI is acting as a band pass filter with an infine gain and is defined as:

$$SOGI(s) = \frac{\hat{W}s}{s^2 + \hat{W}^2} \quad \textbf{(1)}$$

The transfer functions based on closed-loop shown in **fig.3** are described as follows:

$$G_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\hat{W}s}{s^2 + k\hat{W}s + \hat{W}^2} \quad \textbf{(2)}$$

$$G_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k\hat{W}^2}{s^2 + k\hat{W}s + \hat{W}^2} \quad \textbf{(3)}$$

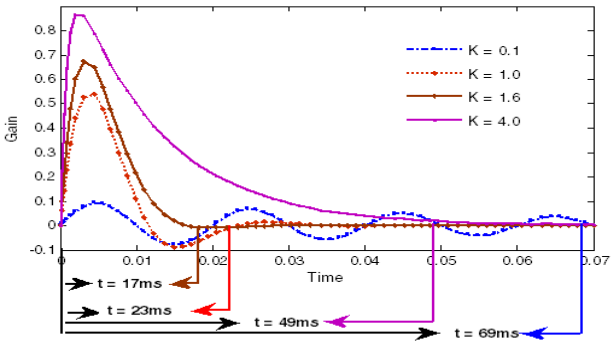


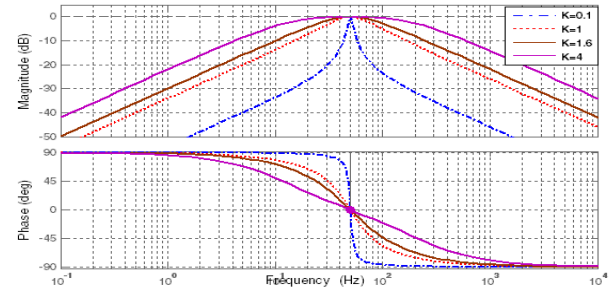
Fig. 4. Bandwidth Response for Various Values of K.

The Bode plots from the transfer functions of (2) & (3) are shown in **Fig. 5(a) & 5(b)** for various values of *k*. In order to get a balanced set of in-quadrature outputs with exact amplitudes, the SOGI frequency must be equal to the input fundamental frequency [20]. Park transformation is used to convert αβ to dq.

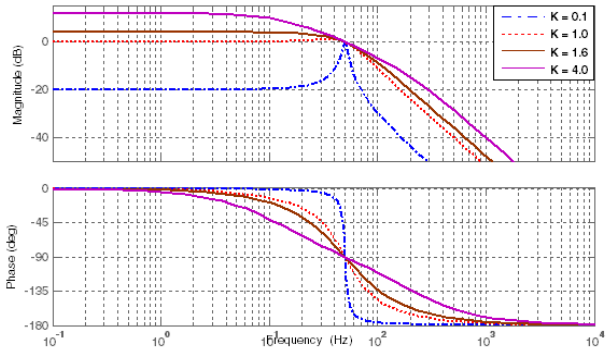
$$T = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \quad \textbf{(4)}$$

The transformation output V_d is used to eliminate high frequency noises by passing it through a Loop Filter (LF) and the estimated phase angle $\hat{\theta}$ is generated by adding fundamental frequency (W). In order to have a balanced set of In-phase and quadrature outputs with exact amplitudes, the frequency of the SOGI must be equal to the fundamental frequency (W = 2π * 50). In **Fig. 3,** The basic loop filter is a Proportional – Integral Controller and

is replaced with the Proportional – Resonant Controller to overcome the disadvantages in it. The response of PI controller under distorted grid conditions is slower than that of PR controller. It is observed that the DC quantities in the synchronous frame are appeared in the output fundamental term and also contribute to harmonics. This can be avoided by an alternate approach of using a Proportional Resonant controller as Loop Filter.



(a)



(b)

Fig. 5. a) $G_{\alpha}(s)=\frac{V_{\alpha}(s)}{V_g(s)}$ **, b)** $G_{\beta}(s)=\frac{V_{\beta}(s)}{V_g(s)}$

IV. PROPORTIONAL RESONANT CONTROLLER

In general, stability analysis is done for a PIcontroller based on extended symmetrical optimum method to achieve maximum possible stability margin for the PLL. A classical PI Controller $G_{PI}(s)$ can be expressed by:

$$G_{PI}(s)=K_P+\frac{K_I}{s} \qquad \textbf{(5)}$$

Where, K_P is the Proportional Gain and K_I is the Integral Gain of the transfer function. The equivalent of (5) in stationary frame is implemented in synchronous reference frame as:

$$G_{PI}{}^{\pm}(s)=G_{PI}(s\mp jw)=K_P+K_I\frac{1}{s\mp jw_o} \qquad \textbf{(6)}$$

Where, (s-jw) is Positive sequence and (s+jw) is negative sequence components in SRF [15]-[16].

The main focus of this paper is to reduce the settling time with zero steady state error and to improve the transient performance during amplitude, phase and frequency variations. In order to obtain high disturbance rejection capability, suitable value of natural frequency (w_n)is choosen for attenuation in all disturbance frequencies. Keeping all these points in view, A PR controller is designed. The complication in single-phase conversion is that chosen frequency component not only appears as DC but, also contributes to harmonic terms at a frequency of 2w. Therefore, the derived generalized integrator is obtained by adding eqn (5) & (6) results in a PR controller [23]. i.e.,

$$G_{PR}(s)=K_P+\frac{K_I*s}{s^2+w_o{}^2} \qquad \textbf{(7)}$$

Where, w_o is the angular frequency of the output signal and K_I=K_R is the Resonant gain. The above eqn.(7) represents an Ideal PR controller. It provides zero gain at other frequencies and infinite gain at fundamental frequency and no phase shift at any other frequencies. Hence, it leads to a large error and stability is affected when tracking the reference voltage. This error can be minimized if a a non-ideal PR controller is used as shown below.

$$G_{PR}(s)=K_P+\frac{K_R*w_C*s}{s^2+2w_cs+(6w_o)^2} \qquad \textbf{(8)}$$

Where, w_c is the Cut-off frequency of the controller and it is given by:

$$w_c = 2*w_o*\varsigma \qquad \textbf{(9)}$$

where, ς is damping factor and is reasonably choosen to get low bandwidth and high value of resonant gain to obtain high attenuation of harmonics. Therefore, wc is the compromise between error of tracking reference signal and reduction of sensitivity. In eqn (8), the value of K_p is tuned in the same way as a PI controller, It determines the dynamics of the system interms of gain, phase margin and bandwidth. K_r is tuned by shifting the magnitude response vertically, but has no much variation in bandwidth as shown in Fig. 6 with various values of W_c [19]. There are three parameters K_p, K_R and W_c and two parameters are kept constant for observing the changes in third parameter.

Assuming K_p=0, W_C=1, The K_R has no effect on bandwidth but the gain increases when K_R is added as shown in Fig 6(a).

Assuming K_p=0 and K_R=1, The changes in W_c has effects on both phase and magnitude of the controller as shown in Fig 6(b). The magnitude and phase changes when W_c changes. But, same gain can be achieved at resonant frequency of the PR controller with W_c.

Finally, when K_p is added, the magnitude of PR controller increase, but has a peak value at resonant frequency. But the phase and magnitude decreases when K_p is added. The value of K_p can be chosen to make sure that the system can achieve high performance in the sinusoidal reference tracking as well as disturbance rejection. Based on this theoretical Analysis, In this paper, the PR controller gains are chosen as: K_p=67.5, K_R=100 and Wc=7.

The PR controller generates the required sinusoidal reference signal along the open loop path and therefore ensuring the zero steady state error. The above eqn.8 makes the controller more realizable due to its finite precision and also provides a very small steady state error when compared to a PI controller.

Besides all these functionalities, selective harmonic compensation can be achieved by cascading multiple resonant controllers. The dynamics are not affected with the use of Multiple resonant controllers as these are used near to the resonant frequencies.

$$G_{PR}(s) = \sum_{h=3,5,7...} \frac{K_{Ih} * s}{s^2 + (hw_o)^2} \quad \textbf{(10)}$$

$$G_{PR}(s) = \sum_{h=3,5,7...} \frac{K_{Ih} * w_C * s}{s^2 + 2w_c s + (6hw_o)^2} \quad \textbf{(11)}$$

Where, h is the order of the harmonic to be compensated. However, the cut-off frequency should be choosen from 5-15 rad/s to avoid difficulty of implementing on a low cost 16-bit processor. The phase and magnitude for various values of cut-off frequencies are shown in **fig.6.**

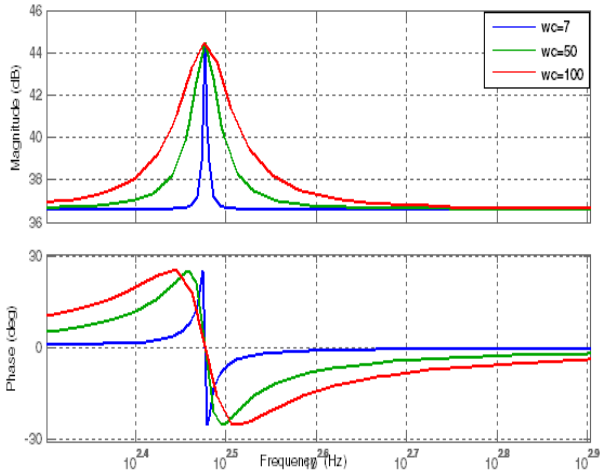


Fig. 6. Frequency Response for various values of W_c.

V. Simulation Results

The performance of PR controller as a loop filter for a SOGI-PLL has been tested using a dSPACE DS1104 setup. In this section, the proposed method is analyzed and evaluated through HIL simulation and an extensive MATLAB simulation. The nominal fundamental frequency is set to 50Hz with a simulation step size of **2ms.** For discretizing the continous system, trapezoidal based method is used to ensure discrete accuracy. The block diagram of the HIL test bed is shown in **Fig. 11.** The dSPACE internally generates the required input signals and sent to to the External D/A converter via the serial peripheral interface to generate the analog signal [6]. The resulted waveform is then acquired by the dSPACE to perform the SOGI-PLL action. The input and output waveforms are sent to D/A converter to be displayed by the 4-channel digital oscilloscope. The RMS values of the single-phase utility grid voltage is V_{rms} = 230V (1 p.u). A frequency step is applied from 50 Hz to 55 Hz is exerted at **0.4s** and back to 50 Hz at **0.8s.** The SOGI-PLL frequency detection is shown in **Fig. 7.**

If the input voltage contains any DC component then it leads to the fundamental frequency oscillation in SOGI output.

In order to obtain a trade-off between proper harmonic attenuation, dynamic conditions and stability, a crossover frequency of 314.15 rad/s is set and the controller values are attained **(Kp = 67.5, Kr = 100),** an acceptable response is attained with an overshoot of less than **5%.** The SOGI gain *K* = 1.6 is used. The performance of the proposed PLL has been tested under different grid disturbances like volatage sag, voltage harmonics, phase jump and frequency step variations variations and compared with SRF, Inverse Park, Enhanced and SOGI with PI as Loop Filter type PLL's.

These tests are performed and the results are shown based on MATLAB/Simulink Environment and HIL simulation which are proved enough to observe all the desired characterstics.

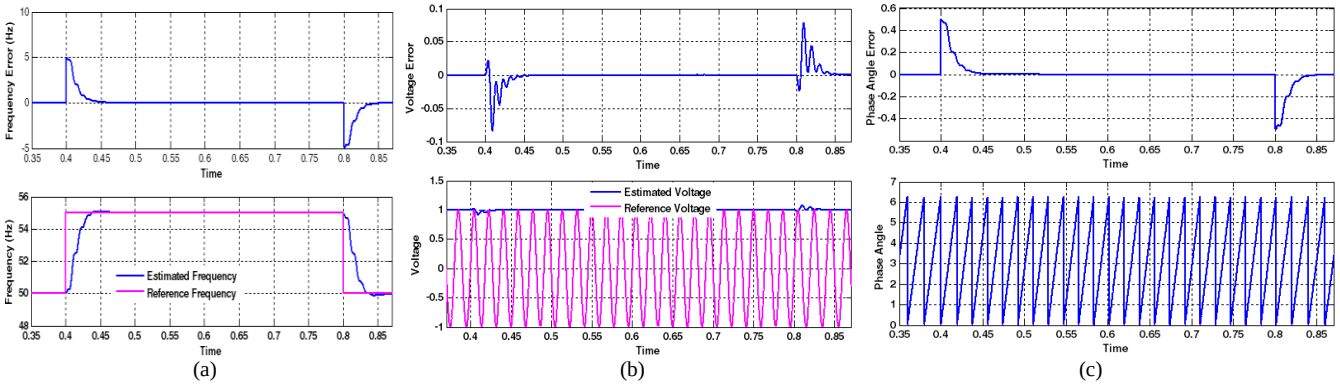
A. Frequency Response:

The input signal is initially sinusoidal with a magnitude of 1 p.u. and a freuqency of 50Hz. **Fig. 7 (a)** shows the frequency response of the SOGI-PLL under step change in frequency. The frequency is varied by **20%** of positive step to test the dynamics and behavior of the SOGI PLL. The PLL lcoks the frequency in less than 4**ms (< 2 cycles).** In the steady state, the error in frequency of the proposed PLL shows almost zero. A very tiny error in voltage magnitude appears even under utility grid

frequency variations as shown in **Fig. 7 (b).** It is clear that the PR control exhibits very less overshoot and the response is faster and accurate. From the results, some observations are made: 1) The frequency is estimated accurately. 2) The tracking capability of the transient is about **2 cycles.** 3) the peak value during frequency variations has a very small transient of about **0.05%** in the estimated magnitudes of the voltage. 4) The transient in the frequency reaches to a peak value of about **0.7%.** 5) The transient in the phase angle error on the phase reaches a maximum of about **0.4%.**

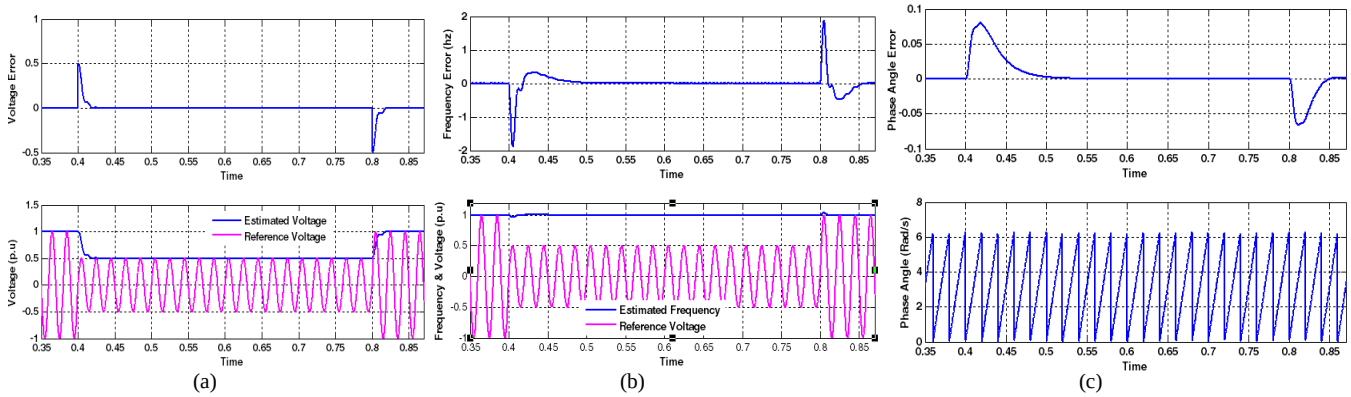
B. Voltage Sag:

The input signal is initially sinusoidal with a magnitude of 1 p.u. and a freuqency of 50Hz. The magnitude of the signal undergoes a voltage sag of **0.5 p.u.** at **t=0.4s. Fig. 8.** shows the simulation results of voltage sag at the grid voltage to evaluate the performance of the PLL with PR control. From the results, some observations are made: 1) The voltage sag is estimated accurately. 2) The tracking capability of the transient is less than **one cycle**. 3) the peak value during sag conditions has a very less transient of about **0.5%** in the estimated magnitudes of the voltage. 4) The transient in the frequency reaches to a peak value of about **0.04%.** 5) The transient in the phase angle error on the phase reaches a maximum of about **0.08 rad/s.**



(a) (b) (c)

Fig. 7. Results under frequency step from 50 Hz to 55 Hz. a) Estimated Frequency b) Estimated Voltage c) Estimated Phase Angle.



(a) (b) (c)

Fig. 8. Results of Voltage Sag from 1 p.u to 0.5 p.u. a) Estimated Voltage b) Estimated Frequency c) Estimated Phase Angle.

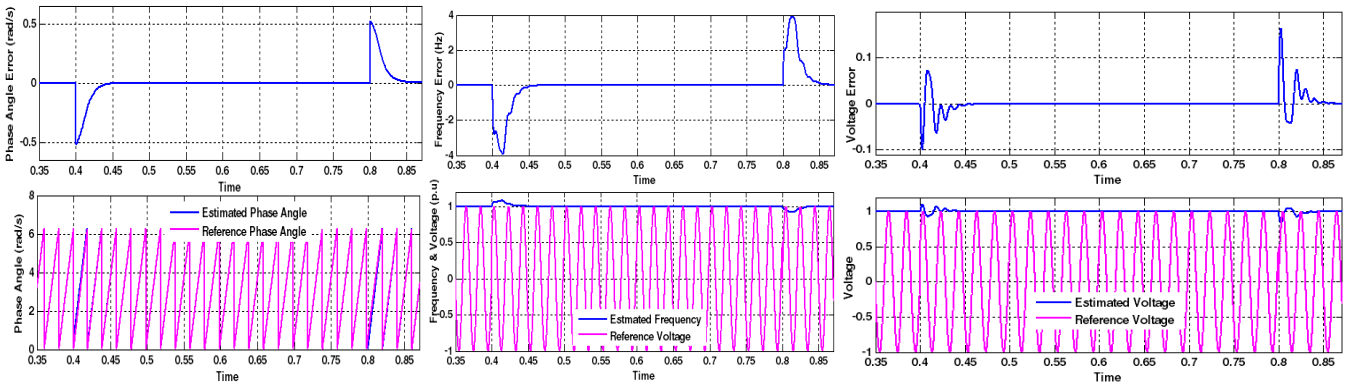


Fig. 9. Results of Phase Jump from 0^0 to 30^0. a) Estimated Phase Angle b) Estimated Frequency c) Estimated Voltage.

angle jump of 30^0 or 0.524 rad/s is applied to the SOGI PLL. The response under steady state and phase jump can be observed in **Fig.9.** The phase angle error reaches its steady state in about **1.5 cycles (30ms).** From the results, some observations are made: 1) The Phase of the signal is estimated and tracked accurately. 2) The tracking capability of the transient is about **one cycle**. 3) the peak value during sag conditions has a very tiny transient of about **0.05%** in the estimated magnitudes of the voltage. 4) The transient in the frequency reaches to a peak value of about **0.07%.** 5) The transient in the phase angle error on the phase reaches a maximum of about **0.5 rad/s [8].**

To validate the method, Three other conventional PLL's are tested and compared . The values of PI controller are considered same as that of PR controller. The mathematical comparison with PLL techniques are shown in Table-I.

Table-I

PLL	Peak Overshoot (%)	Settling Time	Steady Steady Error
SRF	**Oscillatory**	**Oscillatory**	**Oscillatory**
I-Park	**5 %**	**a. 0.48s b. 0.46s c. 0.44s**	**a. 0.1 b. 0.1 c. 0.1**
EPLL	**4%**	**a. 0.44s b. 0.48s c. 0.01s**	**a. 0.01 b. 0.1 c. 0.08**
SOGI-PI	**1%**	**a. 0.44s b. 0.44s c. 0.01s**	**a. 0.08 b. 0.08 c. 0.08**
SOGI-PR	**0.1%**	**a. 0.4s b. 0.4s c. 0.01**	**a. 0 b. 0 c. 0**

VI. HARDWARE –IN – THE – LOOP TEST-BED

Testing of real-time hardware can be simplified using Hardware – In – The – Loop Test – Bed as this method is proved as an efficient and recognized approach with reduced simulation times. HIL interacts with a virtual environment that combines a real time simulation with an electronic interface for digital and analog systems and Matlab/Simulink simulation. The system is modeled and emulated by virtual environment producing the signal interactions and also its dynamic behavior [24]-[25]. The behavior of the entire system can be predicted in the real-time simulation and an electronic interface is used for digital and analog signals that are necessary. The main advantage of using an HIL system is to reduce the cost of real-time testing process and time. The plant model proposed in the paper is developed using dSPACE. In this paper, dSPACE is used as peripheral I/O device and modeling of the proposed plant [26]-[28]. The CPU hosts the MATLAB/Simulink simulation and given as input to the dSPACE for further processing.

The aim of this work is to provide a real-time dSPACE based HIL simulation technique for the proposed SOGI-PLL model. In order to approve the results obtained using MATLAB/Simulink simulation, a series of real-time experiments are tested using a DS1104 dSPACE platform and with several I/O blocks. Considering some security issues and reliability, proper insulation is to be made between the dSPACE, I/O interface and power circuit. The model is designed in MATLAB and the corresponding code is downloaded into the dSPACE with the fixed step and all the I/O parameters are configured. The entire platform is built based on DS1104 dSPACE, Host PC, 4-channel digital oscilloscope for monitoring the results and D/A and A/D converter interface for HIL simulation. The configuration of the HIL setup is shown in **Fig. 10.**

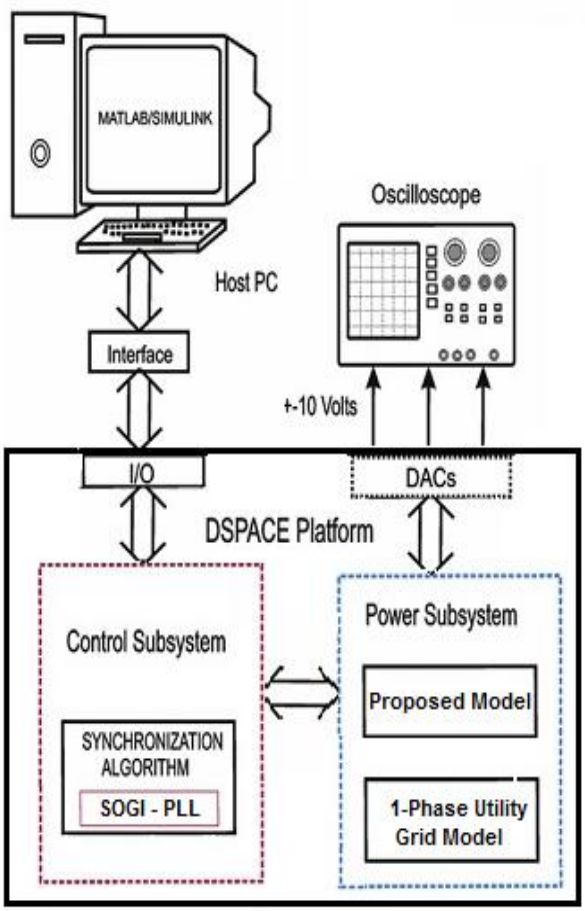


Fig. 10. Platform Setup of HIL for Real-Time Experiments.

Fig. 10 (a) shows the HIL results performed under steady state operation of the proposed model. A 4- Channel digital oscilloscope is used for better viewing of the results simultaneously. In Fig. 11 (a), input is shown in first channel as utility grid voltage and outputs are V_α & V_β (orthogonal signals) as 2^{nd} & 3^{rd} channels and the estimated phase angle as 4^{th} channel.

In Fig. 11 (b), input is shown in first channel as utility grid frequency and outputs are V_α & V_β (orthogonal signals) as 2^{nd} & 3^{rd} channels and the estimated frequency as 4^{th} channel.

In Fig. 11 (c), input is shown in first channel as reference utility grid voltage magnitude in p.u. and outputs are V_α (orthogonal signal) as 2^{nd} channel and the estimated phase angle as 3^{rd} channel.

In Fig. 11 (d), input is shown in first channel as Phase Jump and outputs are V_α & V_β (orthogonal signals) as 2^{nd} & 3^{rd} channels and the estimated phase angle as 4^{th} channel.

VII. CONCLUSION

This paper presents a Second Order Generalized Integrator Phase locked loop with Proportional Resonant controller as its loop filter. Generally, a PI control is used in the loop filter but a comparison and a better study of PR control is done in order to improve the transient responses against abrupt disturbances for single-phase grid connected systems. The algorithm used here is used to obtain the amplitude, Phase angle and frequency of the input voltage signal accurately and efficiently which improves the speed of the system response also smoothness of the responses during transients. The loop filter is having a major role in quadrature signal generation and accurate phase angle detection. Hence, extraction of the required information is done using PR controller and its performance under grid disturbances is also verified using simulation results and Hardware-In-The Loop Simulation.

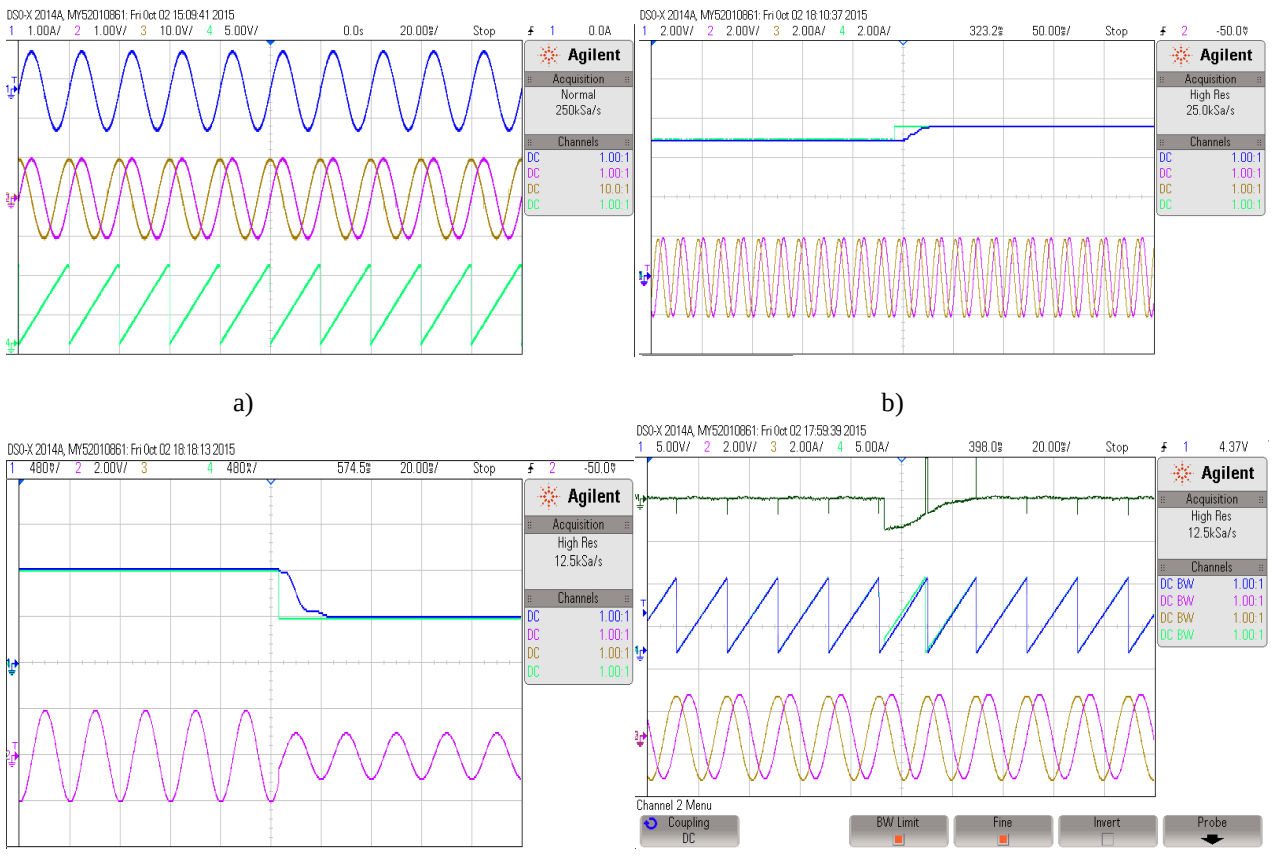


Fig. 11. Hardware – In – The – Loop Results **a) Steady State Conditions** **b) Frequency Step from 50Hz to 55 Hz** **c) Voltage Sag from 1.0 p.u. to 0.5 p.u.** **d) Phase Jump from 0^0 to 30^0.**

Finally, considering the disturbances presented, it was verified that the proposed PR control has a very fast, good response with higher steady state accuracy and high rejection against various disturbances. Thus, a Loop Filter with PR control is expected to be a good choice for single-phase applications.

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