A 3 - DIMENSIONAL SVPWM ALGORITHM, ITS FPGA - IMPLEMENTATION FOR MULTILEVEL INVERTERS

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Abstract: *This work reports a simplified approach to implement a three dimensional space vector pulse width modulation (3D-SVM) for multilevel inverter (MLI). The 3-D SVM is advanced method of 2-D SVM, and it inherits all the advantages of traditional 2-D. A simple technique for the selection of switching states to find the reference vector without redundant switching vectors is proposed here. This paper treasures the reference vector by categorizing sub cubes and tetrahedrons by using mathematical environments and calculates the on-state durations of the respective switching state vectors without involving trigonometric functions or look up tables and angle determination. The detailed analysis, verification has been done by computer simulation using MATLAB –Simulink platform. The proposed algorithm is more suitable for hardware implementation by significantly reducing the hardware core components and cost. Based on the simplified 3D-SVM, the reduced memory intellectual property (IP) core has been developed using Verilog hardware description language (VHDL).The designed 3D-SVM IP core is validation through FPGA-SPARTAN III- XC3SD1800A board and tested with prototype 3-phase 3-level Neutral Point Clamped -MLI. Here the cost of the proposed technique is independent of voltage levels of inverter; this algorithm can minimize extremely the time and complexity of calculation, since the proposed 3D-SVM IP core is simpler and faster.*

Keywords: *Neutral point clamped multilevel inverter (NPC-MLI), Pulse width modulation (PWM), 3D-Space-vector modulation (3D-SVM), Verilog hardware description language (VHDL), and intellectual property (IP) core.*

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I. Introduction

Multilevel inverters [1] have gained much attention in medium voltage and high power applications due to their better performance compared to two-level inverters. Multilevel inverters include an array of power semiconductors, capacitors and voltage sources the output of which generates voltages with stepped waveforms.Attractive features of Multilevel Inverters: Stair case output - Nearly sinusoidal output voltage, Output voltages with lower harmonic distortion, Lower dv/dt in the output voltage, Lower common mode voltage, operates at lower switching frequency, Lower electromagnetic interference problems [2]-[3].

SVM is an algorithm which directly uses the control variable given by the control system and identifies each switching vector as a point in complex space which is used to control the switches of multilevel inverter.SVM utilises the maximum DC Link voltage and can operate in entire modulation region with minimum totalharmonic distortion [4]. Under pulse width modulation techniques SVM and SPWM offers good results, of these, SPWM is not used to analyze each switching state present in a multilevel inverter. SVM techniques are used in both 2D and 3D implementation.

In 2 dimensional space vector modulation, 3 phase n-level inverter consists of six sectors and n^3 switching states (for 3 level 3^3=27 switching states) [4]-[6]. In SVM each sector should contains (n-1)^2 triangles (4 triangles in each sector). It contains 3 zero vectors, 12 small vectors, 6 medium and 6 large vectors. The complexity is due to the difficulty in determining the location of the reference vector, the calculation of on-times, and the determination and selection of switching states.

In [7], implementation of 3 dimensional space vector modulation (3D-SVM) using diode clamped multilevel inverter by directly tetrahedron identification in cube and using difficult matrix mathematical calculation to find switching time calculations. This provides modulation algorithm in all applications which provide a 3D vector control. In [8] 3D space vector algorithm of multilevel inverters for compensating harmonics and homo polar component in the system is presented. This generalized method which provides an on- line computation of nearest switching vectors sequence to the reference vector and calculates duty cycle calculations with using trigonometric functions and some look up table values.

In [9] an approach to implement the 3D SVM, which provides a general view of the modulation characteristics. The algorithm is independent of the number of levels and eliminates the need for tetrahedron identification and lookup tables to calculate duty cycles. The algorithm for finding the state vectors is based on the idea of switching the state vectors nearest to the reference voltage vectors. The switching state vectors and its ON time calculations are determined from the lookup tables.

In [10] feed forward 3D-SVM takes to improve computational cost, number of commutations and voltage distortion. The actual dc capacitor voltage unbalance of the multilevel inverter is reduced. [11] The algorithm can

be used for any number of phases. This gives multilevel multiphase space vector PWM algorithm applied to three phase inverters. And this multiphase algorithm is compared with previous SVPWM algorithms.

In this paper an algorithm to implement the 3 dimensional space vector pulse width modulation for multilevel inverter was proposed. 3D SVM have no redundant switching states, so each vertex will have only one switching state. This should be implemented by sub cube identification and tetrahedron identification. Then duty cycle calculation has done without trigonometric values and other look up tables.

Section II discusses in detail, the modulation strategies for multilevel inverters – 2D SVM. Reference vector synthesis, sub cube identification, tetrahedron identification and switching time calculation are discussed in Section III. Section IV explains the implementation of 3D-SVM algorithm. Simulation and experimental results are discussed in Section V and VI respectively.

I. Modulation strategies for MLI

I.1. 2D Space Vector Modulation (2D-SVM)

It directly uses the control variable given by the control system and identifies each switching vector as a point in complex (α, β) space. By using diode clamped multilevel inverter shown in fig.1which is suitable for digital signal processor (DSP) implementation and it can optimize various switching sequences .The space vector diagram of any three-phase *n*-level inverter consists of six sectors. Each sectors consists of $(n-1)^2$triangles. The tip of the reference vector can be located within any triangle. Each vertex of any triangle represents a switching vector.

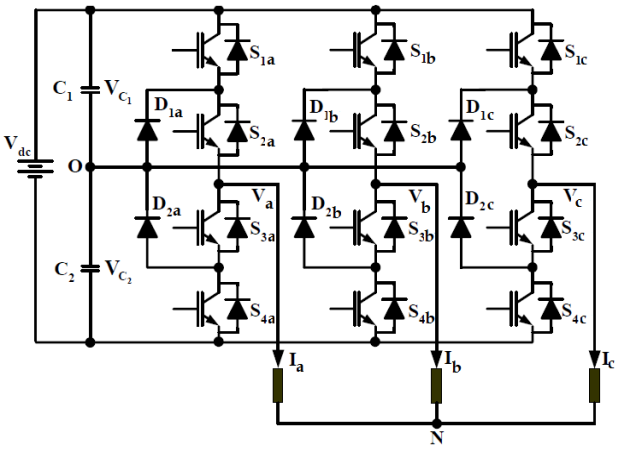


Fig.1. Diode clamped multilevel inverter

A switching vector represents one or more switching states depending on its location. There are n^3switching states in the space vector diagram of an *n*-level inverter. The SVPWM is performed by suitably selecting and executing the switching states of the triangle for the respective switching times [4], [12].

The 2D SVM hexagon diagram is shown in Fig.(2). Here for a 3 level inverter, six sectors are present and each sector is having four triangles. In 2D SVM redundant switching states are present. To find switching times, nearest three vectors and selected three vectors methods are used. The nearest vector redundancy scheme is the proposed technique used to obtain the capacitor balancing problem. The rotating reference vector V* lies in the any of the sub triangles in any of the sector. At that point the switching state selection can be done. Depend upon the point, the participation of the short vector, medium and large vector can be utilized. By the proper utilization of the short vectors the balance can be achieved. In [13] & [14] the short vectors are having two switching states, one state produces the positive phase current and another switching state produces the negative current, then by the redundant states the positive and negative phase currents are cancelled. These three vectors could be used to synthesize the sampled reference voltage vector.

$$V^{*}\delta_{S1} + V^{*}\delta_{S2} + V^{*}\delta_{M1} = V^{*} \quad (1)$$

$$\delta_{S1} + \delta_{S2} + \delta_{M1} = 1 \quad (2)$$

and duty cycles calculations shown in [4].

The sequence, in [15] - [18] which the on-times t_a, t_b, and t_o have to be used, will be dependent on the order of selecting the switching states. Thus, the proposed algorithm is able to make use of any redundancies for any vertex of the triangle. As opposed to this, if the two-level hexagon is used to mimic the two-level modulation, only two redundancies of zero vectors are considered. Hence, for higher level where middle vectors have higher redundancies, such approach will not be able to make use of all redundancies.

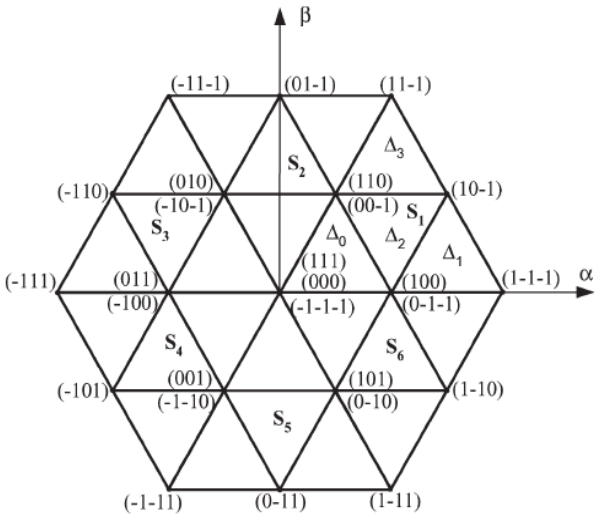


Fig.2.Diagram of 2D-SVM

In 2D-SVM once the triangle identification was done then that particular triangle is treated as sector of a virtual 2-level inverter and the suitable vertex of the triangle can be taken as the zero vector**.**The tip of the reference vector with respect to$\alpha\beta$axis isrepresented as (V_α, V_β).

The duty ratios are,

$$\delta_a = V_\alpha - V_\beta/\sqrt{3} \quad (3)$$

$$\delta_b = V_\beta/m \quad (4)$$

$$\delta_0 = 1 - \delta_a - \delta_b \quad (5)$$

Table I gives the switching states of devices (S_{i1}–S_{i4}) and switching states of the corresponding pole (S_{wi}) of the inverter. The pole output voltage can be expressed as,

$$V_i = S_{wi} * (V_{dc}/2) \quad (6)$$

TABLE 1
SWITCHING STATES, SWITCHING FUNCTION, AND MAGNITUDE OF OUTPUT VOLTAGES

V_i	Switching States				S_{WI}
	S_{i1}	S_{i2}	S_{i3}	S_{i4}	
$V_{dc}/2$	1	1	0	0	1
0	0	1	1	0	0
$V_{dc}/2$	0	0	1	1	-1

SVM increases dc bus utilization by 15% as compared to the SPWM technique. However, due to the lack of six switching states (vertices of hexagon), dc bus utilization would be on par to that of an inverter using the SPWM technique. In the proposed scheme, the computations do not change with the level. The PU remains the same for any level. On-time calculation equations do not change with triangle. The scheme is based on a two-level SVPWM. Therefore, an existing two-level SVPWM module can be easily adapted to the multilevel inverters.In addition to the calculation of on-times, the selection of switching states proposed in this method is restricted to some specific switching sequence(s). As the performance of the multilevel inverter is significantly dependent on the selection of the switching states, the optimization of switching sequence might be required.

II. Proposed 3D Space Vector Modulation (3D-SVM)

In 3D space vector modulation there is no redundant switching state, each vertex will have only one switching state as shown in Fig.(4). So the analysis of switching states, the mathematical calculations are simple and there is no need of transformations and angle determinations [19] & [20]. Implementation of 3D space vector modulation process is shown in Fig.(3).

Three dimensional space vector modulation for three level diode clamped multilevel inverter shown in Fig.(4). The reference vector can be calculated by identifying reference vector which is placed in the sub cube and in the tetrahedron. This should be identified by using the normalized reference vector. The reference vector will be pointing to a volume which is a tetrahedron. The vertexes of that tetrahedron are the state vectors of the switching sequence. In addition, the algorithm permits to obtain the corresponding duty cycles without using pre calculated tables or trigonometric functions. In this analysis, 3D cube is having 8 sub cubes and each sub cube having 6 tetrahedrons [9] & [21]. Here in the proposed 3D-SVM,the reference voltage vector is decomposed in to two components as,

$$V_{ref} = V_0 + V_t \quad (7)$$

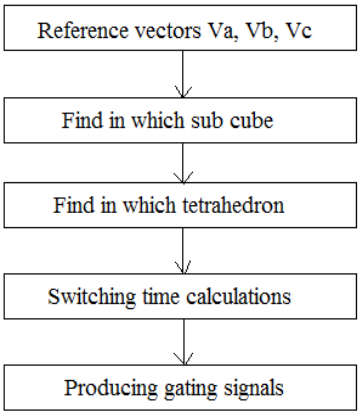


Fig.3. Process of 3D SVM

III.1. Reference vector synthesis

V_o – Off set voltage, V_t - two level voltage

In a-b-c coordinates, it is expressed as

$$\begin{bmatrix} V_{refa} \\ V_{refb} \\ V_{refc} \end{bmatrix} = \begin{bmatrix} V_{0a} \\ V_{0b} \\ V_{0c} \end{bmatrix} + \begin{bmatrix} V_{tla} \\ V_{tlb} \\ V_{tlc} \end{bmatrix} \quad (8)$$

The offset component of the reference voltage vector is defined as

$$v_0 = \begin{bmatrix} v_{0a} \\ v_{0b} \\ v_{0c} \end{bmatrix} + \begin{bmatrix} int(v_{refa}) \\ int(v_{refb}) \\ int(v_{refc}) \end{bmatrix} \quad (9)$$

The reference vector voltage is summation of the offset voltage and the two level inverter voltage is shown in eq (5)

The two level components V_t is defined as

$$v_t = v_{ref} - v_0 = \begin{bmatrix} v_{tla} \\ v_{tlb} \\ v_{tlc} \end{bmatrix} \quad (10)$$

In 2D SVM the reference vector identification is difficult because it has redundant switching states. It has 27 switching states placed in 19 vertices. So it has complexity in analyzing switching states [22]. But in 3D SVM there are no redundant switching states. It has 27 switching states placed in 27 vertices. So mathematical analysis is simple and easy for each and every switching states. Reference vector identification becomes very simple compare to 2D-space vector modulation and total

harmonic distortion, voltage stress on the devices should be reduced [23] & [27]-[30].

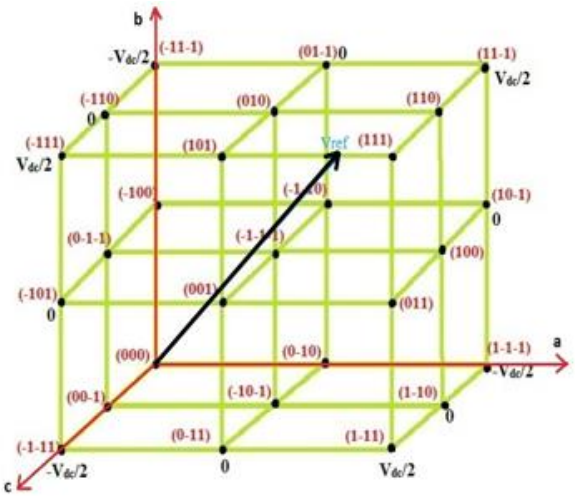


Fig.4. 3D –SVM cube diagram

III.2. Sub-cube identification

For 3 phase n-level inverter has $(n-1)^3$ sub cubes. Here for 3 phase three level neutral point diode clamped inverter has 8 sub cubes presented. From that (a, b, c) are the origin coordinates corresponding to the reference system of the sub-cube where the reference vector is pointing too. This should be explained in the flow chart shown in fig.5.

The space vectors of a multilevel inverter form a cube in a 3Dspace. This space can he decomposed into several tetrahedrons which generate the cube total volume. For a certain reference vector in three-phase coordinates (X_a,X_b,X_c**),** the integer part of each component (a, b, c) is calculated [24], and this is shown in Fig.4. Where,

$$a = \text{integer}(U_a)$$
$$b = \text{integer}(U_b) \qquad (11)$$
$$c = \text{integer}(U_c)$$

The 3D space is formed by a certain number of sub cubes depending on the number of the levels of the inverter.

III.3. Tetrahedron identification

In 3D space vector modulation tetrahedron should be placed in each sub cubes. There are six tetrahedrons ineach sub-cube. So, it is needed to define the tetrahedronwhere the reference vector is pointing too. This tetrahedron is easily found using normalized reference

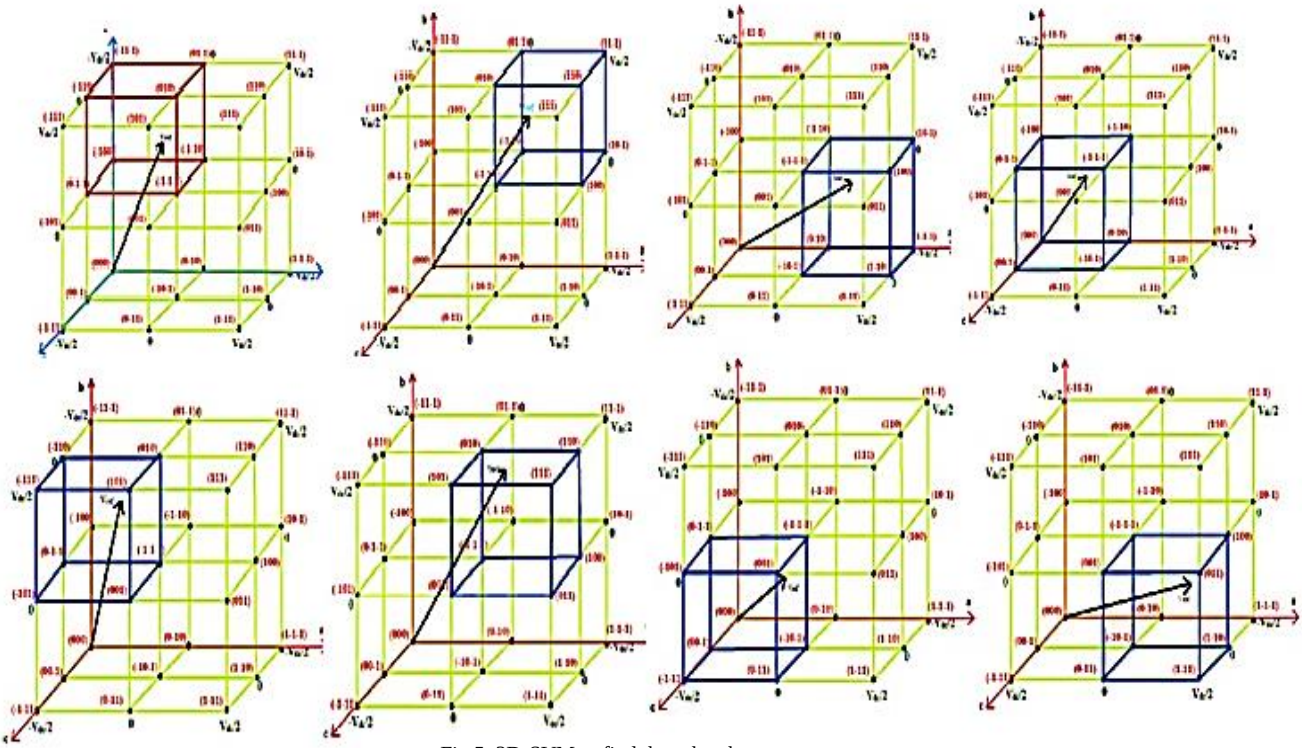


Fig.5. 3D-SVM to find the sub cubes

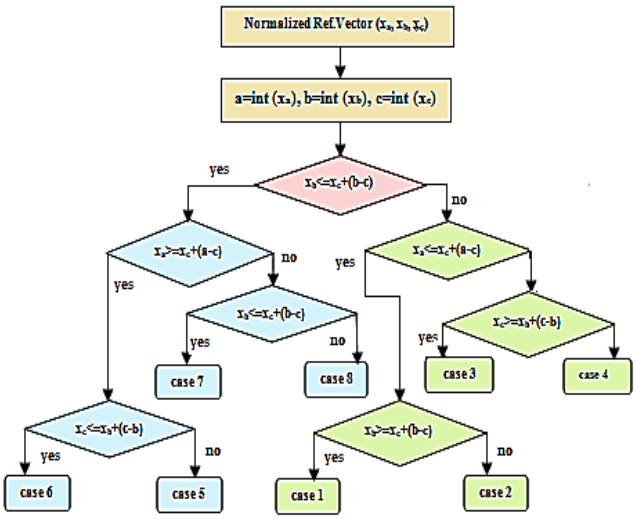


Fig.6. Flow chart to identify the reference vector in which sub cubes

vectors (X_a, X_b, X_c) it is similar to that of sub cube identification. And phase difference of these three planes is 30 degree space, which define the six tetrahedrons inside the sub cube. This is shown in the fig.5. From that normalized reference vectors X_a, X_b, X_c, to find the values of (a, b, c) coordinates.

After finding the coordinates (a, b, c) are the original coordinates corresponding to the reference system. The reference vector is normalized by $V_{dc}/2$, which is expressed as

$$v^*=V^*/(\frac{V_{dc}}{2}) \quad (12)$$

The state vectors are the vertexes of the corresponding tetrahedron which generates the reference vector U_a, U_b, U_c values are,

$$\begin{aligned} U_a &= S_a^1 d_1 + s_a^2 d_2 + S_a^3 d_3 + S_a^4 d_4 \\ U_b &= S_b^1 d_1 + s_b^2 d_2 + S_b^3 d_3 + S_b^4 d_4 \\ U_c &= S_c^1 d_1 + s_c^2 d_2 + S_c^3 d_3 + S_c^4 d_4 \end{aligned} \quad (13)$$

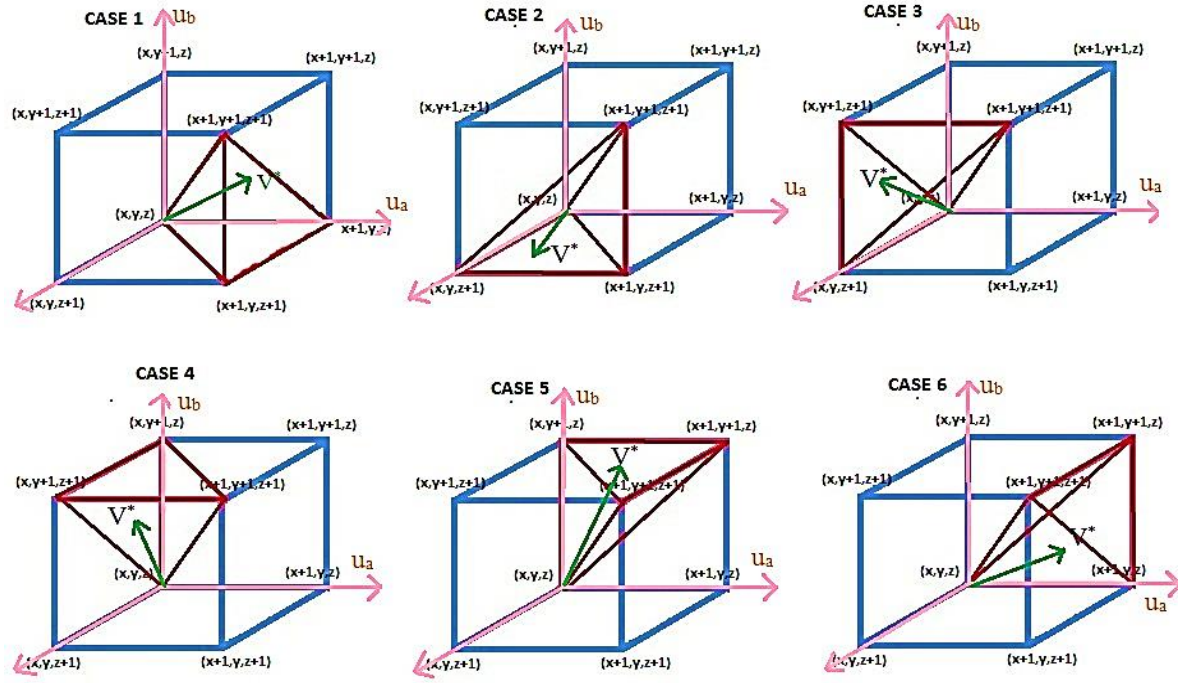


Fig.7. Diagrams to find tetrahedrons in each sub cube

III.4. Switching times calculation

The corresponding duty cycles are calculated once the state vectors which generate each reference vector are known [25].After assuming the normalized reference vector (a,b,c) coordinates, the main step of the algorithm consists in calculating the four space vectors respect to that of four vertices of a tetrahedron into a sub cube. From this normalized reference vector we can get the integer values (U_a,U_b,U_c). Using a = integer (U_a), b = integer (U_b), c = integer (U_c). The duty cycle equation is, $d_1+d_2+d_3+d_4=1$. Once (a, b, c) coordinates are known, the main step consists of calculating the four space vectors u_1, u_2, u_3 and u_4, corresponding to the four vertices of a tetrahedron in the selected sub cube. These vectors will generate the required reference vector.

The next step is to calculate the remaining two vectors u_2 and u_3. These vectors are calculated for optimized switching sequence, such that switchingoccurs only in one phase when the inverter changes its state. This is done to minimize the switching losses. To realize this, the calculation is based on the concept that the vector nearest to any sub cube vertex is switchedfirst and the next nearest vector is switched next. These two sub

cube vertices form the remaining two required vectors. For this, the two level vectors V_{tla}, V_{tlb}, V_{tlc} are first normalized such that the minimum value is 0 and the maximum value is 1. The lower rounded integer values of these normalized two level vectors gives the second state vector u_2, and the upper rounded integer values gives the third state vector u_3.

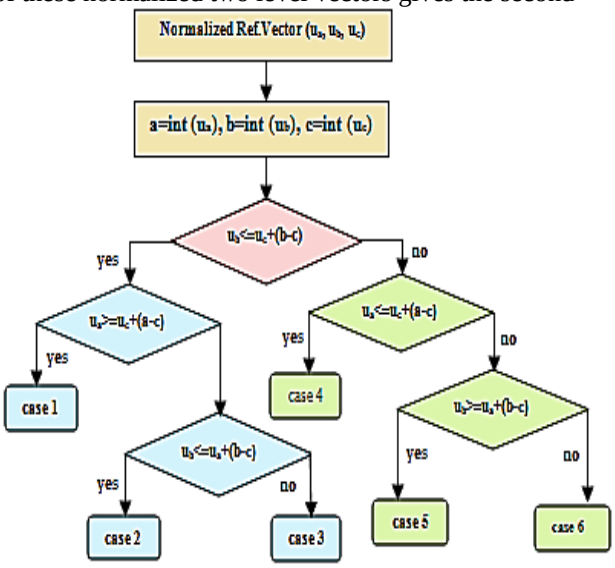


Fig.8. Flow chart to identify reference vector in which tetrahedrons

In tetrahedron 1 the duty cycle calculations can be,

$$v_{tla} = \max(v_{tl})$$
$$v_{tlb} = \min(v_{tl})$$
$$v_{tlc} = \min(v_{tl})$$

Similar analysis of other tetrahedrons leads to the generalization,

$$d_1 = 1 - \max(v_{tl}) \quad (14)$$
$$d_2 = \max(v_{tl}) - med(v_{tl}) \quad (15)$$
$$d_3 = med(v_{tl}) - \min(v_{tl}) \quad (16)$$
$$d_4 = \min(v_{tl}) \quad (17)$$

It can be observed that the duty cycles are only functions of the reference vector two level components V_{tl}. The table (2) shows switching calculations of tetrahedrons present in the sub cube 1.

TABLE2
SWITCHING TIMES OF VARIOUS CASE TETRAHEDRONS

CASES	SPACE VECTOR SEQUENCE	SWITCHING TIMES
case 1	$(s_a^1, s_b^1, s_c^1) = (E_a, E_b, E_c)$ $(s_a^2, s_b^2, s_c^2) = (E_a+1, E_b, E_c)$ $(s_a^3, s_b^3, s_c^3) = (E_a+1, E_b, E_c+1)$ $(s_a^3, s_b^3, s_c^3) = (E_a+1, E_b+1, Ec+1)$	$d_1 = 1 + a - u_a$ $d_2 = -a + c + u_a - u_c$ $d_3 = b - c - u_b + u_c$ $d_4 = -b + u_b$

Similarly the switching times for other tetrahedrons with respect to their sub cubes are calculated. The duty cycles are only functions of the reference vector components and the integer part of reference vector coordinates. In addition, the optimized switching sequence isselected in order to minimize the switching number. The space vector sequences in half cycle are (s_a^1, s_b^1, s_c^1),(s_a^2, s_b^2, s_c^2), (s_a^3, s_b^3, s_c^3),(s_a^4, s_b^4, s_c^4). In the second half cycle the space vector sequenceisin the reverse manner.

VI. Implementation of 3D-SVM algorithm

Implementation of 3D Space Vector Modulation for multilevel inverters based on the flowchart Fig.10. Which is having sub cube identification and tetrahedron identification by choosing some normalized reference vectors and duty cycles can be calculated easily. Fig.10 shows the control algorithm of 3D-SVM, in that the reference vector is divided into offset voltage and two level output voltage value. And by using these voltages determine the output switching sequences and switching time calculated by using two level output voltage, which is common for all sub-cubes present in the 3D-cube.

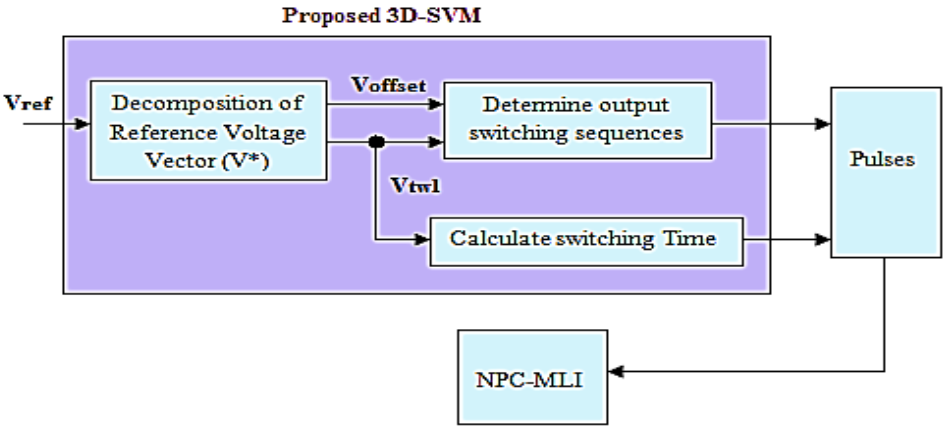


Fig.9.NPC –MLI ,3D-SVMControl algorithm flow

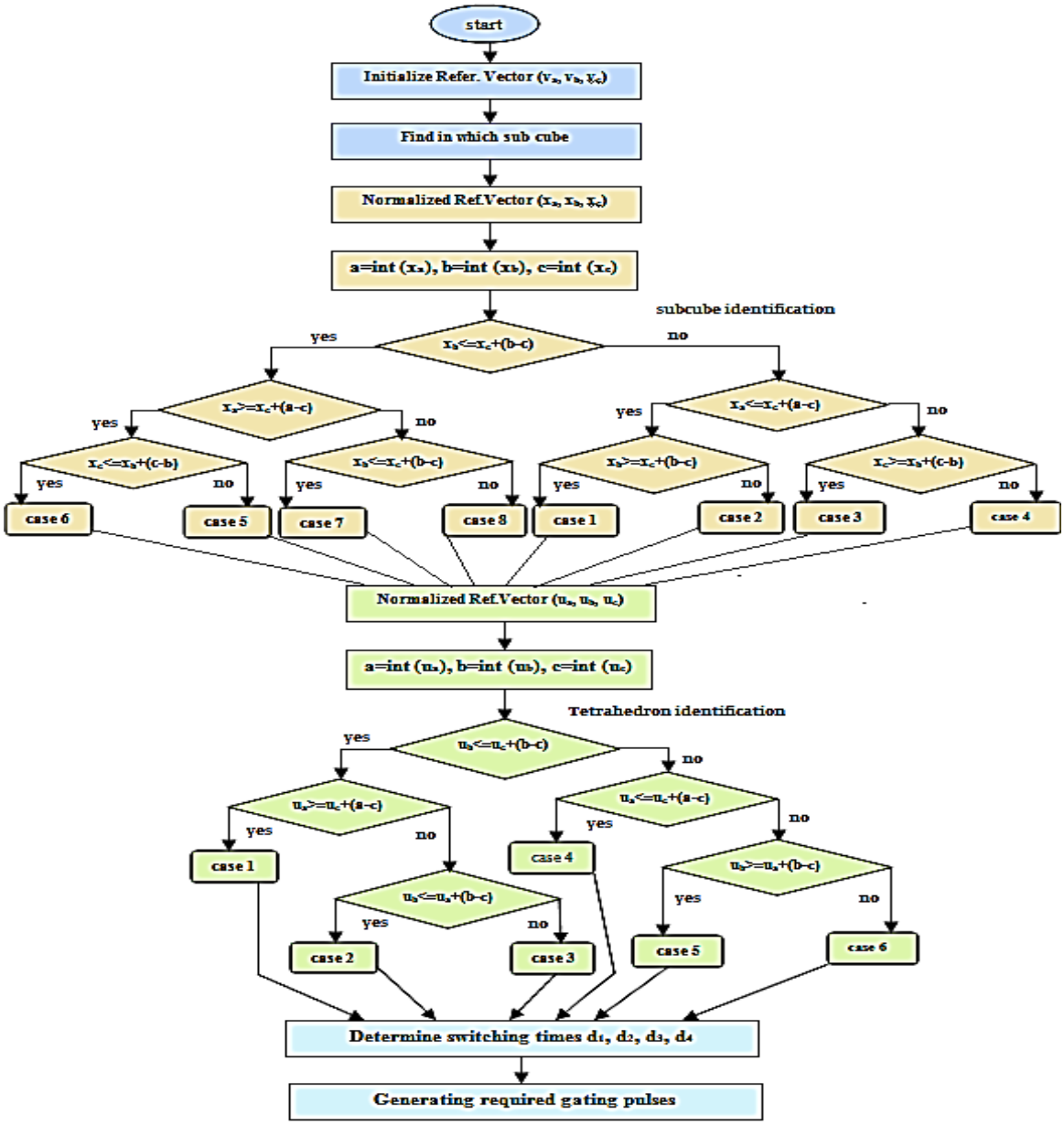


Fig.10. Flow chart for implementation of 3D S

VI. Hardware Implementation

3-phase 3-level NPC-MLI experimental setup for proposed 3D-SVM scheme. The NPC-MLI is designed by 2 front end capacitors and 12 IGBTs and 6 Diodes. The proposed 3D-SVM scheme is tested on 3-phase 3-level NPC-MLI with 1 HP squirrel cage induction motor with open loop *v/f* control for different modulation indexes..Table 4 shows, the hardware parameters of experimental setup. The rectifier side is responsible to control dc-link (V_{C1} and V_{C2}) voltage, and all the experimental results have been taken from the inverter side.

The proposed 3D-SVM scheme is developed by using VHDL code synthesized using Xilinx platform and the same effectively implemented in FPGA SPARTAN III-IP CORE. Pulse generator getting the inputs from the switching timer and frequency analyzer. Finally, NPC-MLI switches receiving pulses from the pulse generator. The corroborating experimental results are captured using 6 channels YOKOGAWA digital signal oscilloscope (DSO) and the switching pulses are captured using 2 channels Agilent technologies DSO results.The fig.20 and fig.21 shows theSPARTAN –III - 3AN – XC3S400 FPGA- Intellectual property (IP) core & 12 pulse output of 3D-SVM.All components were shared in a top file according to Fig. 18. At last, the whole system was simulated and synthesized in the XC3SD1800A-FPGA through the use of theXilinx Foundation ISE tools, which are specific for these tasks.Table 6 shows assets used to implement 3D-SVM algorithm. In thisimplementation, both 2D and 3D-SVM algorithm use only one BRAM-dedicated memory to generate the sine and cosine functions, but the 2-D algorithm uses half flip flops and two hardware multipliers less than the 3-D algorithm. This is because the first algorithm works with only three 2-D vectors, instead of the four 3-D vectors of the second algorithm..Although the 2-D algorithm works with a few and small vectors both implementations use a related number of slices (logic blocks) and LUTsThis is due to the need for an extra task to select the generating vectors in the 2-D algorithm. As a result, the 3-D algorithm is easier to implement but uses more logical resources of the FPGA.

The computational times of 2D-SVM are 8.8 micro seconds and for 3D-SVM are 9.2 micro seconds, which is 2 times of the conventional 2D-SVM algorithm.

VII. Hardware Results

The simplified 3D-SVM, experimental results has shown in table7 with different modulation indexes. In fig.22cshows, at lower modulation index (m_i=0.5)the line voltage V_L= 156V with 3.8% voltage THD ofthe proposed 3D-SVM .whereas, in conventional 3D-SVM produces only 151V with THD of 3.97%.

TABLE 6
THE SOURCE USED IN THE DESIGN

Resources	Used/Available	Utilization (%)
Slice Flip Flops	2670/33,280	8%
4 inputs LUTs	9324/33280	28%
Number of occupied slices related logic	5949/16640	35%
Number of occupied slices unrelated logic	0/1983	0%
Total source used	17279/88590	19%

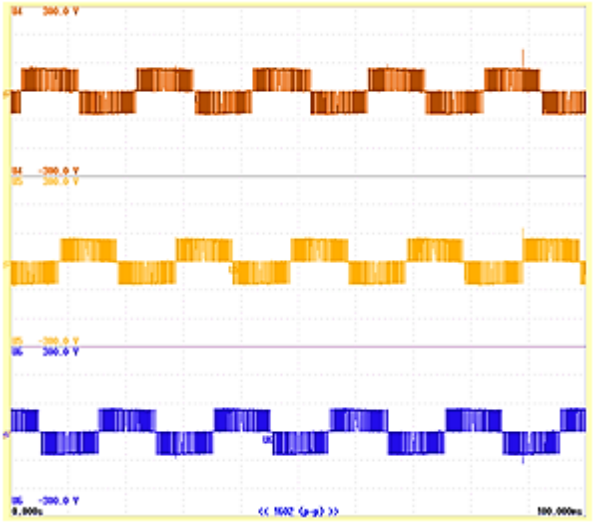
In fig22.d&e.shows, the line voltage, line current & THD spectrum at higher modulation index (0.907). The lower order harmonics in voltage spectrum is minimized up to 3.97% with line voltage of 189.5V, which is more than 2.6% over the 2D SVM.The salient features of the proposed scheme are as follows,

- Proposed technique finds the reference vector without redundant switching vectors.
- Reference vector identification in sub cube and tetrahedron done without any angle determinations and look up tables.
- The volt-sec balance equation is maintained throughout the proposed scheme.
- Algorithm can minimize extremely the time and complexity of calculation.

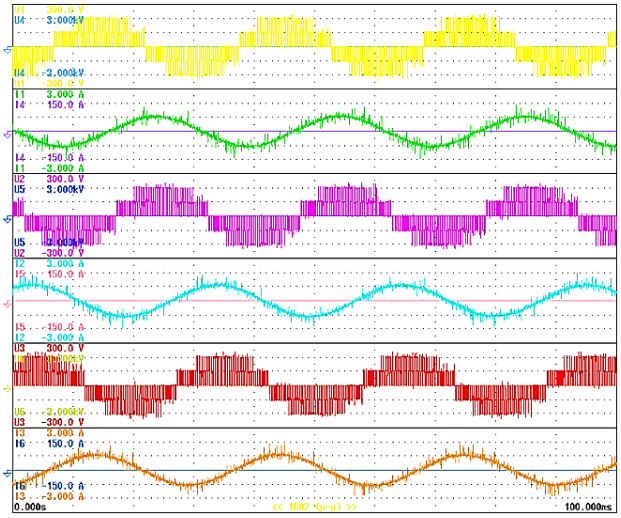
THD value for output voltage of proposed system is 3.8% which is less than that of *IEEE standard 519-1922*(a)

TABLE 5
HARDWARE RESULTS

Modulation index (m)	Hardware results			
	2D		3D	
	V_{out}	THD	V_{out}	THD
0.7	149.27	4.21%	150.93	3.82%
0.8	170.60	4.24%	172.49	3.73%
0.907	193.42	4.31%	195.57	3.95%

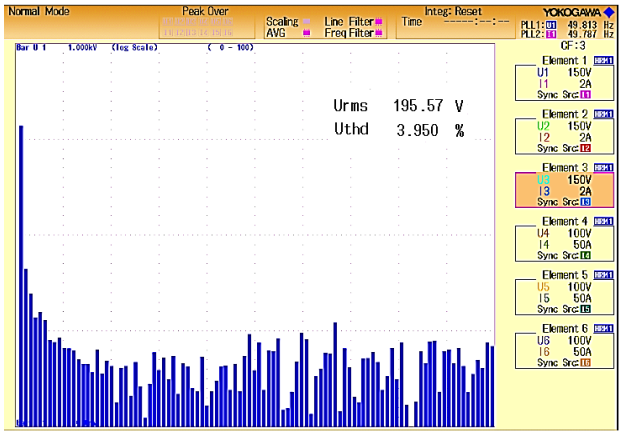


(a)



(c)

Fig.22. Experimental results a)output voltage when m=0.5 b)output voltage and current when m=0.8



(a)

		Order	U1 [V]	hdf[%]	Order	I1 [A]	hdf[%]
		Total	189.72		Total	1.5543	
fPLL1:U1	49.814 Hz	dc	---------	-------	dc	---------	-------
fPLL2:I1	49.815 Hz	1	189.57	99.922	1	1.5541	99.989
		2	0.26	0.135	2	0.0007	0.045
Urms1	195.57 V	3	0.20	0.103	3	0.0071	0.459
Irms1	1.5566 A	4	0.08	0.040	4	0.0005	0.035
P1	-116.92 W	5	0.54	0.286	5	0.0164	1.053
S1	319.67 VA	6	0.23	0.123	6	0.0002	0.010
Q1	297.52 var	7	0.18	0.092	7	0.0027	0.173
λ1	-0.3657	8	0.12	0.063	8	0.0002	0.014
Φ1	G111.45 °	9	0.50	0.266	9	0.0007	0.045
		10	0.22	0.119	10	0.0005	0.033
Uthd1	3.950 %	11	0.19	0.100	11	0.0009	0.055
Ithd1	1.489 %	12	0.15	0.082	12	0.0019	0.124
Pthd1	0.005 %	13	0.20	0.104	13	0.0010	0.065
Uthf1	4.038 %	14	0.22	0.117	14	0.0124	0.795
Ithf1	0.779 %	15	0.07	0.036	15	0.0003	0.021
Utif1	---O F---	16	0.18	0.094	16	0.0034	0.218
Itif1	---O F---	17	0.35	0.184	17	0.0008	0.053
hvf1	0.479 %	18	0.16	0.082	18	0.0011	0.068
hcf1	0.592 %	19	0.28	0.149	19	0.0006	0.039
Kfact1	1.2025	20	0.03	0.018	20	0.0018	0.117

(b)

Fig.23. THD analysis of the proposed system.a)waveform for THD analysis b)Tabulation of THD results

VII. Conclusion

The 3Dspace vector modulation algorithm presented in this work is very useful to readily calculate the switching sequence and the on-state durations of the respective switching state vector corresponding to the space vector modulation used in multilevel inverters. Mathematical analyses is simple because no need of transformations and angle determinations. In this 3D SVM algorithm there is no redundancy switching states. The designed 3D-SVM IP core is validation through FPGA-SPARTAN III- XC3SD1800A board and tested with prototype 3-phase 3-level Neutral Point Clamped -MLI.

The salient features of the proposed system are,

- ✓ The source code of the IP core can be easily implemented even a small scale FPGA processor.
- ✓ Switching time calculation is simple contrast to 2D-SVM.
- ✓ Output voltage is 195.57 V and with THD of 2.29%.

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