ANALYSIS OF FIVE SWITCH SEVEN-LEVEL INVERTER WITH MODIFIED SEPIC CONVERTER FOR FUEL CELL ENERGY CONVERSION SYSTEM

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Abstract — *This paper depicts a single-phase five-switch seven-level inverter topology with reduced number of switching devices for Fuel Cell Energy Conversion System (FCECS). The main objective of this topology is that the number of gate driving circuits and semiconductor devices are reduced, and further condenses the size and power consumption making the inverter circuit less complex. An improved characteristic of robustness and efficiency is achieved using Multi-Level Inverter (MLI) topologies with reduced switch count and passive components. This inverter is coupled with Modified Single Ended Primary Inductance Converter (SEPIC) structure which is more suitable for extraction of DC power from fuel cell with high voltage gain. This converter structure is also applicable to solar photovoltaic energy system. The single-phase seven-level FCECS is simulated using MATLAB Simulink and experimental result shows the features of the proposed inverter structure with high efficiency and low harmonic distortion.*

Index Terms— *Modified SEPIC,* Multilevel Inverter, Reduced Semiconductor Devices, Fuel Cell, Total Harmonic Distortion.

I. Introduction

In recent years, the dependent on conventional energy sources is drastically increased mostly because of world population and tremendous change in their lifestyle at large. Moreover, to reduce this dependence, the current scenario is utilization of the non-conventional energy sources. The prime reason for Power electronic research is to integrate power electronic converters with fuel cells which are an easy conversion mechanism with high efficiency and zero emission. In addition, it is constantly available throughout the year without any scarcity and there is no sudden change in its output power unlike as the wind, solar and other major renewable energy sources. In general, low power distributed generation systems using fuel cell energy may be widely used in residential applications in the near future [1].

Proton Exchange Membrane Fuel Cell (PEMFC) provides more flexibility than other types of fuel cells for the residential application. It has a relatively quick start time at normal room climate because of its low temperature operating capability [2]. Proper converter design is necessary to extract more power from PEMFC.

Many types of DC-DC converter topologies are available to an extent, to convert one level of DC voltage to another level of DC voltage which may be less than equal to or greater than that the given input value [3]-[5]. Among those types of converter, topologies SEPIC converter has some unique features namely buck-boost capability, nature of providing a non-inverted output, low switching losses and so on [6]-[8]. In addition to the above feature, a new modified SEPIC topology along with a seven level inverter is proposed in this paper which contains high gain conversion capability, There are many SEPIC topologies are available with unique features [9,10].

Since the invention of the multi-level inverters there is more popularity and attention in the distributed energy resource sectors. The multi-level inverters reduce the total harmonic content of the output waveforms and also proved easier way in design or implementation [11,12]. A lot of research works are carried out in the field of multi-level inverter topologies. Due to the increase circuit complexities and a large count of passive component usage, the number of level increase suffers from few drawbacks of their own. Therefore, to overcome those demerits of the conventional multi-level inverter topologies there aroused many different types of multi-level inverter topologies. Each type of new MLI topologies focused on overcoming down one or more drawbacks of the conventional topologies. Further, some topologies are with reduced number of switching device [13]-[15].

MLI with a reduced number of DC sources is symmetrical or asymmetrical in arrangements and some incorporate both these factors. Now, the study is based on further reducing the number of switch count and maximizing the total number of output levels of the multi-level inverter [14].

The harmonic reduction is one of the key factors that decide the performance of multi-level inverter. As the number of levels in the output waveform is replicated, the shape of the sinusoidal waveform reduces the harmonics. This is a particular way to reduce the harmonic content of the output waveform and another type is by using PWM techniques for switching pulse generation. The Multiple Carrier Sinusoidal Pulse Width Modulation (SPWM) is common and an efficient PWM technique is used for MLI [15].

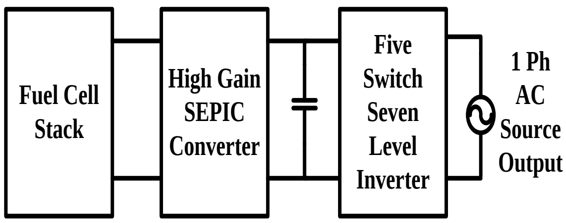


Fig.1.Block diagram for FCECS with proposed converter structure

The proposed MLI has five active power semi-conductor devices with single DC source that makes seven-level AC output. The modified SEPIC is integrated with the proposed seven-level inverter to provide 230V, 50Hz AC waveform. The output of this projected converter system can be used for residential applications. The block diagram of the planned structure is shown in figure.1.

This anticipated FCECS consists of fuel cell stack, Modified SEPIC converter, seven-level Inverter, LC filter and Load. Fuel cell stack is the source of SEPIC converter, as it boosts the input DC voltage and provides constant DC to the proposed inverter through DC link capacitor. The 230V, 50 Hz AC output is taken from the inverter through LC filter. Figure.2. shows the dynamic response of the 1 kW fuel cell stack. The fuel cell voltage and current value is changed according to the power value. Thus, the DC output of the fuel cell stack is changed when the load changes take place. So it needs DC-DC converter prior to the specified inverter.

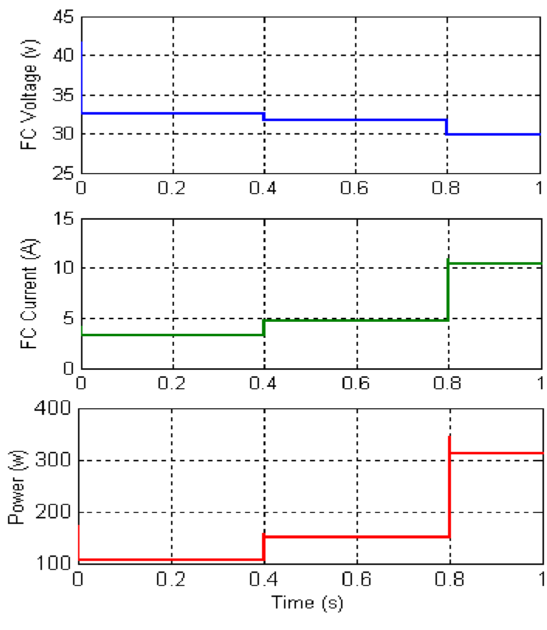


Fig.2. Fuel cell dynamics with change in load

The design of this FCECS is detailed in the following sections, operational principle and comparative analyses are also illustrated in depth with appropriate simulation results and with its experimental validation.

II. Proposed Seven Level Inverter Based Fuel Cell Conversion System

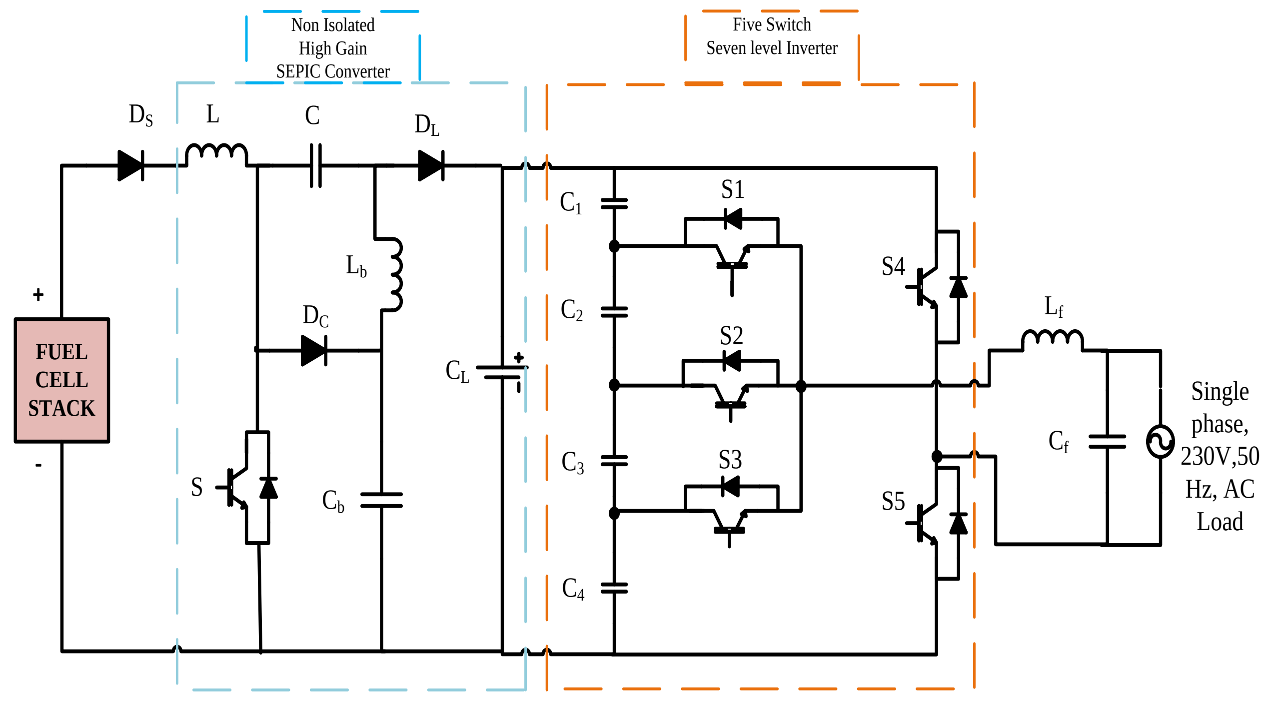


Fig.3.Proposed FCECS Structure

The output of the SEPIC converter is then interfaced with a seven-level inverter, which offers the following benefits: reduced switching and conduction losses, mitigated output DC ripple, and the removal of DC link capacitor leakage compensation problems. The size and cost of the projected inverter is reduced by reduction with a number of active power semi-conductor devices, its control design, isolation and driver modules, allowing for the standalone load operation. Furthermore, the insertion of a middle stage decouples multiple control variables, thus reducing overall system control complexity.

Both SEPIC and seven level inverters are an equal importance of making such an integrated structure, these converters are modified structures of the conventional converters. SEPIC converter is modified for providing high gain and low voltage stress on power semi-conducting devices, likewise, seven-level inverter is modified to provide seven-level output with less number of switching devices than the conventional seven-level cascaded bridge inverter and other types of configurations. Though the modified SEPIC a source of non-isolated nature diode D_S will act as a reverse blocking diode to isolate source from residential loads, also it provides non-inverted output due to load side diode D_L as like as in a classical SEPIC converter.

The FCECS switching devices and other passive elements parameters are also taken into consideration to provide smooth output waveform, in addition, LC filter are further smoothen to eliminate unwanted harmonics as superior as possible. All the standard needs and protection systems are incorporated in all the ways to make this proposed system as a best alternative renewable energy converter system for residential applications among all the other systems. The upcoming results of this work will prove that this is a best efficient system. The structure of the FCECS is depicted in figure.3 with all necessary notations.

2.1 High Gain Modified SEPIC Converter

The modified SEPIC converter is personalized from conventional SEPIC by adding capacitor C_b and diode D_c. Figure.4 shows the operating waveforms of the SEPIC converter during normal conditions. The Inclusion of the D_C,C_b leads to the high voltage gain than the classical one. For a 30V fuel cell input voltage, the converted output voltage is around 380V DC as shown in figure.4.

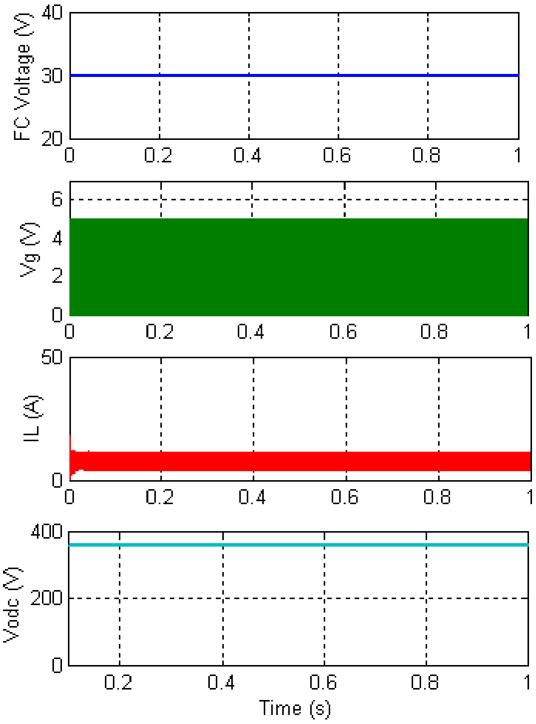


Fig.4.SEPIC converter operating waveforms

The inductance current profile and gate voltage are also shown in the figure. The additional capacitor C_b is used to enhance the voltage level than a SEPIC converter, D_C is used to create a path for mode 2 operation during switch OFF condition to make continuous current flow in the load circuit.

2.2 Proposed Five Switch Seven Level Inverter

The integrated seven-level inverter topology of FCECS is shown in Figure 5. The inverter uses a total of five switching devices to provide an output voltage with seven steps unlike twelve are required in the conventional MLI topologies. The input DC sources sectionalized into four with a capacitor and they are symmetrically arranged. Each level is obtained by the additive and subtractive value of the DC sources. The switching elements are connected to provide seven levels of the output waveform. For the ease of analysis purposes, the power electronic switches are considered to be ideal. The single-phase modified H-bridge seven-level MLI topology is significantly advantageous over the other H-bridge topologies, i.e., fewer power switches and no power diodes or balancing capacitors are required for inverters of the same levels.

Proper switching sequence for the multi-level inverter produces seven output voltage levels from

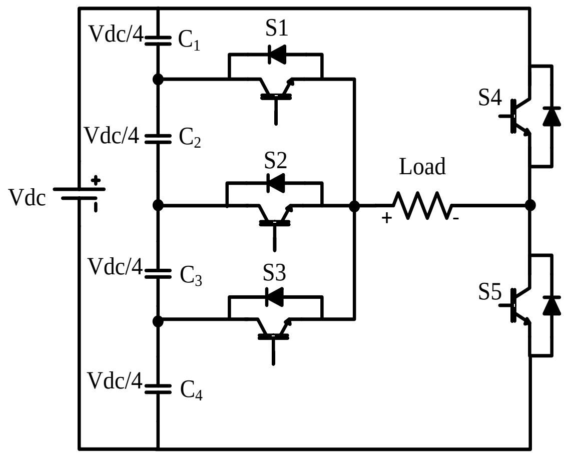


Fig.5.Seven level inverter topology

a single DC source through the capacitive voltage sources, namely +3Vdc/4, +2Vdc/4, +Vdc/4, 0, -Vdc/4, -2Vdc/4 and –3Vdc/4. For every level, only two switches are in the ON state and the remaining three switches are in the OFF state. A resistive load is connected, so as the output current is in phase with the output voltage. It is significant that every switch produces a relative loss during the ON and OFF operations, so reduced switch count proves to be an efficient one. Besides, this topology does not require any of the clamping diodes or clamping capacitors in the circuit.

TABLE I

COMPARATIVE TABLE - 7 LEVEL INVERTER

Topology	Diode Clamped	Flying Capacitor	Cascaded H-bridge	Proposed System
Level	7	7	7	**7**
Switches	12	12	12	**5**
DC source	1	1	3	**1**
Clamping diodes	15	--	--	**--**
DC capacitors	--	15	--	**4**

2.3 Principle of Operation

Figure.5 is the proposed seven-level MLI topology with a resistive load connected to it. The multi-level inverters' operation possibly divided into seven working states based on switching aspect: as given in figures 6 (a-f) of which three are positive and three are negative cycle states with zero state is also added for seven-level operative conditions. The seven output voltage levels of the proposed seven-level modified bridge inverter are generated as follows:

Mode 1:

Maximum positive output (+3Vdc/4): S1 and S5 controlled switches are in ON state. The S1 connects the load positive terminal to the positive of second DC capacitive source and S5 connects the load negative terminal to the negative of the fourth DC voltage source. The three DC capacitive sources are now connected in series ensuring +3Vdc/4 across the load terminal. Figure 6 (a) shows the active current paths that are present in this state.

Mode 2:

Two-third positive output (+2Vdc/4): S2 and S5 controlled switches are in ON state. The S2 connects the load positive terminal to the positive of the third DC capacitive source and S5 connects the load negative terminal to the negative of the fourth DC capacitive source. The two capacitive sources are now connected in series resulting +2Vdc/4 at to load terminal. Figure 6(b) shows the active current paths are present in the current state.

Mode 3:

One-third positive output (+Vdc/4): S3 and S5 controlled switches are in ON state. The S3 connects the load of a positive terminal to the positive of fourth DC capacitive source and S5 connects the load negative terminal to the negative of the same DC voltage source. Only one DC capacitive source is now connected resulting +Vdc/4 at to load terminal. Figure 6 (c) shows the active current paths that are present in this state.

Mode 4:

Zero state output (0V): All the switches are to be in OFF condition during this mode of operation. Meanwhile, no voltage is presented across the load, thus the load disconnects from the capacitive voltage sources and furnishes out 0V at load terminal.

Mode 5:

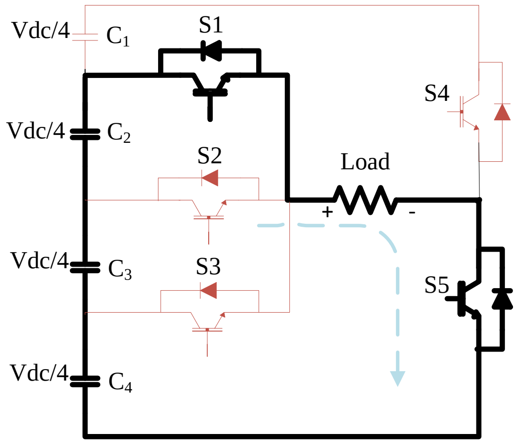
One-third negative output (-Vdc/4): S1 and S4 controlled switches are in ON state. The S1 connects the load positive terminal to the negative of first DC capacitive source and S4 connects the load negative terminal to the positive of the same DC capacitive source. Only one DC source is now connected in reverse polarity giving out –Vdc/4 at to load terminal. Figure 6 (d) the active current paths that are present in this state.

Mode 6:

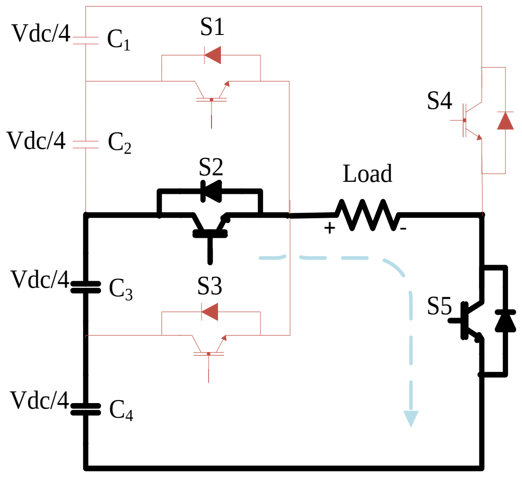
Two-third negative output (-2Vdc/4): S2 and S4 controlled switches are in ON state. The S2 connects the load positive terminal to the negative of second DC capacitive source and S4 connects the load negative terminal to the positive of the first DC capacitive source. The two DC capacitive sources are now connected series in reverse polarity with -2Vdc/4 at to load terminal. Figure 6 (e) shows the current paths that are active in this state.

Mode 7:

Maximum negative output (-3Vdc/4): S3 and S4 controlled switches are in ON state. The S3 connects the load positive terminal to the negative of third DC capacitive source and S4 connects the load negative terminal to the positive of the first DC capacitive source. The three DC sources are now connected series in reverse polarity giving out -3Vdc/4 at to load terminal. Figure 6 (f) shows the current paths that are active in this state.



(a)



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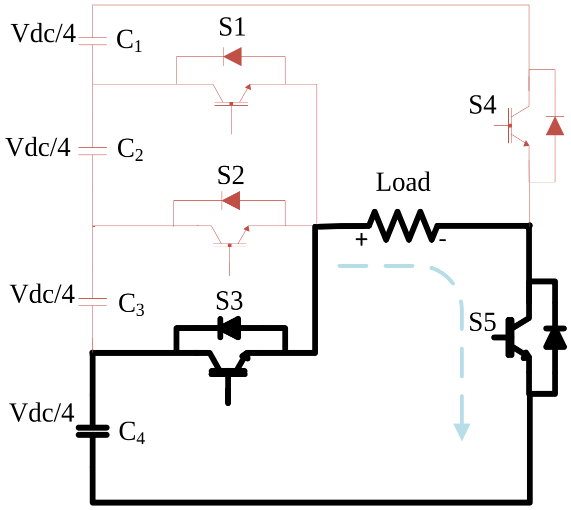

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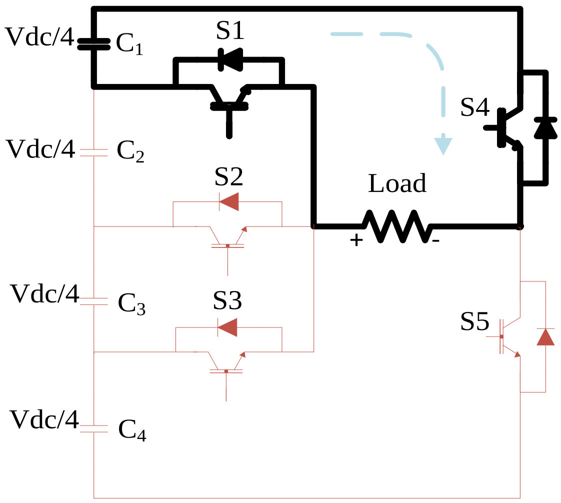

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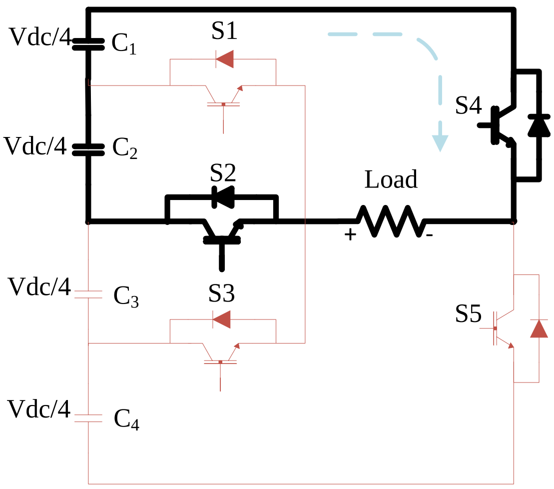

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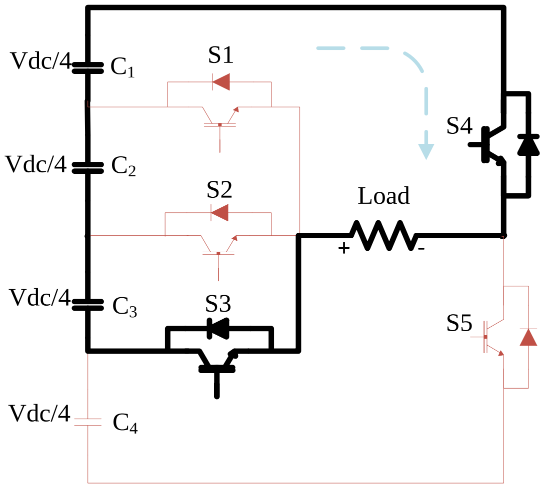


(f)

Fig.6 (a-f). Conduction paths of the proposed inverter configuration

III. Modulation Control for a Seven Level Inverter

In the proposed modulation control, the operating carrier wave is from 3 KHz to 11 KHz. The reason for moving onto high-frequency switching is that the lower order harmonics are eradicated from the output waveform. Conventionally, the PWM signals are generated using a single reference and three carrier waves.

But in high switching frequency, the switches undergo rapid turned ON and OFF states for a large number time within a short span of time. This causes various undesired effects like heating effect in the IGBTs, furthermore enhancing the switching losses. Hence, to overcome these ill-effects, less number of switching devices is used in this topology.

The switching signals are generated using Multiple Carrier Sinusoidal Pulse Width Modulation (SPWM). The commonly used three multi-carrier PWM techniques are Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) [6]. Out of which APOD provides superior harmonic performance than other carrier patterns which is used in this inverter control significance. Altogether three carrier triangular signals that are identical to each other with an offset that is equivalent to the amplitude of the single sine reference signal were used to generate the PWM pulses.

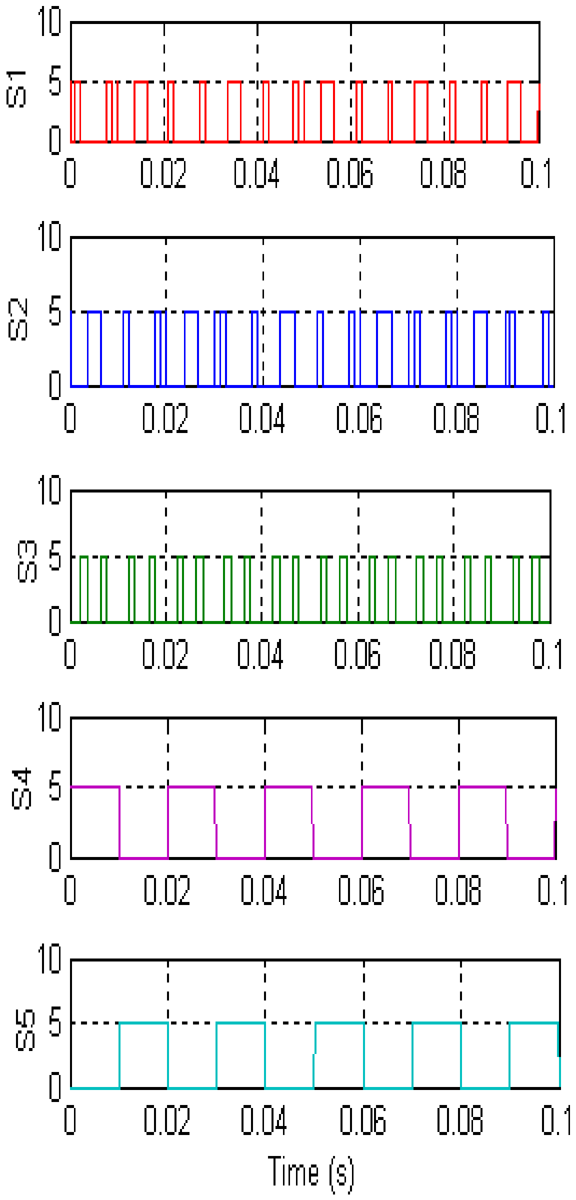
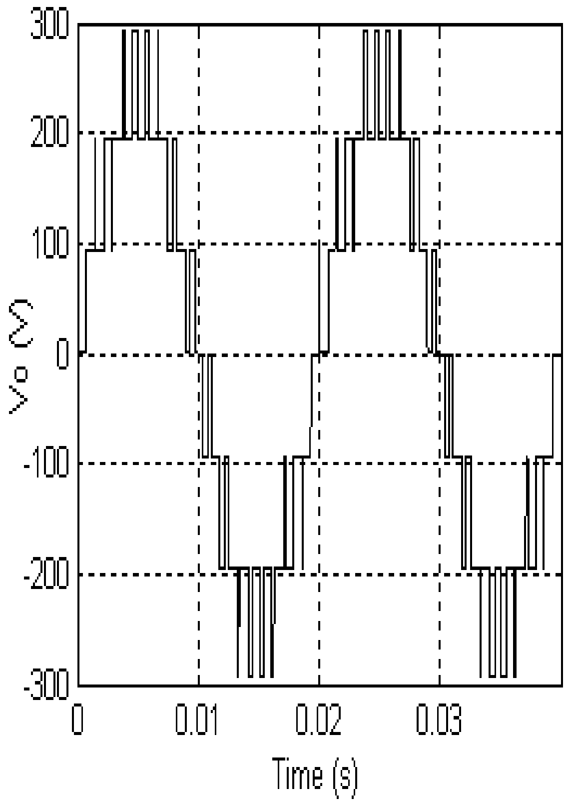


Fig.7. Control pulses for seven-level inverter with APOD carrier pattern

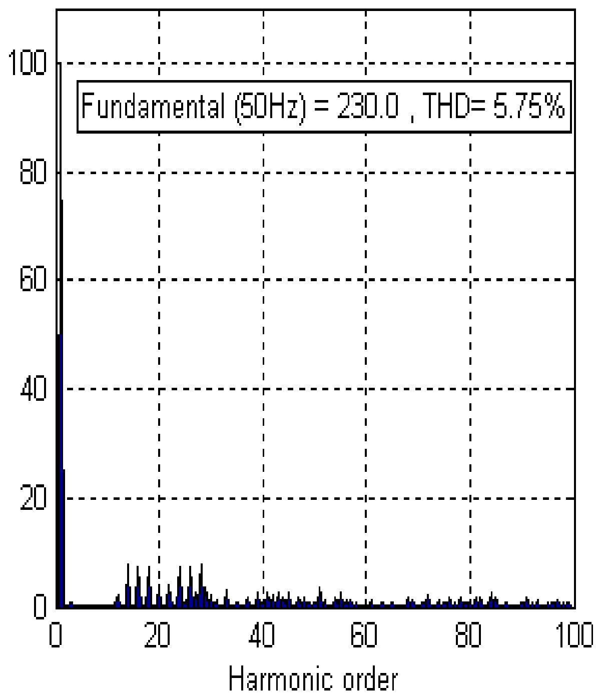
The control pulse pattern for S1-S5 with carrier frequency of 5 kHz is shown in figure.7.

IV. Simulation and Experimental Results

The simulation is done for the proposed single-phase seven-level MLI topology with five switching devices using MATLAB/Simulink software.



(a)



(b)

Fig.8(a, b). Output voltage waveform and its spectral response without filter in proposed inverter

The nature of the inverter output voltage waveform is shown in figure.8 (a). In the harmonic spectrum of the phase voltage in figure.8 (b), the first group of harmonic components is shifted to high-frequency region and its measured Total Harmonic Distortion (THD) value without filter is 5.75%.

THD is the performance indicator, which evaluates the quantity of harmonic contents in the output voltage waveform. THD is measured up to 50th harmonic order from linear to over modulation ranges with the same carrier frequency as shown in figure.9.

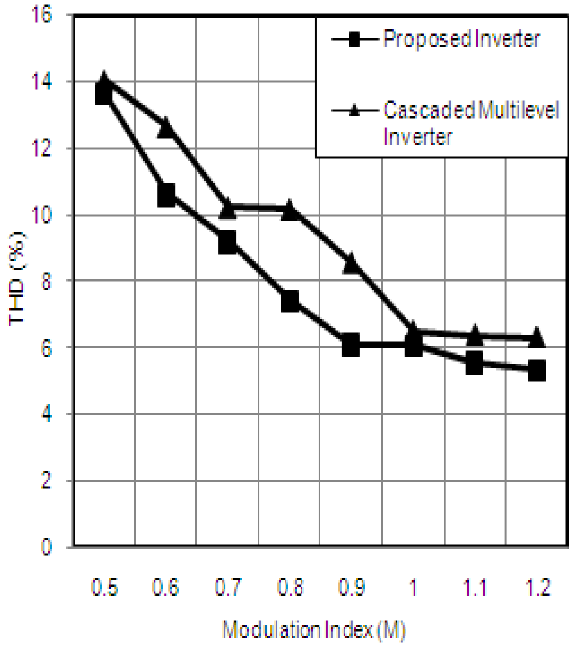


Fig.9. THD Comparison of the proposed Inverter with a cascaded multilevel inverter.

This result shows that significantly lower THD with proposed system compared to the conventional one, thus the superiority of the voltage waveform nature.

V. Prototype Description

Programmable DC source is used as input for the proposed converter, the characteristics is treated as same as 1kW Nexa fuel cell stack. The DSP processor TMS320F2407A is used as switching pulse pattern controller for this converter and inverter switches. The utilised Power IGBTs are from Fairchild Semiconductor, ISL9V2040D3S are employed in this developed prototype. Its operating Drain–to–Source voltage is up to 400V and tolerates the drain current value up to 10A. Vishay vo–1350a is an opto–coupler driver IC used for switching pulse generation. The proposed model is shown in the following figure.

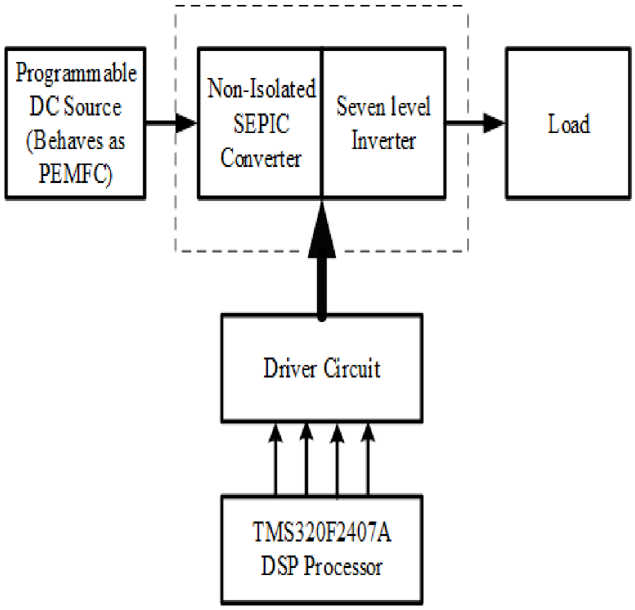
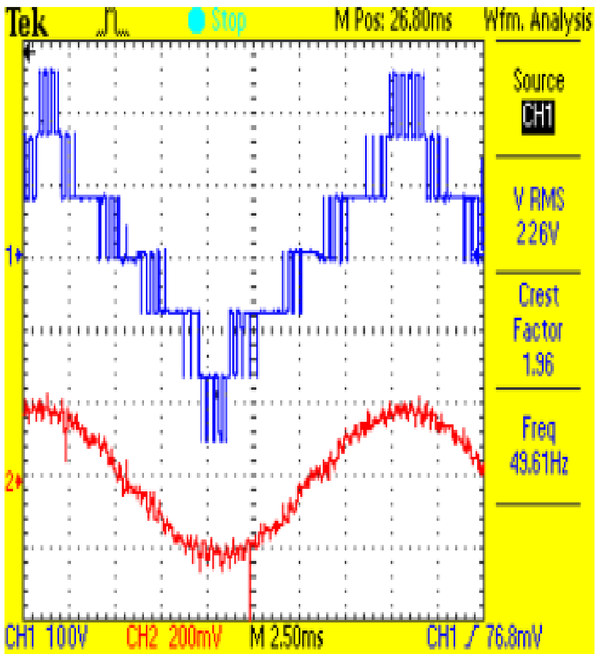
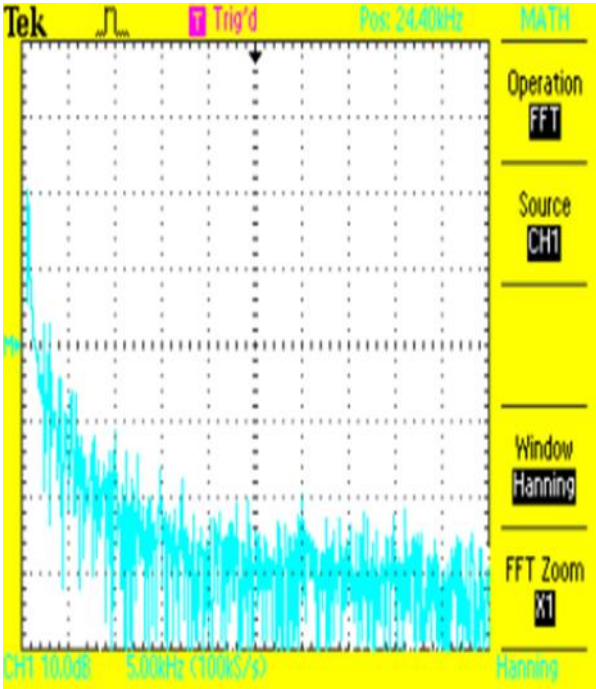


Fig.10. Prototype model of the proposed system

The following waveforms prove the effectiveness of the proposed prototype.



(a)



(b)

Fig.11(a, b) . Experimental output voltage and current waveforms with spectral analysis

Figure.11 (a) shows real-time seven-level voltage waveform and figure.11 (b) represents FFT of output voltage waveform.

The lower order harmonics are eliminated in the current waveform and the higher order current harmonics are filtered by the nature of the inductive load, so the current waveform is close to sinusoidal shape. In a practical power converter, the operating efficiency is more depended on switching losses and conduction losses; therefore, reducing the number of active switches become important for improving the efficiency of the converter.

The measured efficiency of the proposed converter is compared in figure. 12 to the efficiency of the conventional cascaded MLI for several values of load power. Proposed converter performance can easily evaluated by this above comparison chart.

Despite slightly lower efficiency under the lightly loaded conditions, the effective converter efficiency is increased by about 3%, which a significant improvement of the fact that the conventional converter topology already has efficiency greater than 90%.

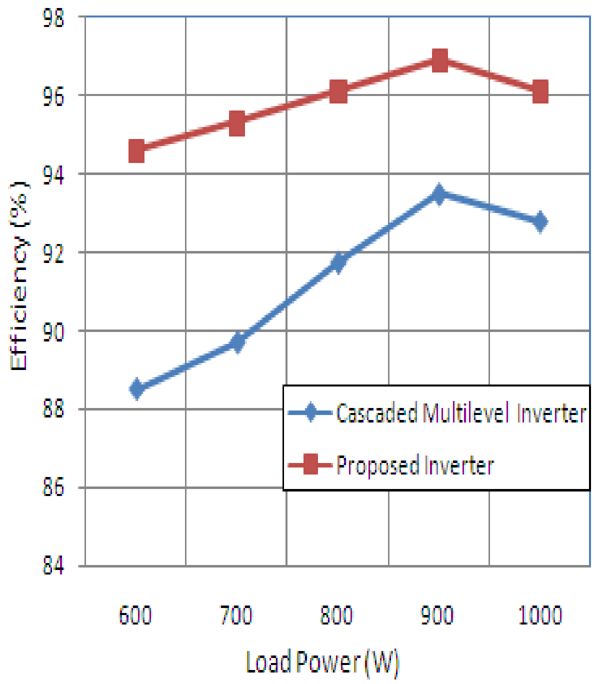


Fig.12. Efficiency comparison of the proposed structure with existing seven-level inverter

VI. Conclusion

A stand-alone single phase Fuel cell sourced power supply is designed with five switch seven-level inverter along with non-isolated SEPIC converter structure. The simulation and experimental results have shown the effectiveness of the power supply characteristics. The result of the proposed system satisfies the performance in delivering boost and inversion functions and capable of providing a 23OV, 50Hz AC from fuel cell output of 30V DC at rated power. The projected system has the feature of a simplified power circuit, high efficiency, low harmonic distortion and low cost.

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