MODELING AND SIMULATION OF DIFFERENT TOPOLOGIES FOR VSI BASED STATIC SYNCHRONOUS SERIES COMPENSATOR

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Abstract: In this paper mathematical models and simulation of different topologies for voltage source inverter (VSI) based static synchronous series compensator are discussed. An overview of different topologies like twelve pulse, forty eight pulse multi-pulse, five level diode clamped multi-level and five level hybrid multi-level in terms of its working principle, merits and demerits are discussed. Modeling and simulation of these topologies using PSCAD software is given.

Key words: Static Synchronous Series Compensator, Multi-Pulse Inverter (MPI), Multi-Level Inverter (MLI), Hybrid Multi-Level Inverter (HMLI)

I INTRODUCTION

The recent advances in power electronics have led to the development of flexible alternating current systems (FACTS). Utilities are beginning to install FACTS devices in their transmission networks due to increase in power system requirements.

The FACTS controllers which are used in series with transmission line are thyristor controlled series compensator (TCSC), GTO controlled series compensator (GCSC) and static synchronous series compensator (SSSC). First two uses the static capacitor in the circuit and third one is based on a voltage source inverter. Voltage is inserted in quadrature with line current.

In [1] it is shown that by dynamically changing the series impedance of the transmission line by controllable series capacitive compensator the oscillations can be damped. Damping of power oscillations using controllable series compensation is insensitive to system load characteristics SSSC which can provide controllable compensating voltage over an identical capacitive and inductive range independently of the magnitude of the line current is usually implemented by GTO based voltage source inverter (VSI).

Basic Characteristics of SSSC is given in [2]. Modeling and control of a 48-step SSSC with a PI controller are presented in [3].

The switching frequency of the commutating devices for a power converter is severely limited and must be kept low. The multi pulse converter has a switching frequency as the fundamental frequency of the output voltage for a 50/60 Hz utility voltage.

This limits the switching losses as well as the heat in the commutating devices [4]. In [5] a three level multi level inverter based SSSC is discussed. In [6] a cascaded multilevel inverter based SSSC is discussed. The major disadvantage with multilevel inverter is as the no. of level increases it is difficult to balance the voltage across dc link capacitors. This drawback can be dealt with hybrid multilevel inverter. A hybrid MLI is suggested in [7], for induction motor drive.

For applications like medium power drives and electric vehicles the topology suggested may be a valid solution to reduce the burden of dc link voltage balancing. In [8] a possible combination of three level diode clamped MLI with two level inverter may reduce the burden of dc link voltage balance controller for large power applications like series facts controller SSSC. The proposed topology will reduce the number of devices to build five level MLI compared to topology suggested in [9].

In this paper different topologies for developing voltage source inverter (VSI) based SSSC are discussed. The PSCAD software is used in designing the different VSI topologies.

In remaining part of the paper, the following sections are discussed. In Part II mathematical model of multipulse SSSC is presented. In part III five level diode clamped MLI is explained. In part IV five level hybrid VSI is explained and in part V the comparison of the above VSI topologies is given.

II SSSC MODELING

SSSC is basically a voltage source inverter connected in series with transmission line. The function of the VSI is to inject a voltage in quadrature with the line current. Fig.1 shows the single line diagram of a transmission line with SSSC as a series compensator.
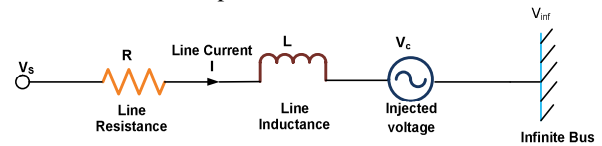

Fig.1 48 pulse SSSC compensated transmission system

The injected voltage is given by (1)

$$V_q = V_c = -jX_cI = -jkXI \tag{1}$$

Where

V_c is the injected compensating voltage   phasor

I is the line current

X_c is the reactance of series capacitor

X line reactance

K=X_c/X = degree of compensation.

If we neglect the harmonics the system equations can be written in terms of dq0 reference frame. The basic equation for the transmission line with voltage source as an SSSC is given by

$$L \frac{dI}{dt} + RI = V_s - V_c - V_\infty \tag{2}$$

Where V_s and V_R are sending and receiving end voltages in per unit. V_c is the injected voltage in per unit. L and R are inductance and resistance of line in per unit. If we will convert the equation (2) in dq0, then it is given by

$$\frac{d}{dt}\begin{bmatrix} i_D \\ i_Q \end{bmatrix} = \begin{bmatrix} -\frac{\omega R_T}{X_T} & -\omega \\ \omega & -\frac{\omega R_T}{X_T} \end{bmatrix} \begin{bmatrix} i_D \\ i_Q \end{bmatrix} + \begin{bmatrix} -\sqrt{3}\frac{\omega}{X_T}\sin\theta_f \\ -\sqrt{3}\frac{\omega}{X_T}\cos\theta_f \end{bmatrix} V_{dc}$$
$$+ \begin{bmatrix} \frac{\omega}{X_T} & 0 \\ 0 & \frac{\omega}{X_T} \end{bmatrix} \begin{bmatrix} v_D - v_{D\infty} \\ v_Q - v_{Q\infty} \end{bmatrix} \tag{3}$$

$$\frac{d}{dt}V_{dc} = \begin{bmatrix} \sqrt{3}\,\omega\, X_{dc}\sin\theta_f & \sqrt{3}\,\omega\, X_{dc}\cos\theta_f \end{bmatrix} \begin{bmatrix} i_D \\ i_Q \end{bmatrix}$$
$$- \frac{\omega X_{dc}}{R_{dc}}V_{dc} \tag{4}$$

Where

i_D and i_Q are D and Q component of line current

X_T is a total reactance including line reactance and SSSC reactance.

R_T is a total resistance including line resistance and SSSC resistance.

X_{dc} is the dc link capacitor reactance

is base frequency in per unit

V_{dc} is dc link voltage in per unit

This injected voltage can be obtained by either using multipulse or multilevel voltage source inverter topology. In the remaining part of this paper these topologies are discussed in detail.

III MULTI PULSE VSI

The multipulse inverter can be obtained from the combination of several converter modules switching at the desired fundamental frequency. Three phase converters switching at the fundamental frequency are known as six pulse inverter. 12-pulse inverter made up from two 6-pulse inverters.

In this case the successive inverter-transformers must have a phase difference of 30^0. If we now add two such inverters, we shall be able to get a 24-pulse inverter. In

this case the successive inverter-transformers must have a phase difference of 15^0.

In a similar way, we can construct a 6q-step inverter by making a phase shift of 360^0/6q between the successive inverter-transformers. 48-pulse inverter will require eight 6-pulse inverters along with suitable magnetic circuits. Fig. 2 shows the block diagram of 48 pulse VSI based inverter. SSSC is inserted in line with interfacing transformer.
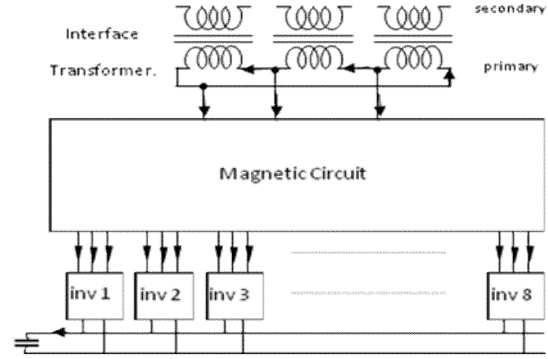

Fig.2 48 pulse SSSC compensated transmission system

The successive inverter phase shift is 7.5^0. The main problem with the 6-pulse inverter is lower order harmonics (5th and 7th harmonics are dominant. This can be resolved by using 12-pulse converter. The minimum harmonics level will be of 11th and 13th number. The 5th and 7th harmonics will get eliminated by suitable secondary winding connections of two transformers.

Fig. 2 shows the block diagram of 48 pulse VSI based inverter. SSSC is inserted in line with interfacing transformer. The minimum harmonic in 48-Pulse inverter is 47th and 49th. By increasing the number of pulses the harmonics of lower orders can be eliminated from output voltage.

With the help of PSCAD software an SSSC model is developed with 12 pulse and 48 pulse VSI. The equation which governs the voltage level and the firing angle of switching devices is given by

$$V_{ac} = \frac{k\sigma\sqrt{3}}{\pi}V_{dc}\sin(\omega t + \theta_f) \tag{5}$$

Where

V_{ac} output voltage of n pulse inverter

k factor based on no. of pulses
for 6 pulse it is 2
for 48 pulse it is 16

σ interface transformer turns ratio

V_{dc} d.c.link voltage

θ_f firing angle

The modular construction of multipulse topology can make the design of VSI flexible. For getting the desired number of pulses the phase shift and turns ratio of

transformers is given in Table I below.
For inverters 2, 3 and 4 =7.5, 15 and 22.5 degrees.
For inverters 6, 7 and 8 Ø=7.5, 15 and 22.5 degrees

TABLE I
Phase Shift and turns ratio for 48 pulse VSI

Inverter number	Primary	Secondary	Tertiary
1	1	$1/\sqrt{3}$	-
3 & 4	1	$Cos \; /\sqrt{3}$	Sin
5	1	1	-
6 ,7 & 8	1	CosØ	$SinØ/\sqrt{3}$

To meet with the losses in the converters and switching loss, a firing angle is controlled with the help of PI controller based closed loop control system. Fig. 2 shows the block diagram of closed loop system of PI controller and power system with 48 pulse VSI based SSSC.

The input to the PI controller is the error between actual and reference dc voltage. Output is in terms of   . It is added with $_{ref.}$ G(s) is the transfer function of total system including SSSC.

Fig. 3 Block diagram of an SMIB system with PI controller as a single input single output (SISO) system

The 48 pulse multi pulse inverter is implemented in PSCAD. The voltage is measured at transmission line level and it is scaled down so that it can be used for PLL application. For every six pulse converter the phase shift of 7.5 degree each (7.5, 15, and 22.5 degree) a control logic circuit is developed.

Fig. 3 shows the SSSC output voltage in kV. Each half cycle consists of 24 pulse shape. The reference voltage is 10 kV. The firing angle is 94.485°. The 48 pulse output voltage is shown in Fig. 4. Harmonics spectrum is shown in Fig. 5. The minimum harmonics is 47th. The fundamental frequency switching is used.
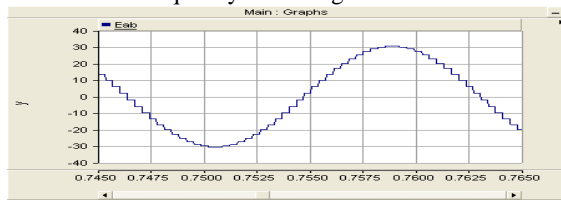
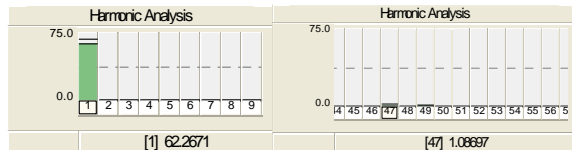

Fig. 4 Forty eight pulse output voltage waveform of SSSC

Fig. 5 Harmonics spectrum of forty eight pulse SSSC

IV FIVE LEVEL MLI BASED VSI

The multipulse inverter although it is advantageous for re moving the lower order harmonics, it involves more and more magnetic circuit due to which the size and cost increases and response time to abnormal condition to react increases.

Due to continuous advancement in power electronics devices and new technologies available in the form of digital control of power electronics based converters, a new breed of transformer less multi-level inverters have come up for high power high voltage applications. There are several types of multilevel inverters.

The three main types of multilevel converters are diode-clamped multilevel converters, flying-capacitor (also referred to as capacitor-clamped) multilevel converters, and cascaded H-bridge multilevel converters.
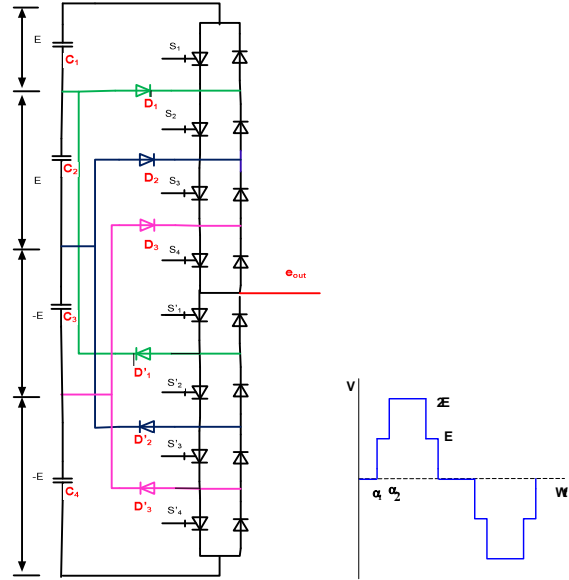

Fig. 6 Power circuit diagram of a five level MLI based SSSC

The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltages these dc voltages may or may not be equal to one another. The ac voltage produced from these dc voltages approaches a sinusoidal. In this paper a five level diode clamped multi level inverter is used as a voltage source inverter to model SSSC. Fig.6 shows a simple arrangement of one phase of a five level inverter. The equation which governs the voltage level is given by(6)

$$V_{ac} = \frac{4\sigma\sqrt{3}}{n\pi} V_{dc} \; \sin(\omega t + \theta_f) \quad (6)$$

Where n= no of levels of output voltage, odd 3, 5…

$$V\left(\omega t\right) = V_C\left(\alpha_1, \omega t\right) + V_C\left(\alpha_2, \omega t\right) \quad (7)$$

$$H\left(n\right) = \frac{4V_C}{n\pi}\left[\cos\left(n\alpha_1\right) + \cos\left(n\alpha_2\right)\right] \quad (8)$$

Where n=1, 3, 5, 7---

Equation (7) and (8) gives an idea about the output voltage of an inverter with selective harmonic elimination (SHE) technique.

Equation (7) gives the output voltage with two switching angles α_1 and α_2 (8) gives the magnitude of nth harmonic. α_1 and α_2 can be between 0 to 90^0 for getting lower harmonic content or a larger fundamental voltage.

For 5th and 7th harmonic elimination, we can simply take two equations of (8).

$$\cos\left(5\alpha_1\right) + \cos\left(5\alpha_2\right) = 0$$

$$\cos\left(7\alpha_1\right) + \cos\left(7\alpha_2\right) = 0 \qquad (9)$$

Equation (9) can be solved using Newton-Raphson method. With the help of matlab based program it gives $\alpha_1 = 5.1429^0$ and $\alpha_2 = 30.8571^0$ respectively. The minimum harmonics in the five-level inverter output voltage with SHE technique will be 11th harmonic. In general for an N-level inverter, (N-1)/2 harmonics can be eliminated for N odd and (N/2-1) harmonics for N even.
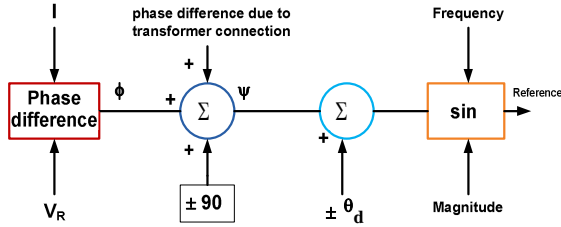

Fig. 7 Control logic block diagram for multilevel based SSSC

Fig.7 shows the phase angle controller used for generating a voltage signal in quadrature with the line current of one phase. The controller calculates the line current angle ( ) with reference to the receiving-end voltage (V_R) considered as the reference phasor (=0).

The phase angle of the generated signal is -90 or +90 degrees for capacitive or inductive mode respectively. A phase shift of 30 degrees is added to compensate for star-delta connection of transformer.
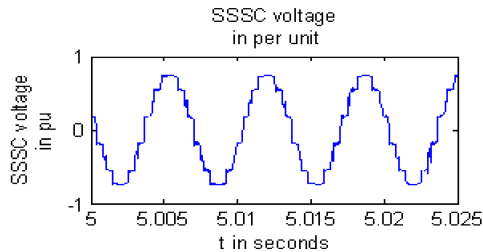

Fig. 8 Nine level L-L output voltage of five level SSSC

The angle obtained from capacitor voltage controller is added or subtracted from depending on whether the capacitor voltages are above or below the normalized

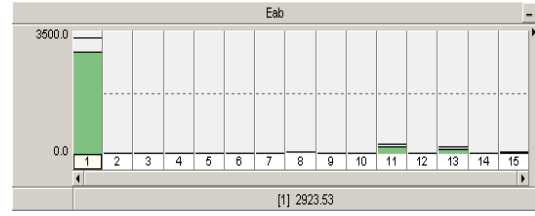levels. In Fig. 8 the output of five level multi level VSI based SSSC is shown.

Fig. 9 Harmonics spectrum of five level MLI based SSSC

By proper selection of PI controller parameters an equal output in both half cycles have been achieved. The harmonics spectrum of the Fig. 8 output voltage is shown in Fig.9.
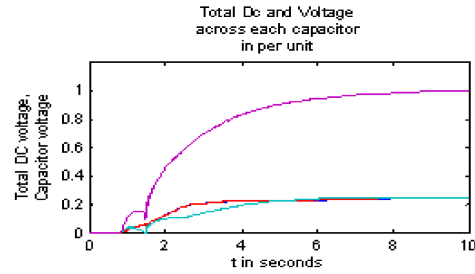

Fig.10 DC link voltage across capacitors for five level MLI

Due to implementation of SHE technique the fifth and seventh harmonics get eliminated from the output voltage of VSI. If any unbalance in the voltage across all the four capacitors will change the minimum harmonic level to 5th from 11th. Fig. 10 shows the total dc link voltage and voltage across all the four capacitors of dc link. A PI controller based d.c. link voltage balance controller is used to balance voltage across 4 capacitors.

V HYBRID FIVE LEVEL MLI BASED VSI

To minimize this difficulty mentioned in section V of this paper in developing the voltage balance controller for five level inverter, a hybrid multi level inverter is suggested in [4]. A two level inverter single phase output is connected as an input to single phase H-bridge inverter.

This topology may be valid for medium power application like industrial drives, electric vehicles etc. For high power application like transmission level FACTS controller a two level VSI in parallel with diode clamped three level VSI.

Fig. 11 shows a five level hybrid MLI power circuit diagram. For each phase only six devices are required. By using this hybrid topology one can save two devices as compared to five level VSI proposed in [9] also at the same time it reduces the work to design a voltage balance controller for voltage across four dc link capacitors to two capacitors.

As shown in Fig. 12, the output voltage waveform of a two level inverter is two levels either positive or negative on reference axis. The output waveform is having three

levels either negative, zero and positive value. The summing of these two voltage waveforms will give two levels on positive side, zero and two levels on negative side, total five levels.
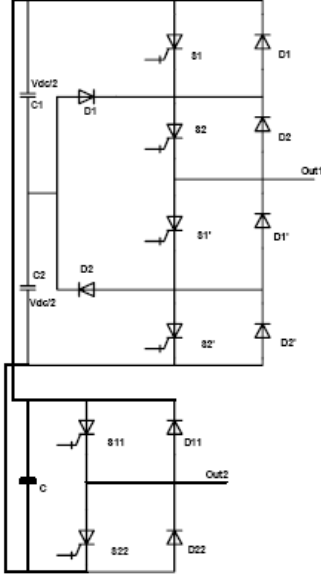

Fig.11 Power circuit Five level hybrid MLI based SSSC diagram

(a) Two level

Va0

(b) Three level
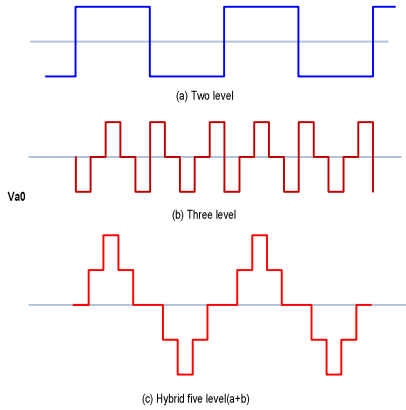
(c) Hybrid five level(a+b)

Fig. 12 Output voltage waveform for hybrid five level MLI based SSSC

The output voltage is a sum of two level and three level inverter output voltage level. The equation (10) gives the output voltage for fundamental frequency switching control. A PSCAD based circuit is developed to obtain five level hybrid VSI.

$$V_{ac} = \frac{2\sigma\sqrt{3}}{\pi}V_{dc}\sin(\omega t + \theta_{f1}) + \frac{4\sigma\sqrt{3}}{n\pi}V_{dc}\sin(\omega t + \theta_f)$$ (10)

Here the first part of RH side of equation gives output of two level. Angle is kept zero. And second half gives output voltage of three level inverter. Angle is set at 15 degrees. Where n= no of levels of output voltage normally odd 3, 5 etc.

This deviation from 90(θ_d) is calculated from the outputs of three PI controllers. One error signal passing through the first controller is the difference between the average of the dc voltages normalized for each level and a V_{dcref} of 1 per unit.

The output of the other three controllers is proportional to the difference between the average dc voltage in pu on all the dc sources, and each individual capacitor voltage measured and normalized to its reference value, producing some small angle θ_d.
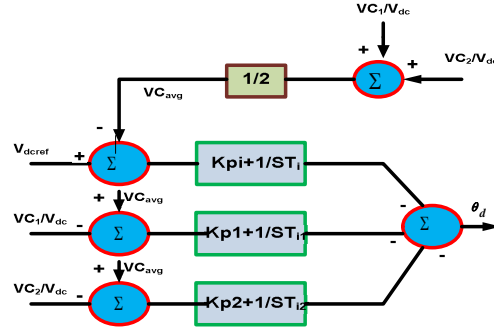

Fig. 13 control logic for dc link voltage balance controller

Fig. 13 shows the control logic for voltage balance across dc link capacitors. For hybrid five level MLI, with two and three level MLI connected in cascade, voltage balance controller is to be designed for three level MLI. By proper selection of PI controller parameters an equal output in both half cycles have been achieved. The output voltage is shown in Fig. 14.
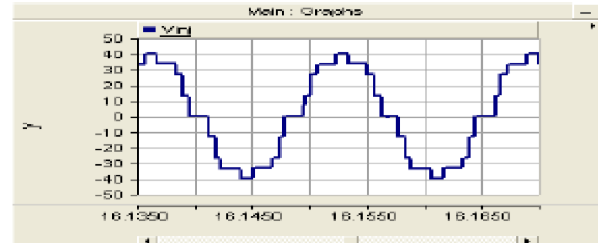

Fig. 14 Output voltage of five level hybrid VSI based SSSC

By proper selection of PI controller parameters an equal output in both half cycles have been achieved. The harmonics spectrum is shown of the above output voltage in Fig. 15.It shows that the minimum harmonic number is 11th.
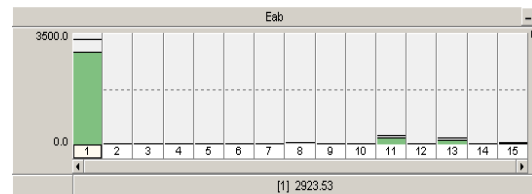

Fig. 15 Harmonic spectrum of five level hybrid VSI based SSSC

VI COMPARISON OF DIFFERENT TOPOLOGIES

Table II gives the comparison of different voltage source inverter topologies.

TABLE II
Comparison of different voltage source inverter topologies

Description	Multi-Pulse VSI (Twelve pulse)	Multi-Level VSI (Five level)	Hybrid VSI Five level
No of power switches required(per phase)	Four	Eight	Six
No. of diodes required	Four	Fourteen	Eight
No. of transformer required	One(Star/delta)	---	---
Design of Control circuit	Simple	Complex	Simple
Minimum harmonics	Eleventh	Eleventh	Eleventh
Physical Size	Biggest	Bigger	Smaller
Modular	Yes	Yes	Yes
Cost	Highest	Higher	Lower
DC link voltage balance controller	Easier to Design	Difficult	Less Difficult

CONCLUSION

In this paper a modeling and simulation of different topologies for VSI based SSSC is discussed. The output voltage equations for multipulse, multilevel and hybrid multilevel VSI are given. Selective harmonic elimination technique is used for five level multilevel inverter. The implementation of PSCAD software for developing these topologies with suitable control logic is briefed. From the comparison of all the topologies discussed, hybrid multilevel inverter may be more suitable compared to other topologies for developing an SSSC. Fundamental frequency switching is used for all the topologies. The minimum harmonic level is 11th for all the topologies discussed.

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