MULTI CARRIER BASED GENERALIZED PWM TECHNIQUE FOR REDUCTION OF COMMON MODE VOLTAGE

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Abstract: *This paper presents a multi carrier based generalized PWM algorithm for the reduction of common mode voltage in voltage source inverter fed induction motor drives. The generalized PWM algorithm is developed based on the concept of offset time. By using the magnitude test, the maximum and minimum time values are calculated at each sampling period from which generalized expression for offset time is derived. By varying a constant in offset time expressions, various PWM techniques like continuous and discontinues PWM techniques can be derived. As the single carrier based continuous and discontinuous PWM techniques generate large variations in common mode voltage, a multi carrier approach is presented in this paper. Based on the slope of reference voltages, suitable carrier signal will be selected. Moreover, by phase shifting the reference voltage signals by 120 degrees, a family of active zero state PWM (AZSPWM) techniques have been proposed in this paper. To evaluate the performance of these PWM techniques, experimental studies have been caried out on v/f controlled induction motor drives by using the dSPACE 1104 kit. From the experimental results it can be concluded that the proposed PWM techniques give superior performance in terms of common mode voltage when compared with the space vector PWM technique.*

Key words: *AZSPWM; Common Mode Voltage; Imaginary switching times; Space vector PWM*

1. Introduction

With the advancement in semi conductor technology, Voltage Source Inverters (VSI) fed induction motor are gaining importance in all commercial and industrial applications. Fig. 1 shows the IGBT based three phase VSI. With the application of high frequency pulse width modulated (PWM) [1-7] control signals to IGBT's, VSI generates controlled output voltage and frequency. The realization of PWM techniques can be carried out based on carrier comparison approach and digital approach. In carrier comparison approach, high frequency carrier signals are compared with reference signals to generate control signals. With the proper selection of reference signals, carrier comparison approach and digital approach gives similar pulse pattern [7]. In this paper much focus was given to carrier comparison approaches.

In carrier comparison approach, generation of modulating signals (reference signals) can be carried out based on scalar approach and space vector approach. Based on type of modulating signals, PWM techniques are classified into continuous modulating signal based PWM (CPWM) techniques and discontinuous modulating signal based PWM (DPWM) techniques [8]. Different simplified methods are proposed to reduce complexity involved in carrier comparison approaches [9-11].

For the generation of control signals to three-phase VSI, three reference signals are compared with common high frequency carrier signals. These conventional PWM techniques [1-11] aimed at reducing the current ripple, torque ripple and switching losses but still a persistent amount of common mode voltage is generated.

For a three-phase two-level VSI fed induction motor drive as shown in Fig. 1, the CMV is defined as the potential between neutral point of induction motor and midpoint of dc bus.

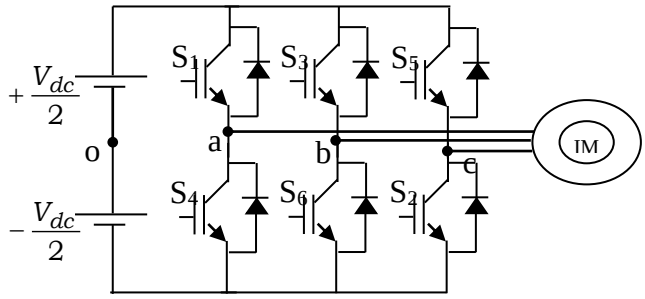


Fig. 1 Voltage Source Inverter schematic diagram

The mathematical expression for CMV can expressed in terms of individual pole voltages as follows.

$$V_{no} = \frac{V_{ao} + V_{bo} + V_{co}}{3}$$

As VSI inverter produces a non sinusoidal output voltage, there exist a predominant amount of common mode voltage. With conventional PWM algorithms, common mode voltage may take value of $\pm V_{dc}/2$. At high switching frequency and high input dc voltage the sharp edges of common mode voltage results in common mode currents which has adverse effects on motor bearings [11-12]. To reduce the effects of CMV different PWM techniques based were proposed [13-17]. The conventional common mode reduction PWM techniques [13-16] require complex calculation and storage space for this implementation. Scalar based PWM techniques provide freedom for the selection of reference signals and carrier signals [11]. Conventional PWM techniques [1-11] utilize the freedom in selecting the reference signals. But, in this paper to reduce the common mode voltage, freedom was utilized in selecting both reference signal and carrier signal. In the proposed PWM technique, multicarrier signals are used to generate control signals. The proper reference signals and multicarrier signals give identical results but implementation complexity is reduced with proposed PWM algorithms.

2. Proposed PWM Technique

The conventional carrier based Space Vector PWM (SVPWM) algorithm requires the angle and sector information to generate the required modulating signals. The complexity in generation of the required modulating signals can be reduced by using the concept of imaginary switching times. The procedure for the generation of modulating signals based on the imaginary switching times is discussed in detailed in [10]. Consider three reference signals of three phases as given in (1).

$$V_{in} = V_{ref}\cos(\theta - 2(r-1)\pi/3); \quad i = a, b, c \text{ and } r = 1,2,3 \tag{1}$$

From these instantaneous reference signals, the imaginary switching time can be directly calculated as defined in (2).

$$T_{in} = \frac{V_{in}}{V_{dc}} T_s \qquad i = a, b, c \tag{2}$$

From (3), it is observed that the switching times may be positive or negative, but depend on reference signals. Hence these switching times are called as imaginary switching times. Now the modulating signals can be generated using the expressions given in (3).

$$V_{in}^{*} = \frac{V_{dc}}{2}\left(\frac{T_{gi}}{T_s/2} - 1\right) \tag{3}$$

Where

$$\begin{aligned} T_{gi} &= T_{in} + T_s(1-k_o) + (k_o - 1)T_{\max} - k_o T_{\min} \\ &= T_{in} + T_{offset} \end{aligned} \tag{4}$$

$$T_{offset} = T_s(1-k_o) + (k_o - 1)T_{\max} - k_o T_{\min}$$

Now, by varying (k_0) between 0 and 1, various offset times (T_{offset}) can be generated. Among various modulating signals, popularly used continuous modulating signals (with $k_0 = 0.5$) is considered which is as shown in Fig.2.

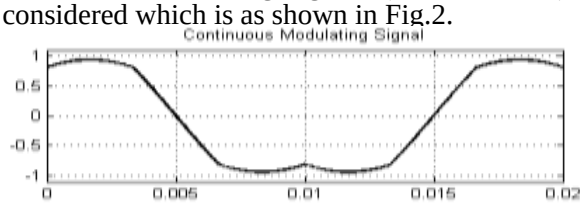
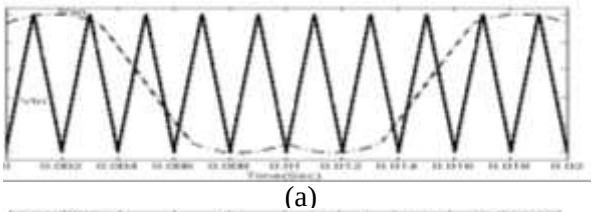


Fig.2 Continuous modulating signals

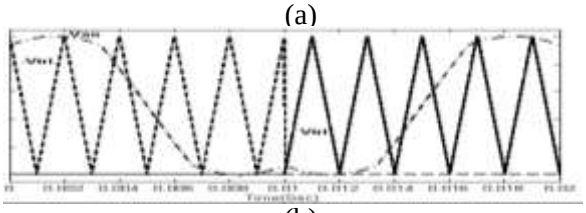
With the continuous modulating signal and common carrier signal for all the three phases yields conventional SVPWM technique. This SVPWM technique has superior performances in terms of ripple reduction and low switching losses but generates high CMV.

In the CMV reduction PWM algorithm, to generate the pulse pattern instead of common carrier signal to all the phases, multi carrier signals (V_{tri} and $-V_{tri}$) must be selected. The selection of carrier signal is done based on slopes of new reference signals which are given in Table 1. If the slope of reference signal is positive, then positive carrier signal (V_{tri}) is selected and compared with the corresponding phase modulating signal. If the slope of reference signal is negative, then negative carrier signal ($-V_{tri}$) is selected and compared with the corresponding phase modulating signal.

By changing the phase of reference signals used for the selection of carrier signals yields additional methods. The corresponding modulating signals and reference signals for selection of various PWM techniques are given Table 1. The realization of SVPWM and AZSPWM1 techniques are shown in Fig. 3.



(a)



(b)

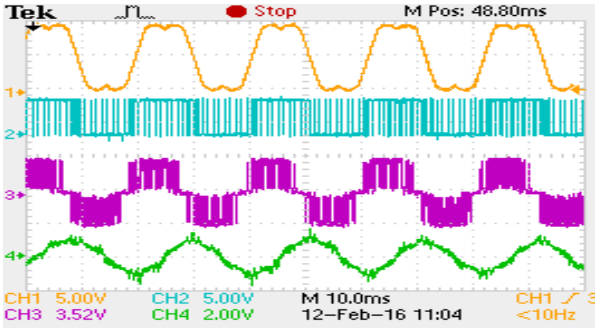
Fig. 3 Realization of carrier based PWM techniques (a) SVPWM (b) AZSPWM1

Type of PWM Technique	Modulating signals	Value of k_0	Reference signals for triangular selection
SVPWM	$V_{in}^{*} = \frac{V_{dc}}{2}\left(\frac{T_{gi}}{T_s/2} - 1\right)$ $T_{gi} = T_{in} + T_s(1-k_o) + (k_o - 1)T_{\max} - k_o T_{\min}$ $= T_{in} + T_{offset}$	0.5	Common carrier signals for all the phases
AZSPWM1		0.5	$V_{it} = V_m \cos(\omega t - 2(r-1)\pi/3)$ $i = a,b,c$ and $r = 1,2,3$
AZSPWM2		0.5	$V_{it} = V_m \cos(\omega t - 2(r-1)\pi/3 + 2\pi/3)$ $i = a,b,c$ and $r = 1,2,3$
AZSPWM3		0.5	$V_{it} = V_m \cos(\omega t - 2(r-1)\pi/3 - 2\pi/3)$ $i = a,b,c$ and $r = 1,2,3$

Table 1: Different Reference Signals for Generation of Switching Sequence

3. Results and Discussion

To test the performance of the CMV reduction PWM techniques, a prototype model of v/f controlled VSI fed induction motor drive is developed. In the laboratory prototype model, the drive is rated to a value of 9.2 KVA. A dc voltage of 510 V is applied to the VSI. The PWM control signals for the VSI are generated using dSPACE 1104 control board. The control signals are generated with a switching frequency of 1 kHz.



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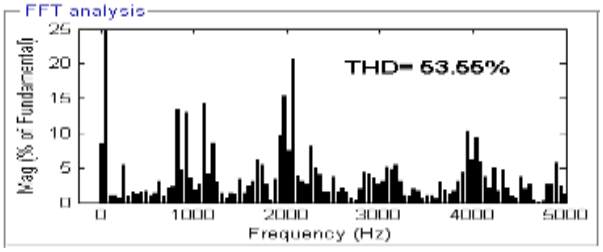

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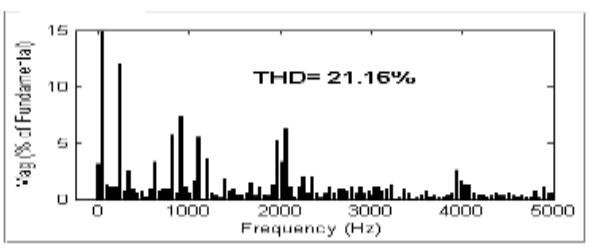

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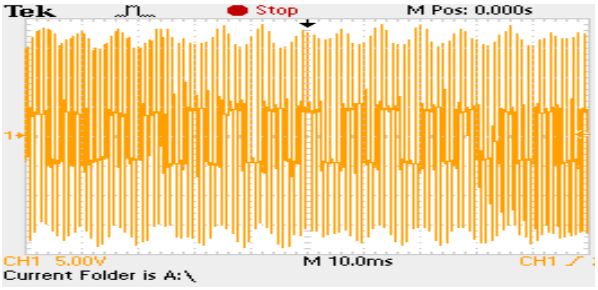
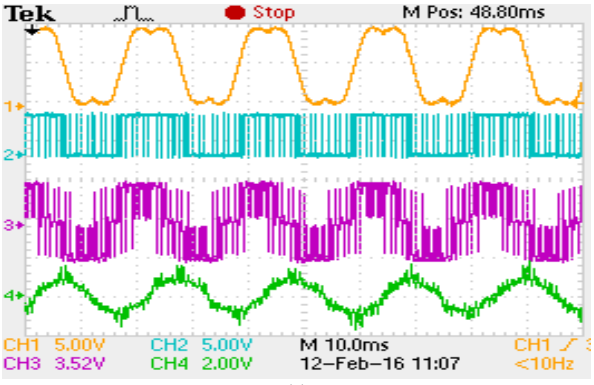


(d)

Fig. 4 Results of v/f controlled VSI fed induction motor drive with SVPWM (a) Modulating signal, pulse pattern, Line Voltage and Line Current (b) Harmonic spectrum of Line Voltage (c) Harmonic spectrum of Line Current (d) Common Mode Voltage at M=0.86



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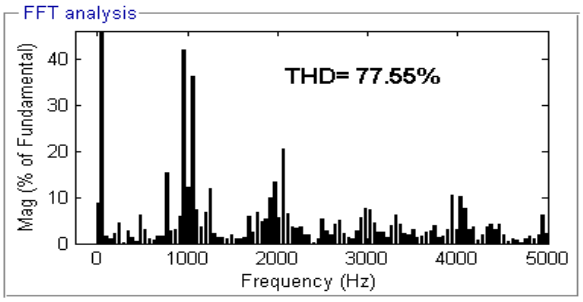

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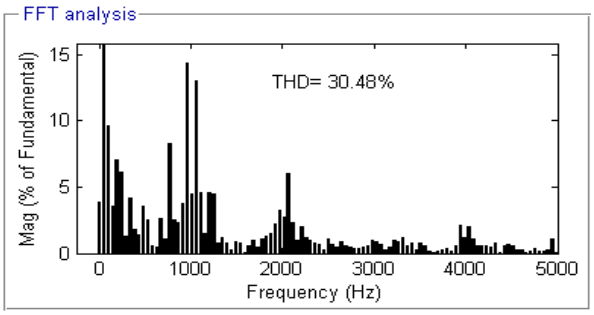

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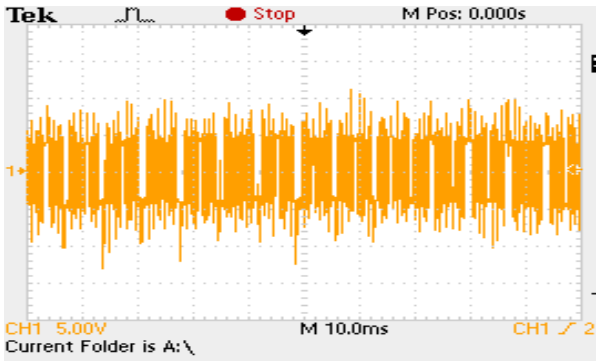
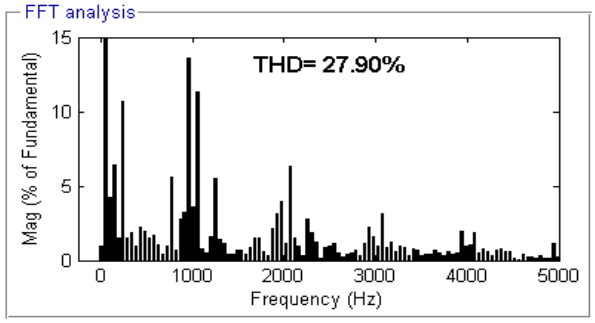


(d)

Fig. 5 Results of v/f controlled VSI fed induction motor drive with AZSPWM1 (a) Modulating signal, pulse pattern, Line Voltage and Line Current (b) Harmonic spectrum of Line Voltage (c) Harmonic spectrum of Line Current (d) Common Mode Voltage at M=0.86



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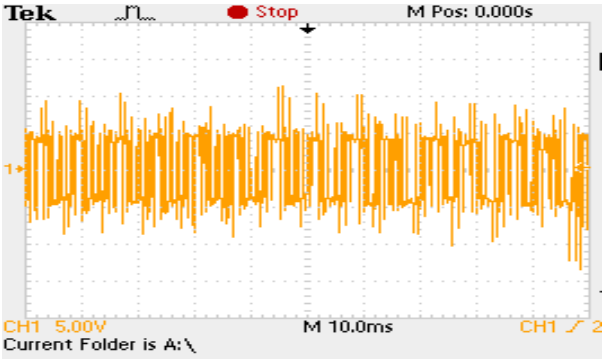
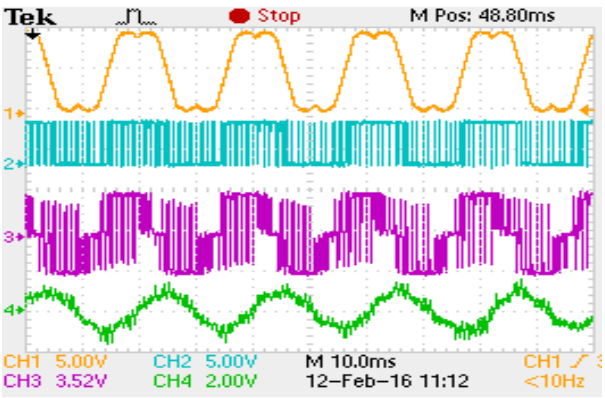
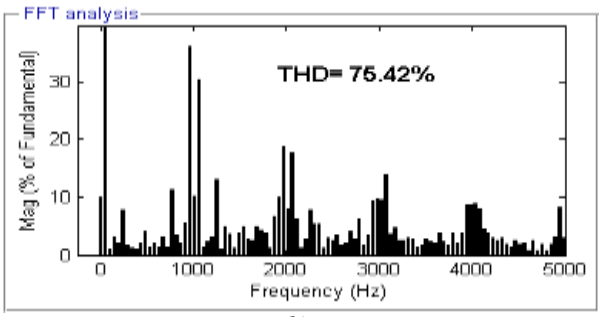


(d)

Fig. 6 Results of v/f controlled VSI fed induction motor drive with AZSPWM2 (a) Modulating signal, pulse pattern, Line Voltage and Line Current (b) Harmonic spectrum of Line Voltage (c) Harmonic spectrum of Line Current (d) Common Mode Voltage at M=0.86



(a)



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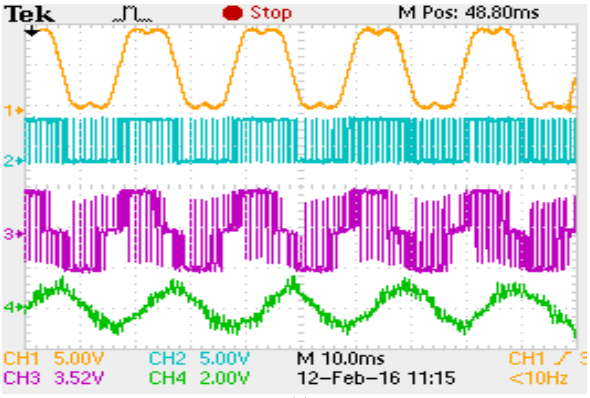

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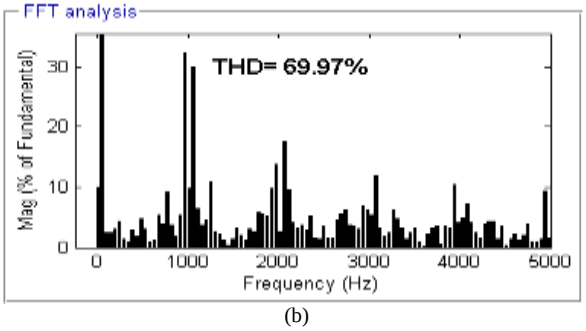

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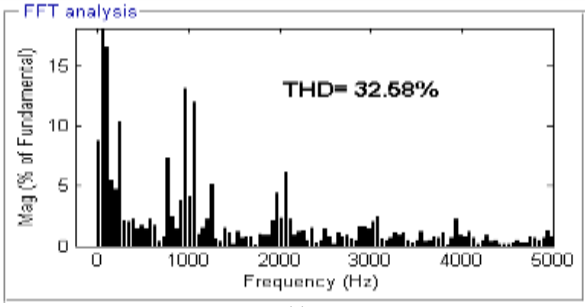

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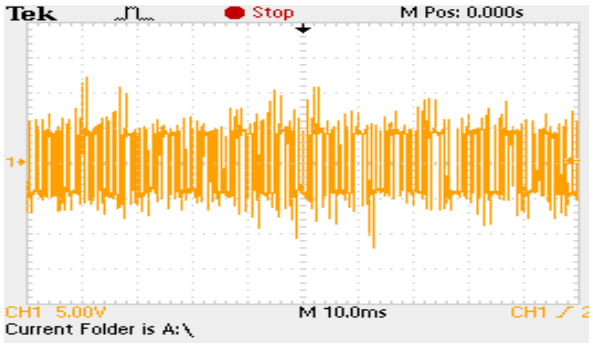

(d)

Fig. 7 Results of v/f controlled VSI fed induction motor drive with AZSPWM3 (a) Modulating signal, pulse pattern, Line Voltage and Line Current (b) Harmonic spectrum of Line Voltage (c) Harmonic spectrum of Line Current (d) Common Mode Voltage at M=0.86

The results of various continuous modulating signal based PWM algorithms for v/f controlled VSI fed induction motor drive are shown in Fig. 4 to Fig. 7. The obtained pulse pattern, line voltage and line current with SVPWM algorithm are shown in Fig. 4(a). The line voltage plot is having three-different levels V_{dc}, 0, $-V_{dc}$ but voltage levels are uni-polar (i.e No opposite negative voltage levels). The harmonic spectrum of line voltage and line current are shown in Fig. 4(b) and Fig. 4(c). As the switching frequency is maintained at 1 kHz, it is observed in harmonic spectrum that much of energy is concentrated at and around harmonics of switching frequencies.

The generated CMV with SVPWM algorithm is having a magnitude of $V_{dc}/2$ and $-V_{dc}/2$ as shown in Fig. 4(d). The obtained pulse pattern, line voltage and line current with AZSPWM1 algorithm are shown in Fig. 5(a). It is observed that line voltage in the plots of SVPWM and AZSPWM1 has same three different levels ($-V_{dc}$, 0, V_{dc}), but with AZSPWM1, the voltage levels are bi-polar.

Hence the total harmonic distortion of line voltage and line current is high with AZSPWM1 when compared with SVPWM. It is observed that, with such type of control signals (multicarrier based PWM algorithm), common mode voltage is decreased to magnitude of $V_{dc}/6$ and $-V_{dc}/6$. Similar to that of AZSPWM1, AZSPWM2, and AZSPWM3 also have bipolar voltage levels hence that total harmonic distortion with these algorithms (AZSPWM1, AZSPWM2 and AZSPWM3) is high (as shown in Fig. 5(b), (c), Fig. 6(b), (c), Fig. 7(b), (c)) when compared with SVPWM.

With CMV reduction PWM techniques like AZSPWM1, AZSPWM2 and AZSPWM3, the CMV is reduced to a magnitude of $V_{dc}/6$ to $-V_{dc}/6$ as shown in Fig. 5(d) to Fig.7(d). As the CMV reduction PWM techniques use multi carrier signals to generate control signals, they produce bipolar voltage levels (negative voltage levels) in the line voltage wave form as of Fig. 5(a) to Fig. 7(a). Hence, SVPWM algorithm shows superior performance in ripple reduction but produces high common mode voltage.

4. Conclusion

The complexity involved in the conventional space vector approach is high because of sector and angle calculation. To reduce the complexity, a novel approach has been presented, by using the notion of imaginary switching times. Convention SVPWM algorithm produces high common mode voltage which has adverse effect on bearings. In this paper simple CMV reduction PWM techniques are presented based on imaginary switching times. From the results, it can be concluded that AZSPWM1, AZSPWM2 and AZSPWM3 have superior performance in terms of common mode voltage reduction but produces high harmonic distortion.

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