FUZZY LOGIC CONTROLLED MODIFIED THREE PHASE MLI FED FROM SINGLE DC SOURCE FOR PV APPLICATIONS

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Abstract: *This paper presents simulation and validation of Fuzzy Logic (FL) controlled modified three phase Multilevel Inverters (MLI) fed from the single DC source for Photovoltaic (PV) applications. In this proposed inverter, gating pluses to the inverter is generated with the help of Space Vector Pulse Width Modulation (SVPWM) control technique. This control technique is implemented in the Field Programmable Gate Array (FPGA) development board. The main aim is to design a FL controller for grid connected applications and to achieve improved output waveforms,* minimum, low Total Harmonics Distortion (THD) values, *quick response and high robustness. Finally, the THD comparison made between PI and FL controller for validation of the proposed system and thus FL Controlled three phase MLI inverter is significantly improved the performances than PI controller. The proposed three phase inverter is verified through using MATLAB Simulink environment and In order to evaluate, the simulated results a laboratory prototype is built. The simulation &experimental results match very closely.*

Key words: *Modified Three phase MLI inverter, FLC, Single DC source, SVPWM, THD, FPGA.*

1.INTRODUCTION

One of the modern ways of generating electricity is using renewable energy sources. Renewable energy sources have drawn lots of attention of engineers, researchers, industries and governments in last one decade. Among the various types of renewable energy sources, solar PV based power generation is very attractive because of solar PV has abundant energy presence in nature Eco friendly qualities and low maintenances [1]. In the solar PV power generation, sunlight is directly converted into electrical energy [2]. Usually solar PV arrays are commonly used to convert solar energy into electrical energy. During the conversion process, the obtaining of maximum power from PV array is very essential. To obtain maximum power from the PV arrays, Perturb and Observe (P&O) based maximum power point tracking algorithm (MPPT) is used [3]. Generally, a single phase system may be suitable for power level up to 10kW. Beyond the 10kW power level, a three phase inverter has been designed for converting DC power into AC power with minimum THD and less filtering requirements [4]. To meet the above problems, three phase MLI's based solar PV inverter is the right choice and also suitable for high power applications. Besides MLI offers quality output voltage, low EMI, minimum switching losses compared to a conventional inverter [5-6]. MLI's are classified into three remarkable topologies, they are diode clamped MLI's, Capacitor clamped MLI and cascaded H-Bridge inverter [7]. In recent years, cascaded H bridge multilevel inverters have been widely used in high voltage and high power applications with separate DC sources as presented in [8]. Three phase cascade MLI's make use of single phase and three phase transformers with single DC source is presented [9-10]. In accordance with the observation from the references [8-10], inverter topology have need of additional number of DC sources, switches and transformers which results in increased volume, costly and complex control. The performances of power converter is mainly depends on the current controller used in the converter. In numerous investigations, the AC side grid currents are effectively by use of proportional-integral (PI) controller. However, in many nonlinear control applications, the conventional PI controller is inappropriate because of large peak overshoot, complex mathematical modeling required to find its parameters. In such control applications, intelligent controllers are used as a current controller. Among the

various intelligent control techniques, FL based controller is famous control techniques for controlling of inverter [11-12]. The three phase MLI inverter is effectively controlled by the FL controller to prevail the problems of conventional PI controller and also implemented using the FPGA based prototype model. In this research, simulation and validation of FL controlled three phase MLI fed from the single DC source for PV applications using FPGA is proposed. Minimum THD, flexibility of design, it uses only 16 (including boost converter) switches for generation (Five level) of three phase power using three phase 12 terminal transformer are remarkable advantages of the proposed system and switching losses of the proposed system is considered. Finally THD comparison made between two controllers (Say PI and FL controller).

2.PV System design

2.1 PV array Modeling

The Fig. 1 represents an equivalent circuit of a single diode of PV cell. Current sources, diode, and series (R_s) and shunt resistance (R_{sh}) are integrated in the equivalent circuits. The output voltage and current of the PV cell is generally based on the parameters such as irradiation level, temperature, number of cells, short circuit current (I_{sc}), etc. The relations of voltage and current of the single diode model array can be given as

$$I = I_L - I_0 \left(exp \left[\left(\frac{q}{\gamma k T_c} \right) x (V + I R_s) \right] \right) \qquad (1)$$

Where, I_L - Photon current, I_0 - Reverse saturation current, q - Charge of electron (1.6 x10^{-19}C), k - Boltzmann constant, T_c- Cell temperature in °C.
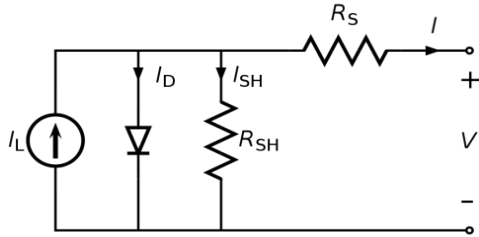

Fig.1. Equivalent circuit of the PV cell

The output of the parameter of the PV arrays such as voltage and current is measured and then given to the P&O based MPPT algorithm for computation process. The comparator compares the carrier signal with the output of the P&O based MPPT. The output of the comparator is given as an input pulse to the MOSFET switch (S_1). The Fig. 2 shows the PV voltage verses PV current maximum PV current attain at 1000 W/m^2. The Fig. 3 depicts PV voltage verses PV power, rated power of PV arrays depends on the irradiance fall on the PV cell. From the Fig. 3 clearly observed that maximum power achieves at 1000w/m^2 and lower power at 200W/m^2.
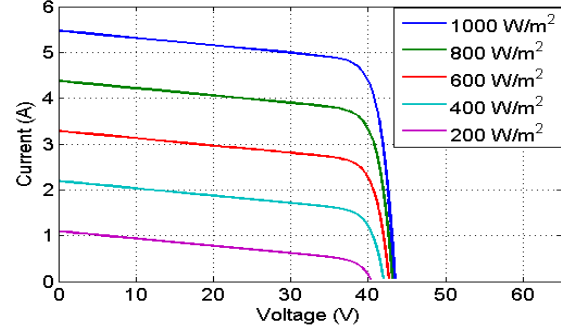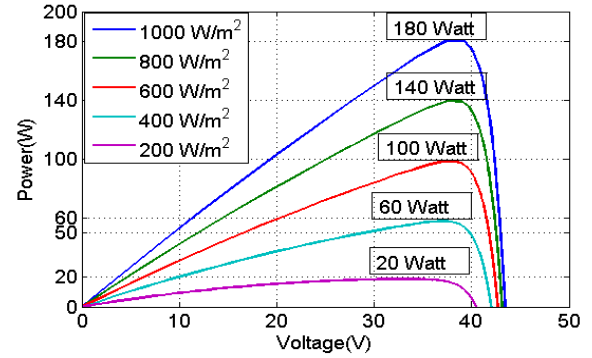

Fig. 2. voltage vs current (PV)

Fig. 3. PV voltage vs power (PV)

2.2 Modeling of Boost Converter

The proposed topology uses the PV tied boost converter. The output voltage of the PV arrays is not enough for driving the many applications. In order to increase the voltage level, the boost converter is used in the front. This is achieved by varying the duty ratio of a switch. The boost converter embraces a smoothing inductor, MOSFET switches and the DC bus. The DC bus formed by connecting the two capacitors in series and has equal values. (C_1, C_2). The duty ratio of the boost converter is based on the following equation [13].

$$D = 1 - \frac{183.6}{330}, D = 0.44 \qquad (2)$$

Equation (2), gives the duty ratio of the boost converter and it is not fixed.

2.3 Inductor Design

The inductor value used in the boost converter is given by:

$$L = \frac{V_i * (V_0 - V_i)}{(\Delta i_L) * f_{SW} * V_0}$$

$$L = \frac{183.6 * (330 - 183.6)}{0.263 * 5000 * 330}$$

$$L= 62.0\text{mH} \qquad (3)$$

2.4 Capacitor Design

The capacitor value used in the DC bus is given by:

$$C = \frac{I_{0(max)}*(D)}{(\Delta V_0)*f_{SW}}$$

$$C = \frac{4.98*0.44}{5000*9.9}$$

$$C = 44.24\mu F, \ (C1=C2= 88.48 \ \mu F) \quad (4)$$

Where;

V_i- Input voltage of the boost converter; V_a-Inverter output voltage; f_{SW}-Switching frequency of the boost converter (5000Hz); Δi_l - Ripple current of the inductor; ΔV_a - Ripple voltage of the capacitor; I_a- Maximum current.

3. Three phase inverter configurations

In this section, mainly deal with various inverter configurations. The classification inverter mainly based on power switches, transformer, input DC sources. Three phase MLI inverter with individual DC source [14] (Topology 1) is shown in Fig. 4. This topology requires an independent PV array for each H-Bridge and each of PV arrays are controlled by an individual MPPT control. This type of topologies has many advantages such as faulty inverter can be replaced by easily; highly suitable for medium and high power applications. However, these types of inverter individual DC sources are needed, extra switch counts are required for higher levels, costlier and reliability of the system is also reduced. For five levels three phase inverter requires 30switches, 6 inputs DC sources. Furthermore, this type of topology, easily reconstructed with unequal DC sources. The merit of this topology is the output voltage level of the inverter increased without increasing the number of levels. But same time controlling charterers of the inverter is very difficult and an application of this type of inverter is too limited [15]. The Fig. 5 shows cascaded type three phase five level inverter with single DC source employing single phase transformer. Each single phase transformer is connected at the output terminals of the H bridge inverter. Similarly, all the transformers are connected in series to form a three phase inverter. This inverter offered well quality of output waveforms and highly suitable for grid connected operation. Observe from the above Fig., this type of topology use only one DC source compared previous topology, but same more numbers single phase transformer are required for higher voltage level. 25 switches, 6 single phase transformers are required for this structure. Three phase cascaded inverter using single DC source employing three Phase transformers is shown in Fig. 6. This topology has single DC source and many three phase transformers are used [16]. This topology is highly suitable for grid connected application because of property of transformer connections at secondary terminals. However, system size, number of switches will be somewhat increased. 25 switches, 3 three phase transformers are needed for this structure. All drawbacks of existing topologies are overcome by the proposed inverter.
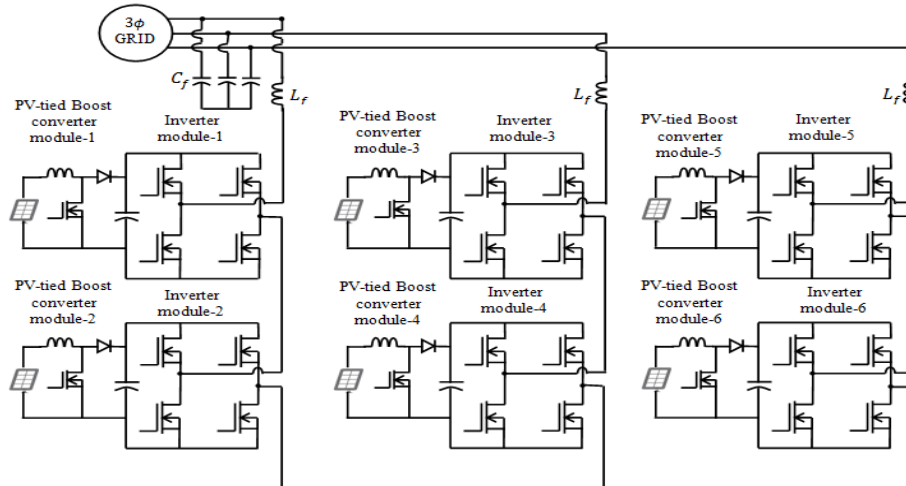

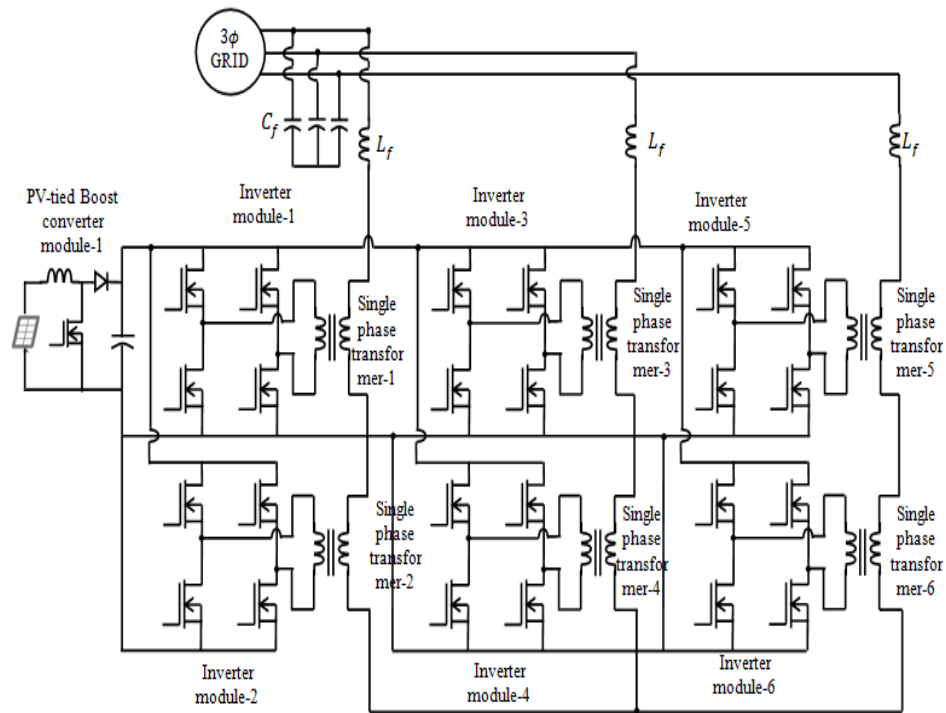Fig. 4. Cascaded three phase MLI inverter with individual DC source (Topology 1)

Fig. 5. Three phase cascaded inverter using a single DC source with single Phase transformers (Topology 2)
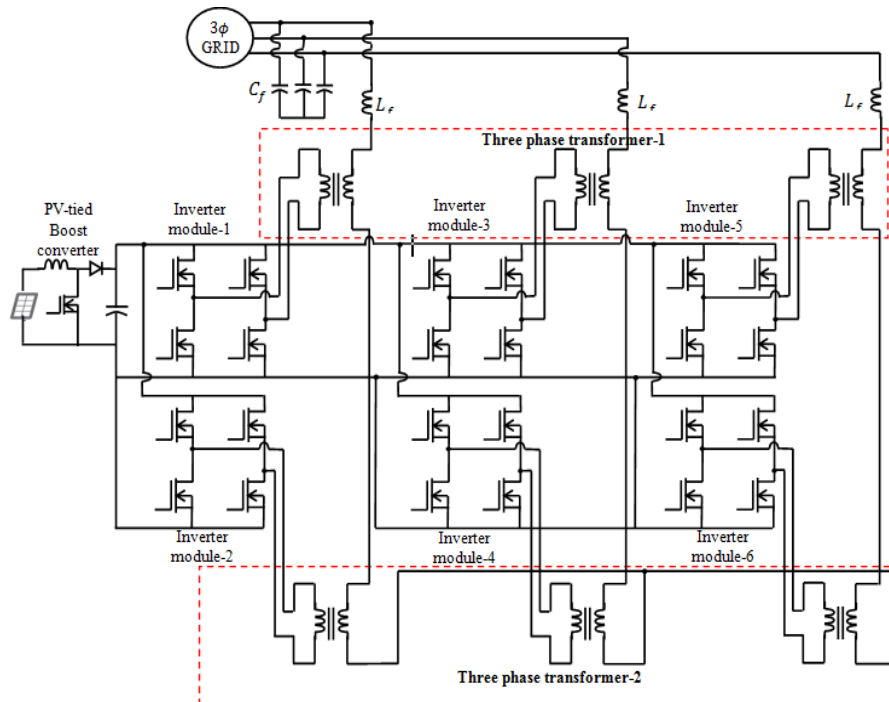

Fig. 6. Three phase cascaded inverter using a single DC source with three Phase transformers (Topology 3)

3.1 Proposed Modified Three Phase Inverter

In this inverter topology, three phase inverter is modified by connecting three single phase inverter in parallel and it's fed with common DC bus. The three phases such as phase A, phase B, and phase C as shown in Fig. 7. All the single phase inverters have five power semiconductor devices and four power diodes. The power switches M1a, M2a, M3a, M4a form H-Bridge inverters and M5a with four power diodes form the full bridge inverter [17]. The power switches M1a, M2a and M5a operated at higher frequencies and M3a, M4a operate at fundamental frequencies (i.e. 50Hz). The output of the PV panels is given to the boost converter. The boost converter consists of an inductor, high speed MOSFET and diodes. The designs of an inductor and the DC bus capacitor play an important role here and 5000 Hz frequency is chosen for designing the inductor, in which the volume of the inductor can be reduced. Furthermore, interference can be minimized through the selection of higher frequency ranges. The DC bus consists of two capacitors with equal rating. The values of the inductor and the capacitor are denoted in the equation (3) and (4) respectively. The DC bus voltage should be higher than the output voltage of the inverter. This DC bus voltage is shared by all the five level inverters and, five level output voltage at the inverter output terminals is realized. Each single phase inverter is capable of generating five level output voltages V_a, $V_a/2$, 0 , $-V_a/2$, $-Va$. The H-bridge inverter is capable of producing Va and $-Va$ and auxiliary circuit can generate $V_a/2$ and $-V_a/2$. The phase and neutral outputs of each inverter are given to the primary terminals of the transformer. Similarly, phase B and phase C are connected to the respective primary terminals of the transformer. All the neutral points of the transformer are shorted and it is connected to three phase LC filter [18]. For the proper inverter operation, space vector pulse width modulation technique is used to generate the PWM signal to the inverter. The space vector control algorithm is implemented (VHDL Programming) in the FPGA board. The injected current and voltage must be a pure sinusoidal waveform with permissible THD. So, there is a need to connect LC filter at the output of the transformers. The filtered sinusoidal output from the inverter power is injected into the grid.
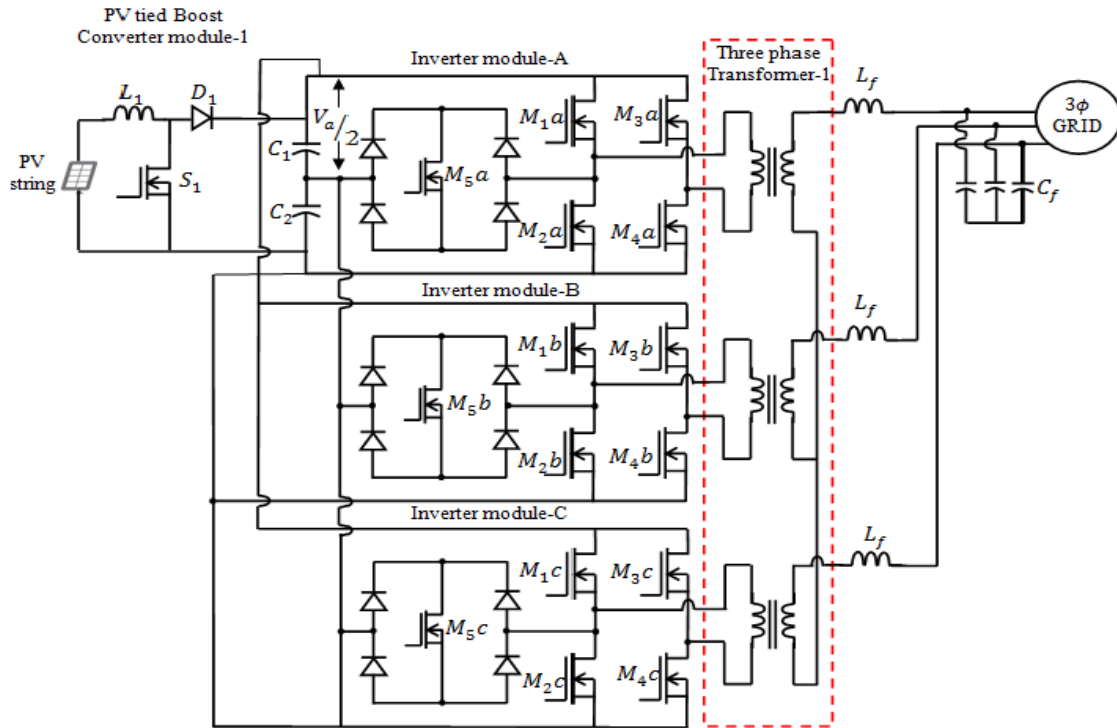

Fig. 7. Proposed Fuzzy Logic Controlled (FLC) three phase MLI inverter using single DC source with 12 terminals transformer

4. Control system design

The control system design plays a vital role in the PV inverter. The control system consists a Phase lock loop (PLL), d-q reference frame, an inverse d-q reference frame and a controller. The purpose of the PLL is that, it synchronizes the output frequency and phase angle of the grid voltage with grid current. Use of the abc to d-q frame, which converts three variable quantities (i.e: three phase current and voltage) into two variable quantities (i.e: d-q values). These values are processed by fuzzy controller. The outputs of fuzzy controller are fed to the inverse park transformation (dq-abc). The inverse park transformation generates the reference signal, which is compared with carrier signal and generates switching sequence for the inverter.

4.1 Fuzzy logic controller

A FLC can be defined as the nonlinear mapping of an input data set to a scalar output data A FLC consists of four major parts that is fuzzifier, rules, inference engine and defuzzifier. The performance of the conventional controller is not satisfactory in controlling various nonlinear control applications. Moreover the design of its control system is also very complex. The newly designed FLC is devoid of these drawbacks [19]. FLC has simple and effective input and output membership functions. Fig. 8 shows the architecture of fuzzy logic controller.
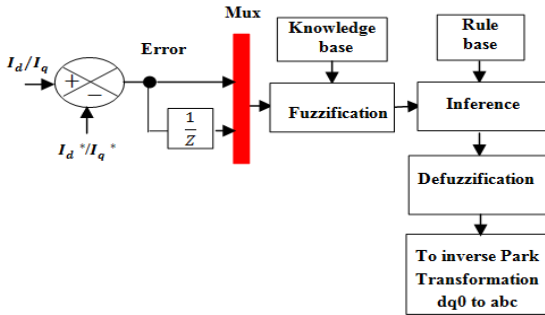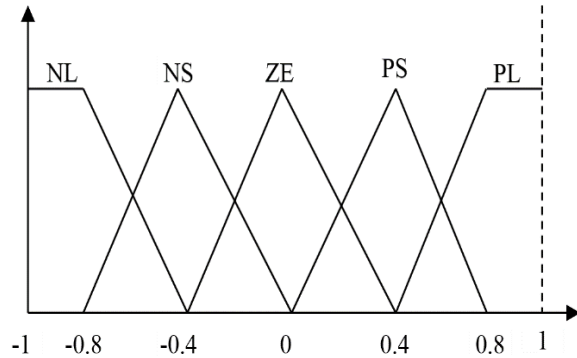

Fig. 8. Fuzzy controllers Architecture
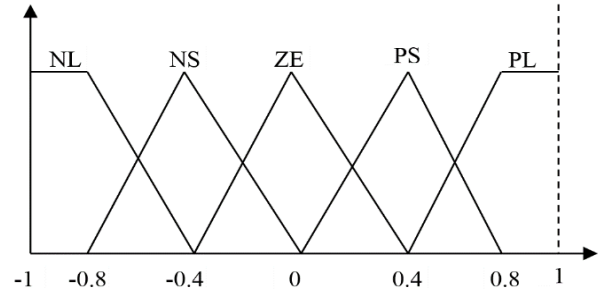

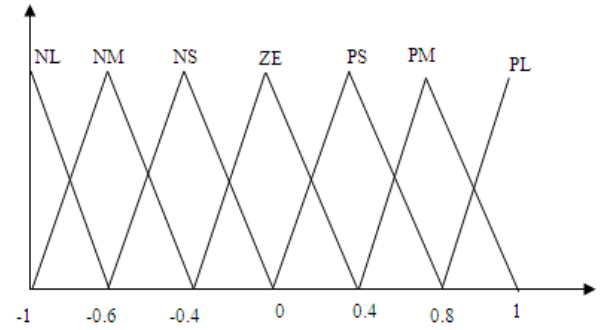Fig. 9. Change in error (de)

Fig. 10. Change in error (de)

Fig. 11. Output of fuzzy controller

Table 1
Fuzzy rules

De d	NL	NS	Z	PS	PL
NL	NL	NL	NM	NS	Z
NS	NL	NM	NS	Z	PS
Z	NM	NS	Z	PS	PM
PS	NS	Z	PS	PM	PL
PL	Z	PS	PM	PL	PL

The input response collected from the knowledge base is categorized as 'd' error and 'de' change in error at a specified time a single member function in error 'd' is compared with all the membership function in change in error 'de' in fuzzy logic controller and it is observed that time consumption in fuzzy logic is very less when compared with conventional controller. Fig. 9, 10 and 11 shows its membership functions of fuzzy logic controller. Table I shows the fuzzy rules of the proposed system. These fuzzy rules generated based on the error (d/de). From the Table 1 'd' represented as error and 'de' represented as change in error.

4.2 Principle space vector PWM

The current harmonics of the system are determined by the switching frequency and the PWM technique applied to the system. Due to some practical reasons, the switching cannot be increased certain degree and also increases switching losses.. So SVPWM techniques are very quite simple for real time execution [20]. In order to make three phase inverters effective Space Vector Pulse Width modulation is developed as a vector approach to pulse width modulation. It is well known that the pulse width modulated techniques is a popular approach for the reduction harmonic presented in inverter output terminal. But it has its own drawbacks as mentioned below [21];

(i). Effective elimination of third and fifth order harmonics may not be possible. (ii). Power loss would increase along the switches due to higher PWM. (iii) Electromagnetic interference in the results of higher order harmonic in the current. Having overcome these limitations of PWM approach, SVPWM techniques prove to be an effective solution to the issue. The basic switching sector and vectors are shown in Fig. 12. SVPWM algorithms are implemented using embedded MATAB function
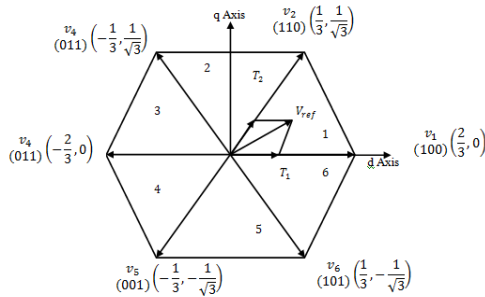

Fig. 12. Basic switching vectors and sector

The adjacent vectors in each sector of SVPWM need to be averaged. Two adjacent vectors and zero vectors are combined to generate the appropriate PWM signals. In order to generate PWM pulses to the inverter, two reference signals ref.1 and ref.2 signals are compared with carrier signal. The intersection point generates PWM pulses to the inverter. The values T_1, T_2 and T_0 are calculated as follows

$$T_1 = k \times \left(\sin\left(\frac{\pi}{3} - \theta + \frac{n-1}{3}\pi\right) \right)$$

$$T_2 = k \times \left(\sin\left(\theta - \frac{n-1}{3}\pi\right) \right)$$

$$T_0 = (T_z - (T_1 + T_2))$$

Where,
K is the modulation index and it can be defined as

$$k = \frac{\sqrt{3} \times T_z \times V_{ref}}{V_{dc}}$$

$T_z = \frac{1}{f_s}$; f_s = Switching frequency

5. Design of AC side LC filter

The current injected into the grid must be pure sinusoidal with permissible THD. The AC side filter is connected to the output of the transformer and removed harmonic content is presented at the output of the transformer. The values of L and C obtained from the following equations (11) and (12) are presented. While designing the AC side LC filter, generally ripple current is chosen from 10-15% of rated current. For the design, 10% &15% of rated current and power are respectively used in [22-23].

Filter inductance (H) is given by the equation:

$$L = \frac{1}{8} * \frac{V_0}{\Delta i_{lmu} * f_{SW}} \tag{11}$$

Where, Δi_{lmu} is the ripple current. This can be 10% of rated current.

Filter Capacitor in C is given by:

$$C = \frac{15\% \ P_{rated}}{3 * 2\pi f * V_{rated}^2} \tag{12}$$

Where,
V_{rated}^2 = 400V, P_{rated}= 1.08kW, f=50Hz

6. Results and Discussion
6.1 Simulation Results

The proposed FL controlled three phase MLI inverter with single DC source is built on MATLAB Simulink model. In the simulation, P&O MPPT algorithm is used to track the maximum available power from the PV array at different climatic conditions. Tata BP 180W solar array specifications are taken into account for simulation studies.
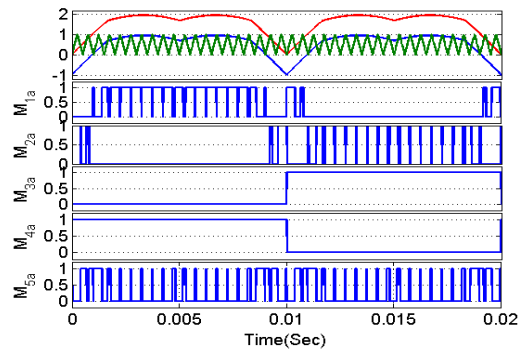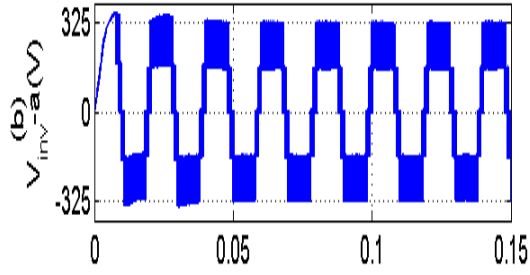

Fig. 13. Switching pulses (simulation)

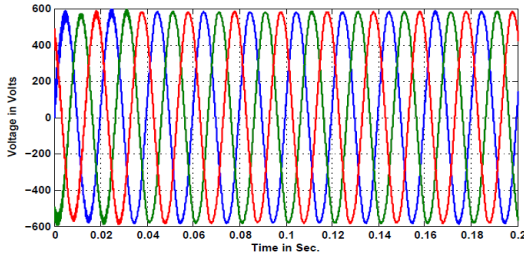Fig. 14. Five level output (one Phase)

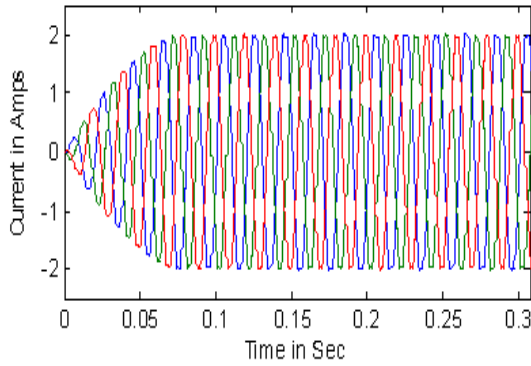Fig. 15. Three phase output voltage

Fig. 16. Three phase current

The Fig. 13 depicts switching pulse to inverter. From the observed that M3a and M4a are operated at fundamental frequencies and other switches are operated higher frequencies ranges. Five levels output voltage of the inverter is shown in Fig. 14. The filtered three phase voltage and current are shown in Fig.s 15 and 16 respectively.

6.2 Experimental results

The proposed FL controlled three phase solar PV inverter implemented using a Spartan FPGA board for validation of simulation results. In this experimental setup, six PV panels are used in the power rating of 180W. So, the total estimated power is 1080W (or) 1.08Kw. The DC bus voltage is approximately set to 330V and five level output voltage realized from the inverter. The output of the inverters is given to the 1:1 three phase 12 terminal transformers. Which is consisting of PV panels, boost converter, three phase inverter, 12 terminal transformers, three phase LC filter and followed by

three phase grid. Fig. 21 showing the experimental setup of the proposed system. In this experimental setup, the control algorithms are written in VHDL language on FPGA board. The Hall Effect current and voltage sensors are used to measure grid side parameters such as voltage and current (LV 25-P and LTS 25-NP). The output of the Hall Effect sensor is given to TL084 OP-Amp based signal conditioner and then the analog signal of the signal conditioner are given to the 6 channel Analog to Digital Converter (AD 8608). On the front end side PV panel voltage and current are measured by sensors and given to the TL084 Op-Amp based signal conditioner. This is transferred to the 6 channel Analog to Digital Converter (AD 8608). The experimental setup consists of buffer, driver and isolation circuits. The purpose buffer circuits are used to match the impedance between input and output lines and optical isolator circuits are used to isolate the low voltage side and high voltage side. The PWM pulses are generated using TLP 250 IC based driver circuits and then fed to the power switches. Switching pluses to the inverter are represented in the Fig.s 17, 18 and 19.
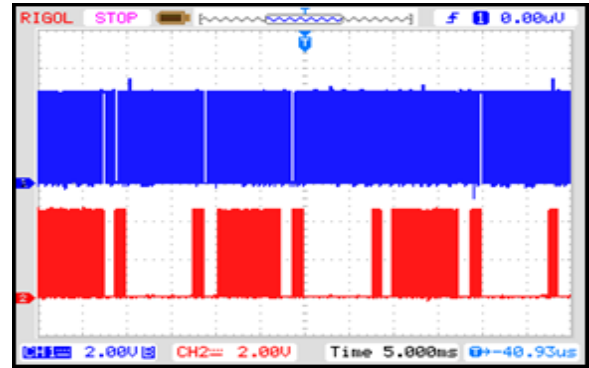

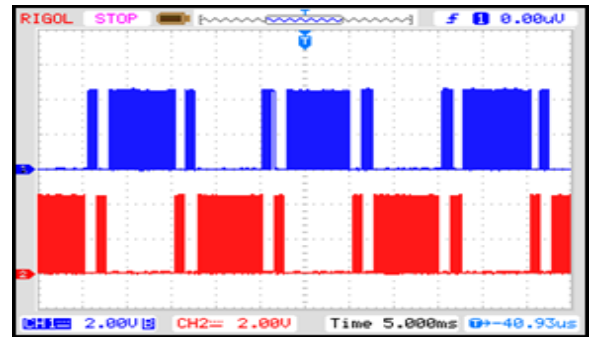Fig.17. Switching pulses for M5a (Upper)
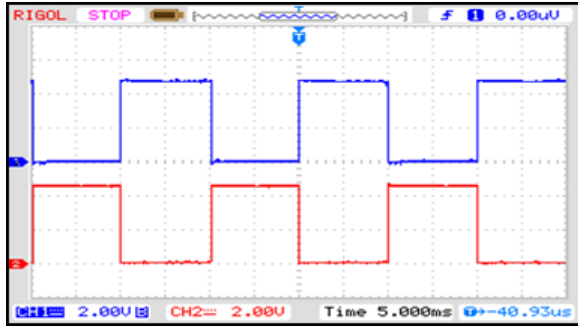

Fig. 18. switching pulses for M1a and M2b

Fig. 20 shows simulated waveform using VHDL coding. Fig. 22 and 23 depict five level voltages each phase (upper screen) with inverter current (lower one) and filtered three phase voltage respectively. From the Fig. 24 it is observed that both voltage and current are in phase, which ensures the system operates near unity power factor. All the waveforms recorded with the help of the YOKOGAWA power analyzer.

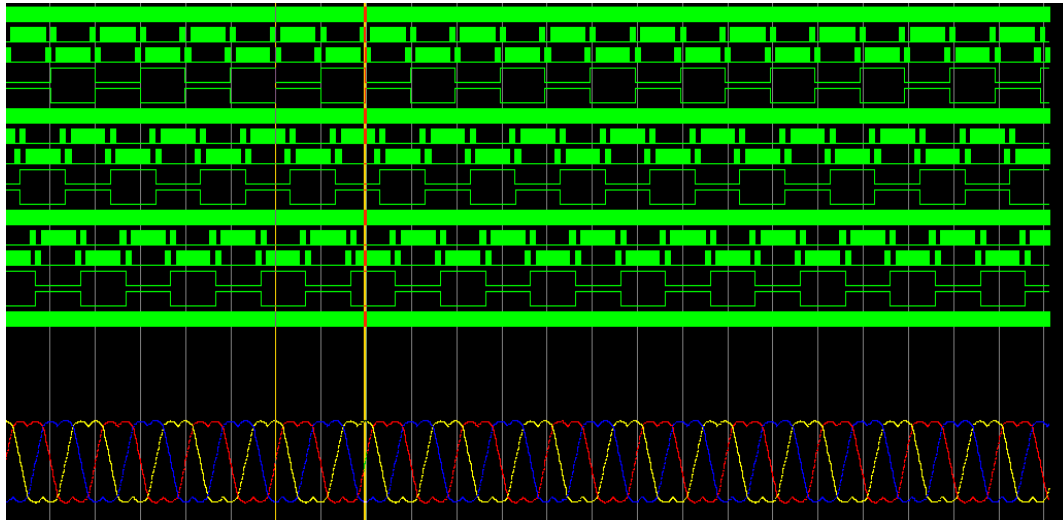Fig.19. switching pulses for M3a and M4a

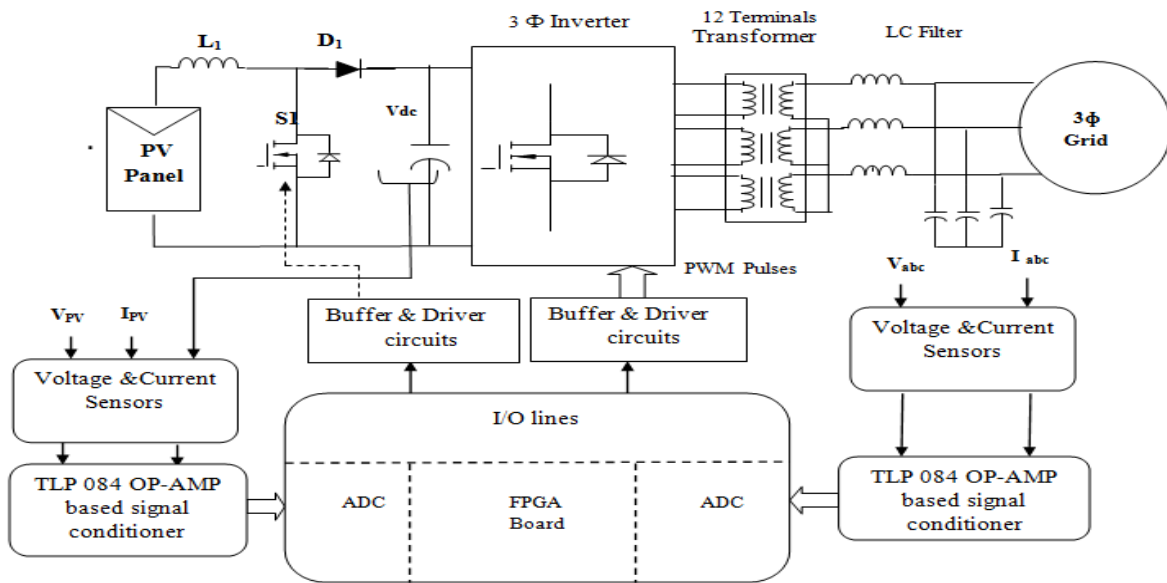Fig. 20. simulated wave form using VHDL coding

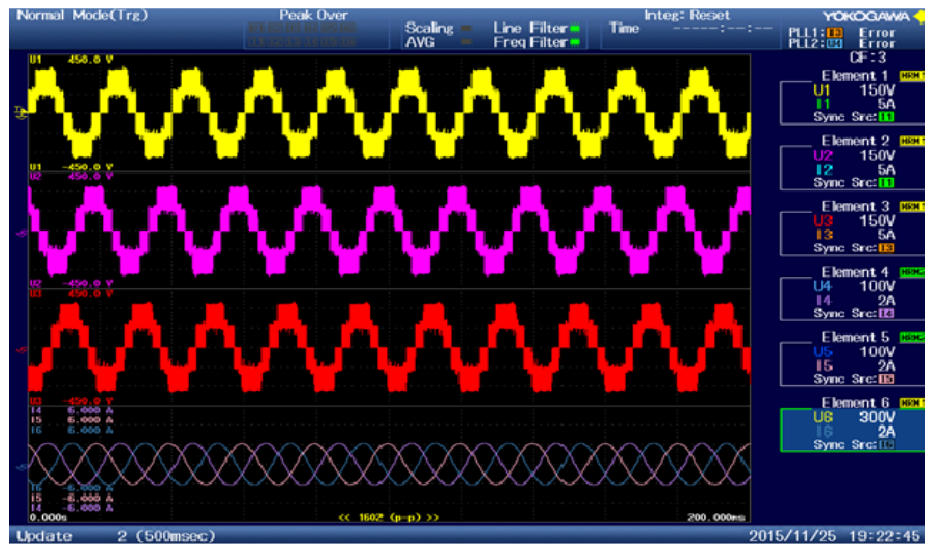Fig. 21. Experimental setup of the proposed system

Fig. 22. Five level inverter output (Upper Three Screen) and Three phase current (Lower Screen)
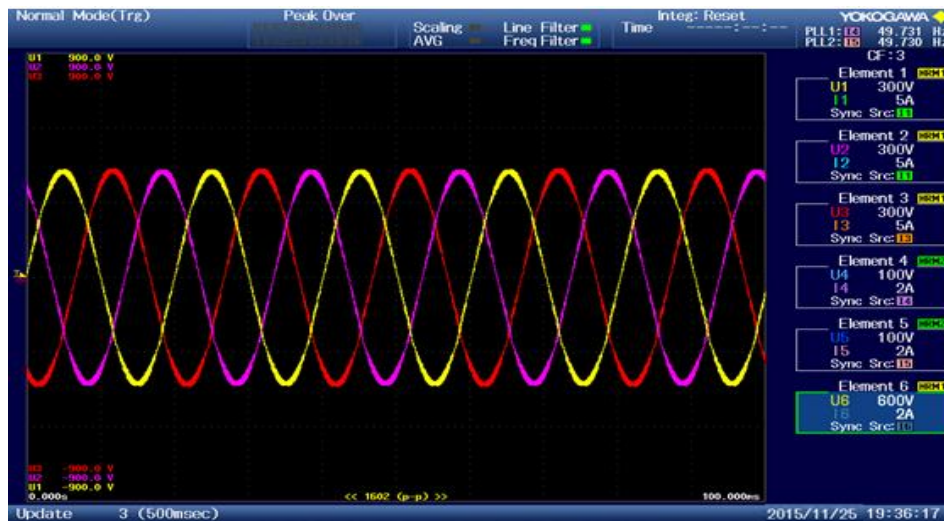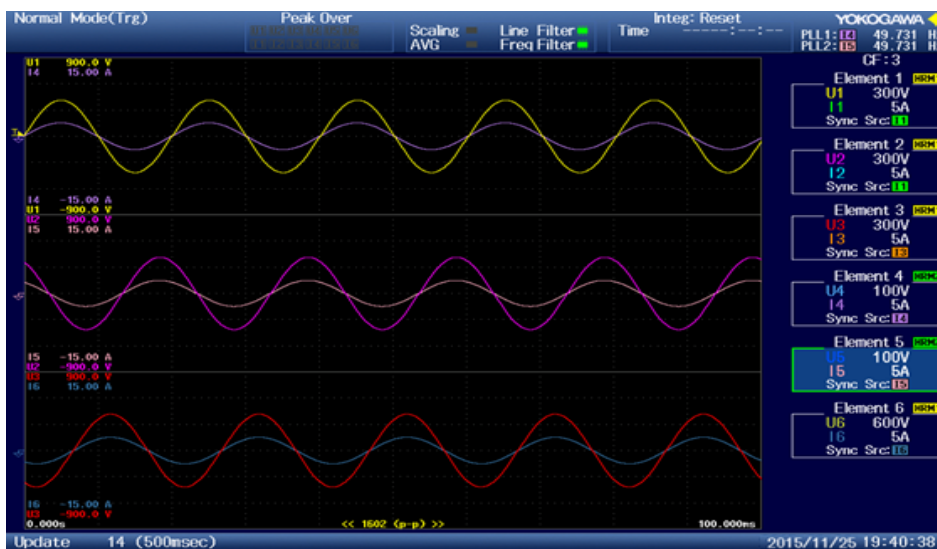

Fig. 23 Three phase voltage (Experimental)

Fig. 24 Grid voltage and inverter current

6.3 Comparative Study

The comparative study mainly focused on utilization of devices and components is used in the proposed topology compared to exiting topologies. This comparison, primarily based number of switches, transformers, DC sources and DC bus capacitors. The proposed topology uses only 16 switches, one transformer, only one DC source, 2 DC bus capacitors. So, totally 20 numbers of devices and components are used. From the Table 2, clearly observed the proposed topology uses lesser device utilization compared to others. The components and devices are used in the fabrication prototype is tabulated in the Table 3 and photocopy of the same is shown in figure 25.

Table 2

Device and components comparison of proposed topology

Configuration	Number of Power Devices					Size
	S_W	T	DC sources	C	Total	
Topology 1	30	-		6	36	Large
Topology 2	25	6*	6	1	38	Medium
Topology 3	25	2**	1	1	29	Medium
Proposed Topology	16	1**	1	2	20	Compact

NOTE: Including front end boost converter power devices; Excluding grid side filter devices.
* represents single phase transformers, ** represents three phase transformers,
Sw- Switches, T- Transformers, C- DC bus capacitors

Table 3
THD profile

% of THD (PI-Experimental)	% of THD (FLC-Experimental)
1.7%	1.4%

Fig. 25 Photograph of experimental setup

7. Conclusion

Simulation and validation FLC three phase MLI inverter fed from the single DC source for PV applications is presented in this paper. The P&O based MPPT algorithm is used for tracking maximum power from the PV panel. The SVPWM switching algorithm is written using VHDL implemented in FPGA and generates gating suitable gating pulses to the inverter. Current harmonics of the system are effectively minimized through SVPWM technique with the utilization of fuzzy logic controllers. Thus the THD performances of the proposed inverter are significantly improved compared to conventional PI controller. Advantages of the proposed reduced number of switches, transformers and input DC sources. The simulations study carry out on a five-level inverter based on the proposed configuration have been validated experimentally.

Acknowledgement

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