CURRENT SHARING IN PARALLELED CONNECTED LUO CONVERTERS FOR STANDALONE PHOTOVOLTAIC SYSTEM

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Abstract: *This paper proposes a new current sharing scheme for solar integrated parallel connected positive super lift LUO converters (PSLLCs). The proposed current sharing scheme consists of two loops, an outer voltage loop and an inner current loop. The outer voltage loop ensures voltage regulation using fuzzy pre-compensated PID controller. An inner current loop ensures equal sharing of load current between parallel connected converter modules. For ensuring equal sharing of load current no dedicated current sharing controller is used. Instead by sensing power input voltage, output voltage and inductor currents of parallel connected converter modules, inner current loop ensures equal sharing of load current. Since parallel connected converters are designed for renewable energy systems, the input current is used as a control parameter. PID controllers and fuzzy pre- compensated PID controllers are designed for voltage regulation and compared through MATLAB based simulation and fuzzy pre-compensated PID controllers are found to be satisfactory. The proposed current sharing scheme is implemented using PIC16F877A and the results are presented*

Key words: *Closed loop systems, current sharing, dc-dc power converters, Photovoltaic cells*

1. Introduction

Renewable energy generation using solar photovoltaic system reduces energy utilisation obtained by oil and gas. In general solar energy from sun in one hour satisfies the energy requirement of human population in one year [1].

Many research works have mentioned the growth of solar power system in recent years. Standalone photovoltaic system supply load directly without connecting to the utility system. Such systems have simple configuration and control scheme [2-3]. More number of solar arrays in series or parallel satisfies the energy requirement of domestic, industrial applications etc [4-5].

Maximum power obtained from solar panel is delivered to load through dc-dc converters [6]. Than using a single high power dc-dc converter, two or more low power parallel connected dc-dc converters helps to increase power ratings and enhance reliability of the system. [7-8].

Hence this paper proposes solar input parallel connected PSLLCs for generation of higher output current. Due to component tolerances, unequal sharing of load current takes place between two parallel connected converters. For ensuring equal sharing of load current, many current sharing schemes have been proposed.

Current sharing takes place in [9] by vector representation of converter currents. Virtual impedance current sharing takes place in [10]. Modification of converter output voltage is required in [11] & [12] for current sharing. Primary droop current sharing method is presented in [13] which results in poor voltage regulation. Current sharing was implemented in [14] by sensing the input currents, but a dedicated current sharing controller was used. Steady state solution of parallel connected converters with master slave current sharing was derived in [15]. The drawback associated with this method is if one converter fails, entire system does not work. Active current sharing methods use feedback control [16] which increases circuit complexity. Common duty ratio method of current sharing gives perfect current

sharing only in presence of less parameter mismatches. No perfect current sharing takes place if parameter mismatches are more [17].

This paper proposes equal sharing of load current in paralleled connected PSLLCs for standalone photovoltaic system. In the proposed control scheme there are two loops. One loop regulates the output voltage using fuzzy pre-compensated PID controller. It is referred to as voltage loop. The control signal from voltage loop is acting as a reference for current loop.

The current loop doesn't have any dedicated controller. Instead current loop adjusts duty ratio of converter modules, which depends on converter inductor currents, capacitor voltages and power input voltage of parallel connected PSLLCs. This method gives perfect current sharing even if circuit parameters of converters connected in parallel are different.

In the following, PV cell characteristics are presented, the block diagram and control scheme are described, Luo converter operation and its mathematical model is given and the design of fuzzy pre-compensated PID controller are presented. The design of controllers is then verified by simulation and the proposed control scheme is implemented in real time.

2. Modeling of PV cell

Based on photovoltaic effect principle PV cell converts solar radiation into the dc current. The important characteristics of a solar cell are described by the voltage-current and power-voltage characteristics. The equivalent circuit of PV cell consists of photo current, a diode, a resistor connected in parallel to express a leakage current and a resistor in series which describes an internal resistance for current flow, is shown in Fig.1. The voltage-current characteristic equation of a solar cell is expressed as follows:

$$I = I_{ph} - I_s\left(exp\frac{q(V+R_sI)}{NKT} - 1\right) - (\frac{V+R_sI}{R_{sh}}) \qquad (1)$$

Here, I_{ph} represents photocurrent, I_s indicates reverse saturation current of the diode, q mentions electron charge, V is the voltage drop across the diode, K and T *are* Boltzmann's constant and junction temperature respectively, ideality factor of the diode is denoted as N, R_s and R_{sh} are the series and shunt resistors of the cell, respectively. From above equation it is known that the PV,VI and IV characteristics of PV cell will be changed when solar illumination changes.

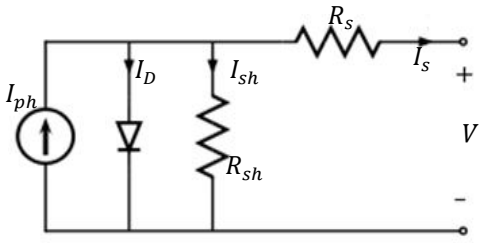


Fig. 1. Equivalent circuit of a PV Cell

In the present work PV array module (BPSX150s) is given as input to parallel connected PSLLCs.

2.1 Proposed MPPT Algorithm

Adaptive neuro fuzzy inference system (ANFIS) based constant voltage reference method is acting as maximum power point tracking controller (MPPT) controller. The output voltage (V_{solar}) from solar array is sensed and compared with the reference voltage (V_{ref}). The error difference between output voltage (V_{solar}) and reference voltage (V_{ref}) acts as an error signal. Based on error signal the maximum power point tracking controller (ANFIS) generates a control signal. This control signal adjusts the duty ratio of buck-boost converter for obtaining a regulated output voltage.

3. Circuit configuration and control scheme

3.1. Circuit Configuration

The block diagram of paralleled connected PSLLCs for standalone photovoltaic system is shown in Fig. 2. The maximum power obtained from solar panel is delivered to load through battery. Consider the signal from battery as v_g. It is applied to parallel connected PSLLCs. As a result current flowing through inductances are i_{L_1} andi_{L_2}.

The output current due to i_{L_1} and i_{L_2} isi_o. This output current i_o doesn't get shared equally, if there exists parameter mismatches between parallel connected converter modules. In order to share load current equally between parallel

connected converter modules with different circuit parameters a new control scheme is proposed.

3.2. Proposed Control Scheme

The proposed control scheme is shown in Fig. 3. It consists of two loops, an outer voltage loop and a current loop. The outer voltage loop generates a control signal ($\hat{\imath}_c$) which is the difference between reference signal ($\hat{v}_{ref}$) and the actual output voltage ($\hat{v}_o$).

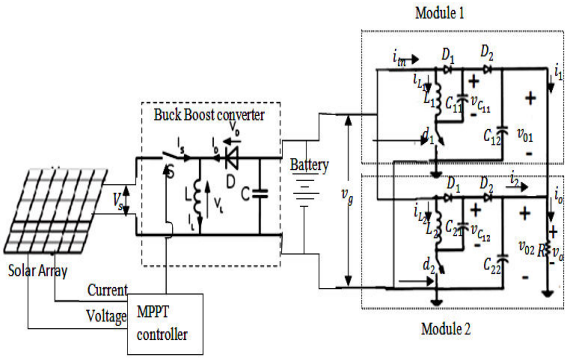


Fig. 2. Block diagram of paralleled connected PSLLCs

The difference between the control signal ($\hat{\imath}_c$) and sum of signals from input voltage with its gain($\widehat{H}_g$) , output voltage with gain ($\widehat{H}_v$) and input current ($\hat{\imath}_{L_1}$) adjust the duty ratio of PSLLC module1.

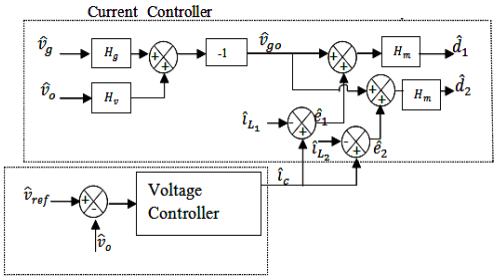


Fig. 3. Proposed Control scheme

Similarly difference between the control signal ($\hat{\imath}_c$) and sum of signals from input voltage with its gain($\widehat{H}_g$) , output voltage with gain ($\widehat{H}_v$) and input current ($\hat{\imath}_{L_2}$) adjust the duty ratio of PSLLC module 2. This ensures equal sharing of load current between paralleled connected converter modules in presence of parameter mismatches.

4. Small signal modeling of PSLLC

Positive Super Lift Luo Converter is shown in Fig .4[18]. It consists of an input supply voltage V_{in}, the capacitors C_1 and C_2, the inductor L_1, the power switch S, the freewheeling diodes D_1 and D_2 and the load resistance R.Assume that the PSLLC operates in Continuous conduction mode (CCM).There are two modes of operation for PSLLC. Under mode 1 the switch is closed and under mode 2 the switch is open.

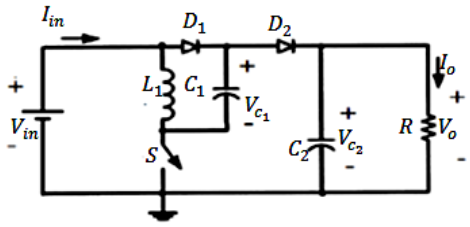


Fig. 4. Circuit of positive super lift Luo converter

The linearised equation for inductor from fig 4 is

$$L\frac{d\hat{\imath}(t)}{dt} = \hat{v}_g(t) + D'(\hat{v}_1(t) - \hat{v}_2(t)) - \hat{d}(t)(V_1 - V_2) \qquad (2)$$

Similarly the linearised capacitor equations are

$$C_1\frac{d\hat{v}_1(t)}{dt} = -D\hat{\imath}_{L_1}(t) - \hat{d}(t)I_{L_1} + \hat{\imath}_{in}(t) \qquad (3)$$

$$C_2\frac{d\hat{v}_2(t)}{dt} = -\frac{\hat{v}_o(t)}{R} - \hat{d}(t)I_o + D'\hat{\imath}_o(t) \qquad (4)$$

Finally the linearised equation of the average input current is

$$\hat{\imath}_g(t) = D\left(\hat{\imath}_{L_1}(t) + \hat{\imath}_{C_1}(t)\right) + \hat{d}(t)\left(I_{L_1} + I_{C_1} - I_{C_2} - I_o\right) + D'\left(\hat{\imath}_{C_2}(t) + \hat{\imath}_o(t)\right) \qquad (5)$$

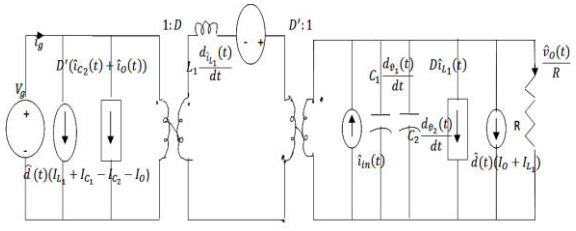


Fig. 5. Small signal equivalent circuit of PSLLC

From equation 2, 3, 4 and 5 the small signal equivalent circuit of PSLLC is obtained and is shown in Fig. 5.

From Fig. 5 the line to output transfer function $G_{vg}(s)$ is found using the voltage divider formula:

$$G_{V_g}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = \left(-\frac{D}{D'}\right)\frac{1}{1+\frac{L}{D'^2}S+\frac{RL(C_1+C_2)S^2}{D'^2}}. \quad (6)$$

The control to output transfer function $G_{v_{\hat{d}}}(s)$

$$G_{v_{\hat{d}}}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}, \quad (7)$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \left(-\frac{(V_1-V_2)}{D'}\right)\frac{\left[1+S\frac{LI_o}{D'(V_1-V_2)}\right]}{\left[1+\frac{L}{RD'^2}S+S^2L\left(\frac{C_1+C_2}{D'^2}\right)\right]}. \quad (8)$$

Equation (8) gives the expression for control to output transfer function. Equation (6) and (8) gives the transfer function of PSLLC.

4. Design of fuzzy pre-compensated PID controller

The basic block diagram of fuzzy logic controller (FLC) for dc-dc converter is shown in Fig 6. The components of FLC are a fuzzifier, a fuzzy rule base, a fuzzy knowledge base, an inference engine and a defuzzifier [19].The fuzzifier converts crisp quantities into fuzzy quantities. The fuzzy rule base stores the knowledge about the operation of the process to be carried out. The fuzzy knowledge base stores the knowledge about all the input-output fuzzy relationships.

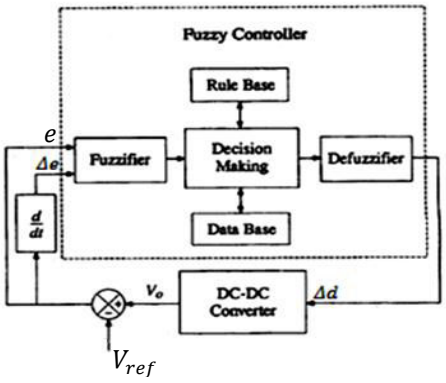


Fig. 6. Block diagram of fuzzy control scheme for dc-dc converters.

The steps involved in designing FLC for load regulation in PSLLC are

Step:1 Select the variables error 'e' and change in error (Δe) for designing FLC in order to regulate load voltage in PSLLC. Error 'e' is the difference between (v_o and v_{ref}) . Change in error (Δe) is the difference between error and change in error

Table 1.Linguistic labels representation of rule base

$e/\Delta e$	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	ZE
NS	NB	NB	NS	ZE	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	ZE	PS	PB	PB
PB	ZE	PS	PB	PB	PB

Step:2 The output to be controlled is the duty ratio of PSLLC.

Step:3 Obtain the membership function for e, Δe and the output. The obtained membership function is shown in Fig 7.

Step:4 Form rule base by assigning the fuzzy rulebase for e, Δe and the output .The rule base is given in Table 1.

Step:5 Choose appropriate scaling factors for input and output variables for normalising variables between [0,1] and [-1,1] interval.

Step:6 Combine the fuzzy outputs from each rule and finally apply defuzzification for fuzzy outputs to form crisp output.

The block diagram of proposed system with fuzzy pre-compensated PID controller is shown in Fig. 8. From Fig. 8 the membership functions error '$e(k)$' and change in error $\Delta e(k)$ are expressed as

$$e(k) = V_{ref} - V_O \quad (9)$$

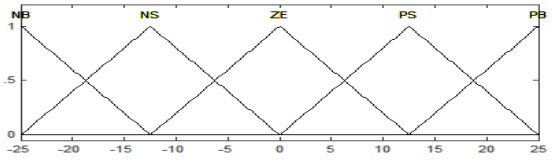
$$\Delta e(k) = e(k) - e(k-1) \quad (10)$$

Where V_{ref} is the reference voltage and V_o is the actual output voltage of PSLLC at k_{th} sampling time.

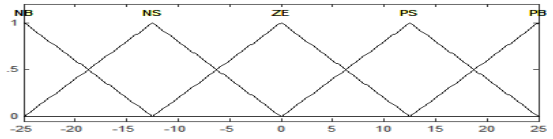
Based on input membership functions error '(e)' and change in error (Δe) the control output from FLC is Δf.

The sum of signals, FLC output Δf and reference voltage V_{ref} generates a reference signal Δu.

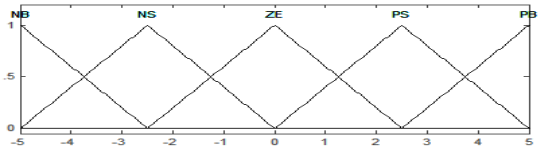
The error difference between Δu and actual output voltage of PSLLC V_o generates an error signal $e(k)$, which is given as input to PID controller.



(a). Membership function for error



(b). Membership function for change in error



(c). Membership function for output

Fig. 7. Membership function for error,Change in error and Output for FLC .

The discrete time domain representation of Fuzzy-pre-compensated PID controller is

$$u(k) = u(k-2) + e(k)\left(K_p + \frac{K_i T}{2} + \frac{2K_d}{T}\right) +$$

$$e(k-1)\left(K_i T - \frac{4K_d}{T}\right) - e(k-2)(K_p - \frac{2K_d}{T}). \qquad (11)$$

The output signal from Fuzzy-pre-compensated PID controller acts as a reference signal for current controller.

The signal from current controller adjusts the duty ratio of respective converters for equal sharing of load current.

6. Results and discussions

This section discusses the simulation studies of parallel connected PSLLCs for PV system. The proposed system is simulated in MATLAB/ Simulink and the performances of fuzzy pre-compensated PID controller and PID controller are compared. BPSX150 PV module is adopted as the PV array model and the specifications are listed in Table 2

Simulations are performed on parallel connected PSLLCs circuits with parameters listed in Table 3 using MATLAB/Simulink. Fig.9 compares simulation waveforms of current sharing among each PSLLC converter module with a dedicated current sharing controller and without a dedicated current sharing controller .

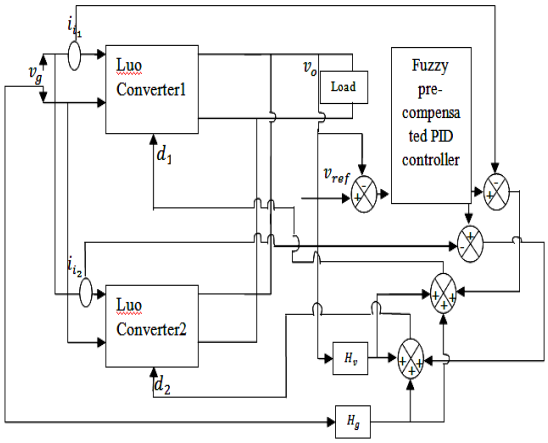


Fig.8 . Block diagram of proposed system using fuzzy pre-compensated PID controller

Fig.9 indicates for current sharing scheme that is not having a dedicated current controller, response of output voltage, output current, output current of module 1 and output current of module 2 settles faster and overshoot is totally reduced.

Table 2.BPSX150 PV module specifications

Parameter	Specification
Peak Power (P_{PV})	80 W
Peak power voltage (V_{PV})	16V
Current at peak power (I_{PV})	5 A
Open circuit voltage (V_{OC})	0.9 V
Short circuit current (I_{SC})	5A

Table 3.Parameters of IPOP connected PSLLCs

Parameter Name	Symbol	Value
Input Voltage	V_{in}	12V
Output Voltage	V_o	36V
Inductor	L_1, L_2	100uH
Capacitors	$C_{11}, C_{12} C_{21}, C_{22}$	30uf
Nominal switching frequency	f_s	100KHz
Load resistance	R_L	50Ω
Output current	I_o	0.72
Range of duty ratio	d	0.3 to 0.9

But for current sharing scheme that is having a dedicated current sharing controller, response of output voltage, output current, output current of module 1 and output current of module 2 takes more time to settle and are having very high overshoot.

Fig.9 shows the effectiveness of proposed current sharing scheme that is not having a dedicated current sharing controller.

Fig.10 shows simulation waveforms of current sharing among each PSLLC converter module with $L_1 = 100\mu H \; and \; L_2 = 110\mu H$ using PID controller and fuzzy pre-compensated PID controller as a voltage regulator. The current sharing scheme is not having a dedicated current sharing controller.

In Fig.10 perfect current sharing takes place in presence of parameter mismatches. Both PID controller and fuzzy pre-compensated PID controller reject line disturbance at t=0.05s. Similarly PID controller and fuzzy pre-compensated PID controller settles correctly for change in load from R=50 Ω to R=40 Ω at t=0.07s.

In fig.10 using fuzzy pre-compensated PID controller the output current 1 and 2 of parallel connected converter module is 0.36A. But for PID controller it is 0.358A.It indicates that fuzzy pre-compensated PID controller works well than PID controller.

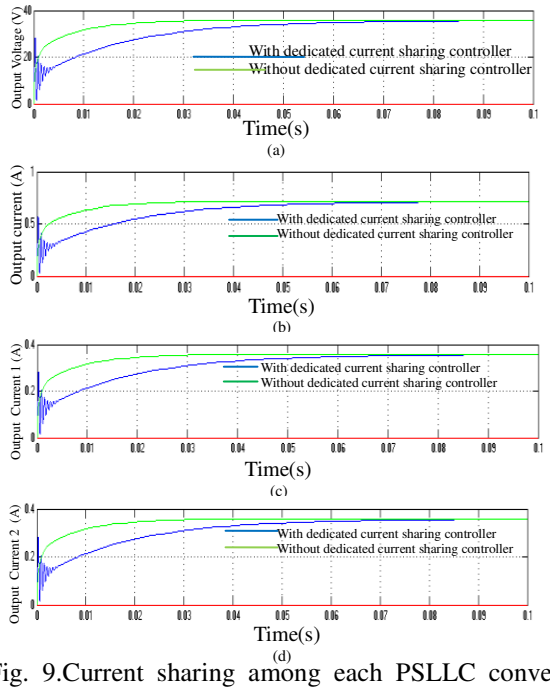


Fig. 9.Current sharing among each PSLLC converter module with dedicated current sharing controller and without dedicated current sharing controller

Fig.11 shows simulation results of output current1 and output current 2 of parallel connected PSLLCs for various values of load resistances. It indicates that for all values of resistances equal sharing of load current takes place between parallel connected PSLLC converter modules.

From Fig.10 and 11 it is inferred that the proposed current sharing scheme works well for fuzzy pre-compensated PID controller as a voltage regulator. Hence the proposed current sharing scheme is implemented in real time using PIC16F877A controller.

For output voltage regulation in parallel connected PSLLCs fuzzy pre-compensated PID controller is used. Because simulation results show that the performance of fuzzy pre-compensated PID controller is better than PID controller. The proposed current sharing scheme is implemented in real time, using PIC16F877A controller

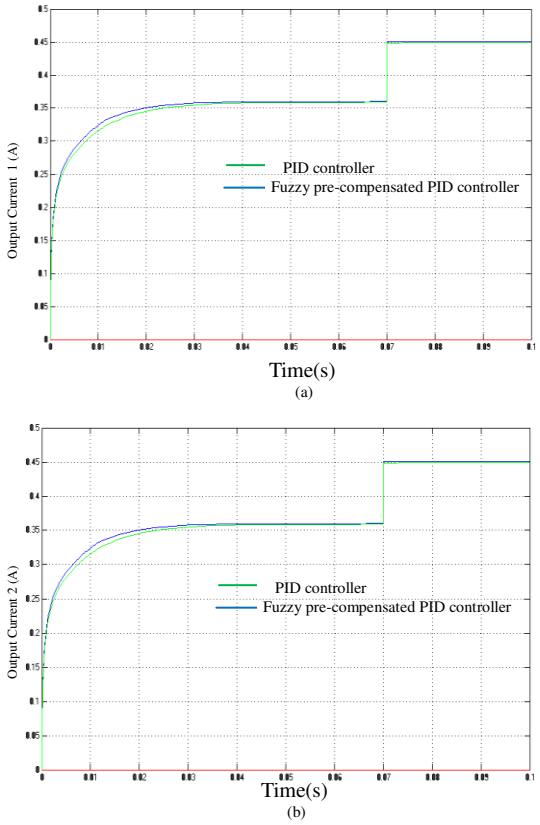


Fig.10. Current sharing among each PSLLC converter module with $L_1 = 100\mu H$ *and* $L_2 = 110\mu H$ using PID controller and fuzzy pre-compensated PID controller for change in load from R=50 Ω to R=40 Ω at t=0.07s.

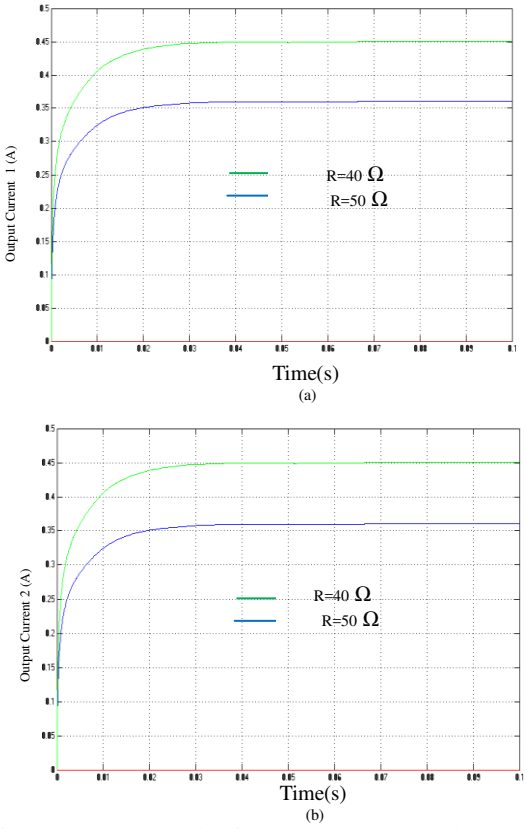


Fig.11.Current sharing among each PSLLC converter modules with $C_{11} = 30\mu F$ *and* $C_{21} = 40\mu F$ for various values of load resistances.

6.1 Experimental Results

As in Fig.8 the prototype of parallel connected PSLLCs has been built to verify the effectiveness of the proposed current sharing scheme. The parameters of solar panel and PSLLC are similar to those used in simulation results.

Fig.12 shows PWM pulse given to PSLLC1 and PSLLC2.

As in fig.8 the individual input currents $(\hat{\imath}_{L_1}$ *and* $\hat{\imath}_{L_2})$ of parallel connected converters are sensed using IC741 current sensor. The sensed individual input currents of converter modules are compared with control signal $(\hat{\imath}_c)$ to generate error signals $(\hat{\imath}_{e_1})$ and $(\hat{\imath}_{e_2})$.

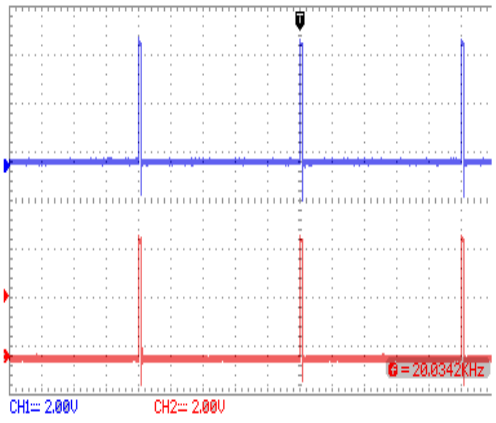


Fig. 12. PWM pulse given to PSLLC1 and PSLLC2

Similarly output voltage $(\hat{v}_o)$ and input voltage $(\hat{v}_g)$ are sensed using IC 741 voltage sensor. The sensed input and output voltage signals are then combined with their corresponding gain values and

generate respective signals $\hat{v}_{h_g}$ and $\hat{v}_{h_v}$ .The negative value of sum of signals from $\hat{v}_{h_v}$, and $\hat{v}_{h_g}$ generate signal $\hat{v}_{go}$.

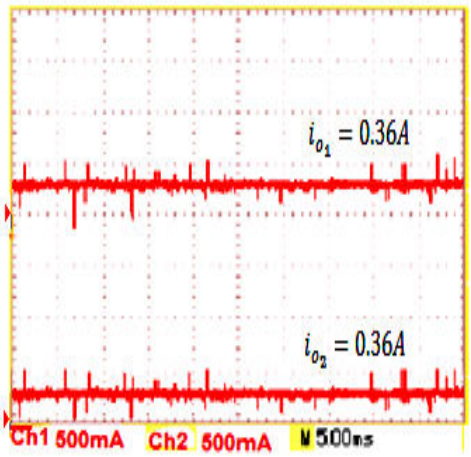


Fig. 13. Response of the individual output currents with $L_1 = 100\mu H$ and $L_2 = 110\mu H$

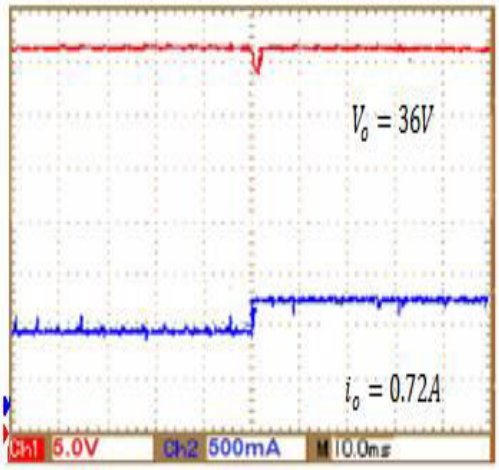


Fig.14. Response of the output voltage and output current with $C_{11} = 30\mu F$ *and* $C_{21} = 40\mu F$ and for load change from 50Ω to 60Ω

The sum of signals from $\hat{v}_{go}$ and $\hat{\imath}_{e_1}$ adjust the gate pulse of module 1 converter. Similarly sum of signals from $\hat{v}_{go}$ and $\hat{\imath}_{e_2}$ adjust the gate pulse of module 2 converter. This ensures load current sharing in parallel connected PSLLCs.

Fig. 13 shows experimental waveforms at full load of 0.72A with difference in individual leakage inductances $L_1 = 100\mu H$ and $L_2 = 110\mu H$.

The waveform indicates even in presence of mismatches in leakage inductances perfect sharing of output current (i_{o_1}=0.36A and $i_{o_2} = 0.36A$) has been achieved.

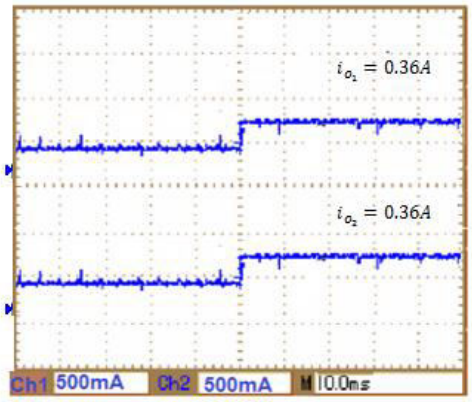


Fig. 15. Response of the individual output currents with $C_{11} = 30\mu F$ *and* $C_{21} = 40\mu F$ and for load change from 50Ω to 40Ω

Figure 14 shows experimental waveforms of output voltage and output current of parallel connected PSLLCs in presence of mismatches in individual capacitances $C_{11} = 30\mu F$ *and* $C_{21} = 40\mu F$.

It indicates that even with load change from 50Ω to 40Ω perfect voltage regulation has been achieved.Fig. 15 shows the response of individual output currents with $C_{11} = 30\mu F$ *and* $C_{21} = 40\mu F$ and for load change from 50Ω to 40Ω.

The waveform indicates that even in presence of mismatches in leakage capacitances and for load change from 50Ω to 40Ω perfect sharing of output current (i_1=0.36A and $i_2 = 0.36A$) has been achieved.

Table 3 shows the comparison between theoretical and experimental results of proposed current sharing scheme using PIC16F877A controller. It indicates that perfect current sharing takes place using proposed current sharing scheme.

Table 3.Comparison between simulation and experimental results

Line/Load Variation	Experimental(PIC16F877A)				Theoretical			
	V_0	I_0	I_{01}	I_{02}	V_0	I_0	I_{01}	I_{02}
(0-1000)W/m^2	36	.72	.36	.36	36	.72	.36	.36
50Ω	36	.72	.36	.36	36	.72	.36	.36
40Ω	36	.9	.45	.45	36	.9	.45	.45
60Ω	36	.6	0.3	0.3	36	.6	0.3	0.3

VI. Conclusion

This paper has proposed a new current sharing scheme in parallel connected PSLLCs which generate higher output current for standalone photovoltaic system. The proposed current sharing scheme gives perfect current sharing without a dedicated current sharing controller. It gives better performance than current sharing scheme having a dedicated current sharing controller. The proposed current sharing scheme ensures perfect current sharing by sensing the input voltage, output voltage and individual currents of IPOP connected PSLLCs. Thus no dedicated current sharing controller is needed. This reduces complexity of the proposed system. Regulation of load voltage takes place using fuzzy pre-compensated PID controller.The proposed

System find its application in satellite communication, uninterrupted power supplies etc.

REFERENCES:

1.McCarthy L., Pieper J., Rues A.,Wu C.H.: *Monitoring in UMR's solar car*. In:IEEE Instrumentation & Measurement Magazine, 3 (2000), No. 3, p. 19-23, Missouri.

2.Huan-Liang, Tsai,Ci-Siang, Tu, Yi-Jie Su.:*Development of Generalized Photovoltaic Model Using MATLAB/SIMULINK*. In: Proceedings of the World Congress on Engineering and Computer Science, October 22 – 24, 2008, San Francisco.

3. Nehrir, M. H., Wang, C., Guda, S. R.*: Alternative energy distributed generation: Need for multi-source operation*. In: Proc. 38th NAPS, 2006, p. 547–551.

4. Wai, R. J., Wang, W. H., Lin, C. Y.: *High-performance stand-alone photovoltaic generation system*. In:IEEE Transaction on Industrial Electronics, 55 (2008), No. 1, p. 240–250, USA.

5.Ramaprabha, R., Mathur B.L., Sharanya, M.:*Solar Array Modelling and Simulation of MPPT using Neural Networks*. In: proc. of IEEE conf. Control. Automation, Communication and Energy Conversion, June 2009, Erode, p. 1-5,.

6. Chih-Yu Yang, Chun-Yu Hsieh, Fu-Kuei Feng, Ke-Horng Chen.:*Highly Efficient Analog Maximum Power Point Tracking (AMPPT) in a Photovoltaic System*. In:IEEE transactions on circuits and systems, 59 (2012), No.7 , p.1546-1556, USA.

7.Hyunsu Bae, Jaeho Lee, Jeonghwan Yang,Bo Hyung Ch.:*Digital Resistive Current (DRC) Control for the Parallel Interleaved DC–DC Converters*. In: IEEE Transactions on Power Electronics, 23 (2008), No. 5 , p. 2465-2476, USA.

8.Xu Zhang, Luca Corradini,Dragan Maksimovic Colorado.:*Sensorless current sharing in digitally controlled two-phase buck dc-dc converetres*. In: Applied Power electronics conference and Exposition, Feb 15-19, 2009, p.70-76.

9. Jassim, B.M.H., Atkinson, D.J., Zahawi, B.:*Modular Current Sharing Control Scheme for Parallel-Connected Converters*. In: IEEE Transaction on Industrial Electronics, 62 (2015) , No.2 , p.887 – 897, USA.

10.Jassim, B.M.H., Zahawi, B., Atkinson, D.J.:*Virtual impedance current sharing control of parallel connected converters for AC motor drives*. In: IEEE Energy Conversion Congress and Exposition (ECCE),September 14-18 , 2014, Pittsburgh, p.5024 – 5028.

11.Wang, J. B.:*Primary Droop Current-Sharing Control of the Parallel DC/DC Converters System considering Output Cable Resistance*. In: Advances in Power Electronics, (2011) , Article ID 713250.

12. Erdogan, A. D., Mehmet Timur Aydemir.: *Use of input power information for load sharing in parallel connected boost converters*. In: Electrical Engineering, 91 (2009), No.4, p. 229-250,Heidelberg .

13. Ming Li, Chi K, Tse˙,Xikui Ma.:*Calculation of steady-state solution of parallel-connected buck converters with active current sharing and its parameter sensitivity*. In: International Journal of Circuit Theory and Applications, 39 (2011), No. 3, p. 275–297, USA.

14. A.Johnsy.: *Analysis of a Control Strategy for Parallel Operation of Single Phase Voltage Source Inverters*. In: International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, 3 (2014) , No.2, p.148-154, India.

15. Jianjiang Shi, Zhejiang Univ, Hangzhou, Tianji Liu,Juan Cheng Xiangning He.:*Automatic Current Sharing of an Input-Parallel Output-Parallel (IPOP)-Connected DC–DC Converter System With Chain-Connected Rectifiers*. In: IEEE Transactions on Power Electronics , 30 (2015) ,No. 6 ,p.2997-3016, USA .

16.Deshang Sha ,Zhiqiang Guo, Xiaozhong Lio.: *Cross-Feedback Output-Current-Sharing Control for Input-Series-Output-Parallel Modular DC–DC Converters*. In: IEEE Transactions on Power Electronics, 25 (2010), No.11,p.2762-2771, USA.

17.Dhanasekar, Kayalvizhi, R.:*Design and Simulation of PI Control for Positive Output Triple Lift Luo Converter*. In: International Journal of Modern Engineering Research ,2 (2012) , No.6, p.4186-4188, India.

18. Joseph Basanth, A., Natarajan, S.P., Sivakumaran, T.S.:*Performance Analysis of Positive Output Super-Lift Re-Lift Luo Converter With PI and Neuro Controllers*. In: IOSR Journal of Electrical and Electronics Engineering, 6 (2013) , No. 3, p. 21-27, India.

19.Zainal Salam, Fazel Taeed, Shahrin Md. Ayob.:*Design and Implementation of a Single Input Fuzzy Logic Controller for Boost Converters*. In: Journal of Power Electronics, 11 (2011), No. 4, p.542-550, South Korea.