Practical Design Aspects of SHE PWM Controlled 1ph. STATCOM

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Abstract: *This paper addresses the key issues of design and implementation of Selective Harmonic Elimination (SHE) PWM controlled 1ph. STATCOM. A simulation model of 25kV, +/- 600kVAR STATCOM is presented. The total capacity of 600kVAr is divided into eight parallel connected modules of +/-75kVAr, connected at the secondary of a 25kV/425V transformer. On-line control technique of SHE PWM Voltage Source Inverter (VSI) is proposed. The technique is based on on-line solution of 7^{th} order polynomial equations approximately representing SHE solution trajectories, relating SHE switching angles and modulation index, m. A methodology for selection of passive components is also proposed. A robust phase synchronization technique based d-q transformation is used to maintain rigid phase locking. A prototype of the 230V, +/- 20kVAR, 1ph. STATCOM module is built to test the effectiveness of the on-line VSI control technique. The 20kVAr STATCOM is controlled by a 16 bit-fixed point processor (TMS320LF2406). Simulation and experimental results of are in good agreement and show the prowess of the developed prototype.*

Key words: *Selective Harmonic Elimination, 1ph. STATCOM, Voltage Source Inverter, Coupling Inductor, Phase Synchronization.*

1. Introduction

While the power demand is growing leaps and bounds, public concerns over space, environmental impacts and costs are making it more difficult for utility companies to expand their networks. This has created a need of power conditioning and flow control devices to ensure full utilization of the existing capacity of the network. Power electronics technology has given solution to the need of the hour. FACTs devices have been used for manipulation of power flow, control of voltage levels, reactive power compensation, and damping of oscillations to improve transient stability, harmonic filtering. This paper presents various design issues of SHE PWM controlled 1ph. STATCOM. The proposed application of the STATCOM is at 25kV/425V 1ph. traction substation.

2. Working Principle of 1ph. STATCOM.

STATCOM (STATic COMpensator) is a power electronic equivalent of synchronous condenser. Its inductive and capacitive output currents can be controlled independently from its connected AC bus voltage. STATCOM has increased transient ratings both in inductive as well as capacitive regions [1]. The basic schematic block diagram of 1ph. STATCOM is as shown in Fig.1. The VSI converts the DC voltage across DC capacitor into PWM output that is in synchronism with the AC supply voltage. The DC capacitor provides a circulating current path and acts as a DC voltage source for inverter operation.

The difference between the inverter output and the AC supply voltage determines the direction of reactive power flow, i.e., if the magnitude of the VSI output voltage is increased above supply voltage, then the VSI generates capacitive reactive power and if the magnitude of VSI output voltage is decreased below the supply voltage, the VSI absorbs inductive reactive power. The VSI can exchange real power with the supply system. This can be done by adjusting the phase angle between the supply voltage and the VSI output voltage. If VSI output leads the supply voltage, VSI supplies real power and if it lags behind the supply voltage, it absorbs real power. In practical STATCOM, a small lagging phase shift between supply voltage and VSI output has to be maintained to supply VSI losses and maintain the DC bus voltage. The active and reactive powers can be expressed as,

$$P = \frac{V_s V_0}{X_{L_{ac}}} \sin(\partial) \quad (1)$$

$$Q = \frac{V_s^2}{X_{L_{ac}}} - \frac{V_s V_o}{X_{L_{ac}}} \cos(\partial) \quad (2)$$

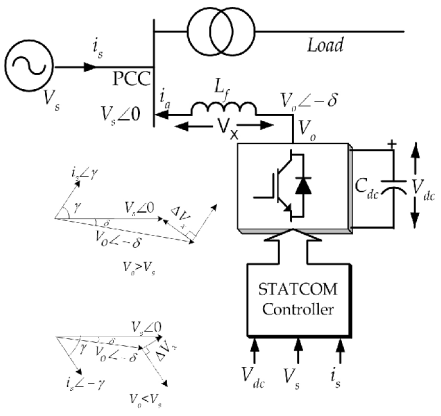

Fig. 1. Basic Schematic block diagram of single phase STATCOM

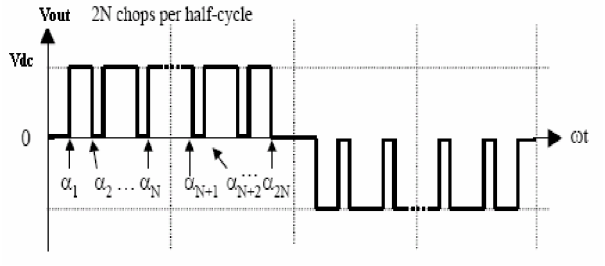

Fig. 2. SHE PWM output waveform

2. VSI switching logic.

The switching module is an integral component of the STATCOM. Its task is to control the switching sequence of the various semiconductor devices aiming at producing output waveform as near as possible to a sinusoid with high controllability and low switching loss. Presently used VSI switching techniques can be classified in two categories; Fundamental frequency switching, Pulse Width Modulation Method (PWM) [2]. In the present work SHE PWM technique has been used. The SHE PWM inverters eliminate low order harmonics and operate at low switching frequency that result in reduced switching losses. SHE PWM was originally proposed by Patel and Hoft [3] [4]. The SHE-PWM output waveform obtained from H-Bridge VSI consists of series of positive and negative pulses of constant amplitude but variable switching angles as shown in Fig. 2. The waveform has N switching angles per quarter cycle to eliminate first $(N-1)$ odd harmonics from the inverter output. The switching angles $\alpha_1, \alpha_2, \alpha_3, \ldots \alpha_N$ need to be calculated for given modulation index, m. The output waveform being odd symmetric, dc and even harmonic components are equal to zero. The Fourier series of the three-level VSI output voltage can be expressed as,

$$V_o(\omega t) = \sum_{k=1}^{\infty} a_k \sin(k\omega t) \tag{3}$$

where, $a_k = \dfrac{4V_{dc}}{k\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(k\alpha_j)$ (4)

k is the harmonic order. N is the number of switching angles per quarter cycle. V_{dc} is the amplitude of DC voltage source and α_j is the j^{th} switching angle which must satisfy the following condition,

$$\alpha_1 < \alpha_2 < \alpha_3 < \ldots \alpha_j \ldots < \alpha_N < \frac{\pi}{2}$$

Defining modulation index, $m = \dfrac{V_{o1}}{V_{dc}}$,

the non-linear SHE-PWM equations are,

$$\begin{aligned}
\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3) \ldots\ldots \pm \cos(\alpha_N) &= \frac{\pi}{4}m \\
\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) \ldots\ldots \pm \cos(3\alpha_N) &= 0 \\
\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) \ldots\ldots \pm \cos(5\alpha_N) &= 0 \\
\cos(N\alpha_1) - \cos(N\alpha_2) + \cos(N\alpha_3) \ldots\ldots \pm \cos(N\alpha_N) &= 0
\end{aligned} \tag{5}$$

For given m, the nonlinear equations in (3) can be solved numerically using Newton iteration technique [3] to get $\alpha_1, \alpha_2, \alpha_3, \ldots \alpha_N$. Typical solution trajectories are shown in Fig. 3. The solution process is math intensive and convergence largely depends upon choice of the initial values. This makes it unfit for microprocessor implementation. Various techniques for on-line solution of SHE equations are reported in [5] [6] [7]. A relatively simple method [8] based on curve fitting is implemented here which is described in subsequent sections.

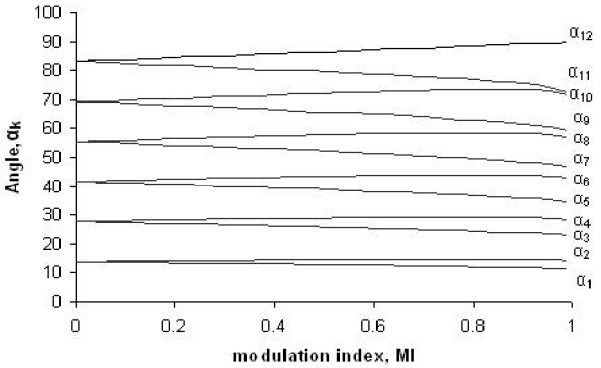

Fig. 3. Typical solution trajectories of switching angles

4. Online control of SHE VSI

The approach taken here is to represent the solution trajectories with a polynomial equation in terms of m. By using polynomial regression method [8], the approximate nth order polynomial can be expressed as,

$$\alpha = C_0 + C_1 m + C_2 m^2 + \ldots\ldots + C_n m^n \tag{6}$$

where n the polynomial order. The unknown coefficients $C_0, C_1, \ldots C_n$ are calculated using least square fit which minimizes the sum of squares of the deviations of the data which in this case is the values of α corresponding to each m, from (5). The order of the polynomial equations representing each trajectory is determined comparing residuals for various fits. Presently, a 7th order polynomial is used to represent the α trajectories. The proposed SHE PWM VSI output has 12 switching instants per quarter cycle to eliminate 3rd to 23rd harmonics from the inverter output. The values of C_0 to C_7 are given in the Table 1 for typical values of $\alpha_1, \alpha_2, \alpha_3$. Rests of the values are computed in the similar manner. The residual error for a typical modulation index is shown in Fig. 4. The maximum error is less than 0.006^0 which ensures accurate α calculation for a given m.

Table 1. SHE Polynomial constants

	α_1	α_2	α_3
C_0	13.8407	13.8476	27.6943
C_1	-1.7945	1.4384	-3.5137
C_2	1.8846	3.3679	4.2996
C_3	-17.0898	27.5460	36.8583
C_4	55.8251	88.6621	119.9109
C_5	-93.1147	-147.890	-199.930
C_6	76.8612	122.109	164.943
C_7	-25.0164	-39.777	-53.6554

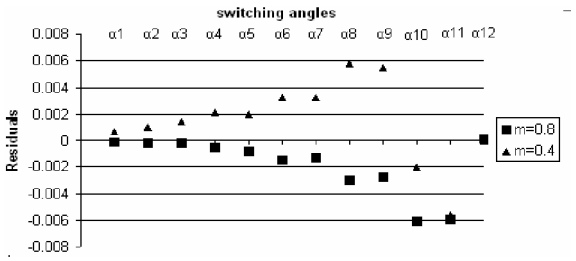

Fig. 4. Residual error in α for m=0.8, 0.4

5. Selection of passive components of STATCOM

Apart from the power electronic control and other design aspects of the STATCOM, optimum selection of passive components viz. coupling inductor and DC capacitor are of subtle importance as it controls the performance, cost, size of STATCOM. Selection methodology of passive elements of 3ph. STATCOM is discussed in [9] [10] [11]. The selection of the two passive elements, L_{ac}, C_{dc} is mainly constrained by harmonic distortion of the STATCOM injected current at point of common coupling (PCC) at rated conditions and DC bus voltage ripple respectively. The assumed upper limits of those parameters are as per the Indian Railways Standard considering application of the STATCOM for Dynamic Reactive Power Compensator at a 25kV traction substation. The constraint on the TDD of the STATCOM injected current at PCC is less than 17% and the allowable ripple in the dc bus voltage is less than 5%.

By using mathematical model of the VSI at fundamental and harmonic frequencies and imposing the above limits, optimum value of L_{ac}, C_{dc} are calculated. The method can be generalized for SHE controlled 1ph. STATCOMs. The detailed procedure and the simulation results are given in the following subsections.

5.1 Selection of coupling reactor

Consider the fundamental frequency equivalent circuit of the STATCOM as shown in Fig.5. It is presumed that the switching elements, coupling inductor are ideal. From Fig. 5,

$$V_{o1} = V_s + j I_{a1} \omega L_{ac} \tag{7}$$

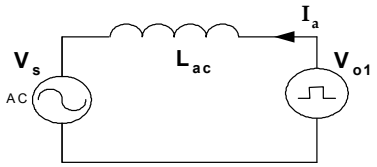

Fig.5. Fundamental frequency circuit of STATCOM

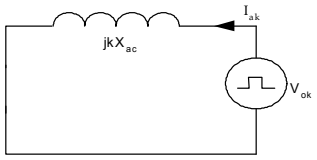

Fig. 6. Equivalent circuit of STATCOM at harmonics

The VSI output voltage can expressed as [3],

$$V_{o1} = \frac{4V_{dc}}{\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(\alpha_j) \tag{8}$$

where *(N-1)* harmonics are eliminated and α_j are the switching angles as shown in Fig.2. The p.u. values are expressed with base values as, $V_{base} = V_s$, rated supply voltage and $I_{base} = I_{a1}$, rated fundamental current supplied by STATCOM.

The equation becomes,

$$1 + X_{ac} = \frac{4V_{dc}}{\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(\alpha_j) \tag{9}$$

This equation gives minimum value of X_{ac}. From equivalent circuit for harmonics as shown in Fig. 6,

$$V_{ok} = j k X_1 I_{ak} \tag{10}$$

The total demand distortion (TDD) is defined as,

$$TDD_i = \frac{100}{I_{a1}}\left\{\sum_{k=2}^{\infty}\left(I_{ak}\right)^2\right\}^{\frac{1}{2}}$$

$$TDD_i = \frac{100}{I_{a1}}\left\{\sum_{k=2}^{\infty}\left(\frac{V_{ok}}{k\,X_{ac}}\right)^2\right\}^{\frac{1}{2}} \tag{11}$$

where,

$$V_{ok} = \frac{4V_{dc}}{k\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(k\alpha_j) \tag{12}$$

Substituting (12) in (11),

$$TDD_i = \frac{100}{I_{a1}X_{ac}}\left\{\sum_{k=2}^{\infty}\left(\frac{4V_{dc}}{k\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(k\alpha_j)\right)^2\right\}^{\frac{1}{2}} \tag{13}$$

Considering I_{a1} as 1p.u., X_{ac} can be calculated as,

$$X_{ac} = \frac{100}{TDD_i}\left\{\sum_{k=2}^{\infty}\left(\frac{4V_{dc}}{k\pi}\sum_{j=1}^{N}(-1)^{j+1}\cos(k\alpha_j)\right)^2\right\}^{\frac{1}{2}} \tag{14}$$

The equations to be solved are (9) and (14) to get the optimum value of L_{ac}.

5.2 Selection of DC Capacitor

DC capacitor plays an important role in STATCOM performance and its overall cost as well. Proper sizing of dc capacitor is essential to lower the system cost and optimize performance. An expression is derived for dc capacitor voltage, V_{dc}. The optimum value of C_{dc} is selected to meet the minimum (5%) ripple voltage constraint. The equivalent circuit of H-bridge VSI is shown in Fig. 7. The dc side current, i_{dc} and the injected current, I_a be related by following equation [12],

$$i_{dc}(t) = sw(t)\, i_a(t) \tag{15}$$

The switching function, $sw(t)$ is defined as,

$$sw(t) = \frac{V_o(t)}{V_{dc}}$$

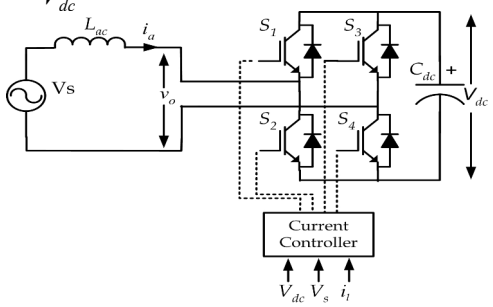

Fig. 7. Schematic diagram of H- Bridge VSI

Considering fundamental component of injected current,

$$i_a(t) = I_m \sin(\omega t \pm \phi) \tag{16}$$

Substituting in (15),

$$i_{dc}(t) = \frac{V_o(t)}{V_{dc}} I_m \sin(\omega t \pm \phi) \tag{17}$$

where, $$V_o(t) = \sum_{k=1}^{\infty} V_{ok} \sin(k\omega t) \tag{18}$$

Substituting (18) in (17),

$$i_{dc}(t) = \frac{\sum_{k=1}^{\infty} V_{ok} \sin(k\omega t)}{V_{dc}} I_m \sin(\omega t \pm \phi) \tag{19}$$

Considering only fundamental component of $V_o(t)$,

$$i_{dc}(t) = \frac{V_{o1} \sin(\omega t)}{V_{dc}} I_m \sin(\omega t \pm \phi) \tag{20}$$

$$C_{dc} \frac{dV_{dc}}{dt} = \frac{V_{o1} I_m}{V_{dc}} \sin(\omega t) \sin(\omega t \pm \phi) \tag{21}$$

Simplifying further,

$$\frac{dV_{dc}}{dt} = \frac{V_{o1} I_m}{2 C V_{dc}} \left[\cos(\phi) - \cos(2wt \pm \phi)\right] \tag{22}$$

$$V_{dc}(t) = V_{dc}(0) - \frac{V_{o1} I_m}{4 C_{dc} V_{dc} \omega} \sin(2\omega t \pm \phi) \tag{23}$$

Where $V_{dc}(0)$ is the steady value of the dc bus voltage. By specifying the peak-to-peak ripple voltage, ΔV_{dc} in the above equation, optimum value of C_{dc} can be calculated as,

$$C_{dc} = \frac{m I_{am}}{2 \omega \Delta V_{dc}} \tag{24}$$

Equations (14) and (24) are guiding equations for selection of L_{ac} and C_{dc}. The calculated values for 75kVAr STATCOM are listed in Table 2.

Table 2 Parameters for 1ph. 75kVAR STATCOM

STATCOM rating	75 kVAR
System rated voltage, V_s	425 V
Rated fundamental current, I_{a1}	177 A
DC voltage, V_{dc}	750V
No. of harmonics eliminated, *(N-1)*	11 (3^{rd} to 23^{rd})
Pulses per quarter cycle in VSI output, N	12
Coupling Reactance, L_{ac}	1.4mH
DC Capacitor, C_{dc}	13000 μF

6. Phase synchronization

The phase locked loop (PLL) used here is based on inverse park transformation method to achieve better filtering of harmonics [14] [15]. In order to adopt this method for 1ph application, an artificial orthogonal signal is internally generated (V_β). The complete block diagram of the PLL structure is shown in Fig. 8. A single phase voltage (V_s) (input as V_α) and internally generated V_β are used as an input to the park transformation block ($\alpha\beta$-dq). V_β is obtained through an inverse park transformation block where the inputs are d-axis and q-axis output of the park transformation block fed through first order low pass filter. The first order lag blocks need to be adequately tuned in order to guarantee performance of the PLL. The simulink model is shown in Fig. 8 and the frequency tracking response in Fig. 9, which validates effectiveness of the technique used.

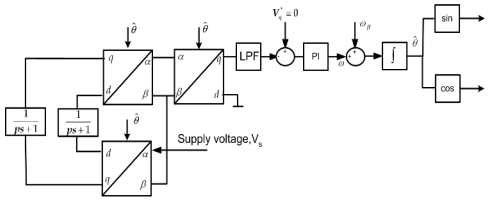

Fig. 8. PLL structure based on d-q transformation

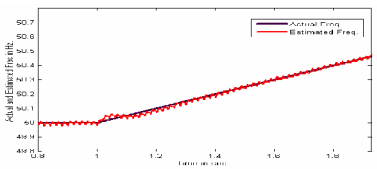

Fig. 9 Frequency tracking response of d-q PLL

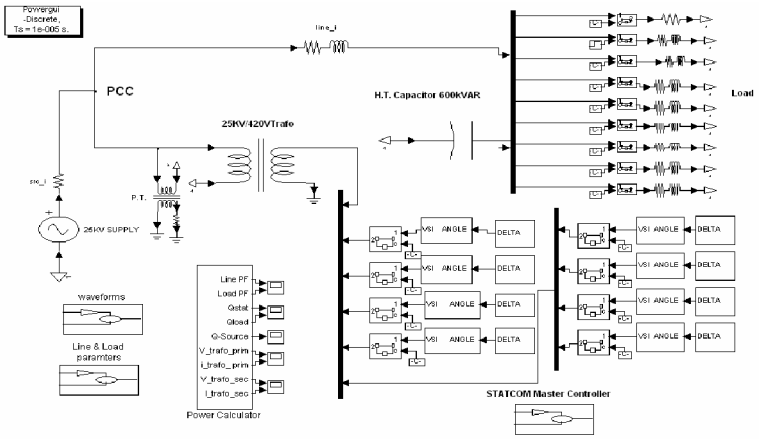

Fig. 10. Simulink diagram of the +/600kVAr 1ph.

7. Simulation of +/600 kVAr STATCOM

The network model used for simulation is based on traction substation requirements of Indian railways. The STATCOM is connected to the secondary side of the 25kV/425V step-down transformer. There is a fixed bank of 600kVAr on 25kV side. The STATCOM along with HT capacitor bank can inject 0-1200kVAr capacitive reactive power into the grid. Whenever there is no load, the STATCOM injects 600kVAr to nullify 25kV side fixed capacitive kVAr. The total 600kVAr to be injected at PCC is divided in 8 modules of 75kVAr each. The STATCOM master controller measures the load reactive power (including that of HT capacitor bank) and calculates the total reactive power to be injected into the grid. The master controller is implemented using Simulink state-chart. The net requirement is divided into 8 modules. The distribution is in such a manner that full capacity of the individual 75kVAr module is utilized. The master controller sends reactive power reference to each individual 75kVAr module. The module has a P+I controller to control modulation index, *m*, which in turn controls the fundamental output voltage of VSI to track the reactive power reference. The SHE switching angles for the given, *m*, are calculated by solving polynomial equations. The DC bus voltage is maintained at 750V by another P+I controller that adjusts phase angle, δ, between the fundamental component of the utility voltage and VSI output. The power circuit parameters of 75kVAr module are listed in Table 2. The overall simulation diagram is shown in Fig. 10. The responses of the 25kV side voltage and current, as shown in Fig. 11, are recorded with a step input in the load reactive power from -600kVAr to +1200kVAr. As seen from 25kV side current in Fig. 11, the response time is less than 3 power cycles. The harmonic spectrum of the current is shown in Fig. 13 and THD is less than 5.5%. The DC bus voltage response is shown in Fig. 12. The ripple in the DC Bus voltage is well below 5%.

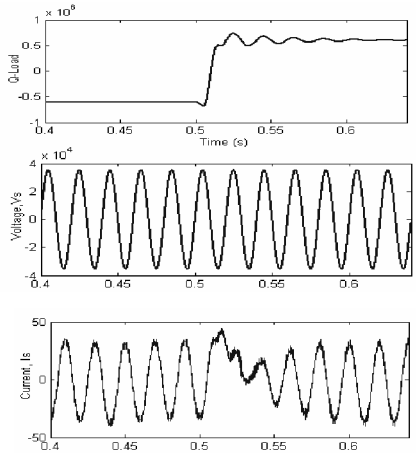

Fig. 11. Simulated step response

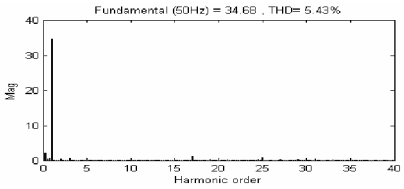

Fig. 12. Harmonic spectrum of 25kV side current

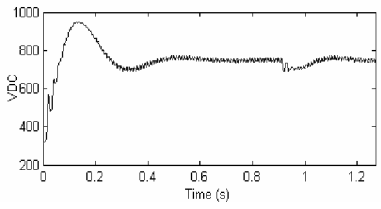

Fig. 13. DC Bus Response of 75kVAR module

8. Practical Implementation of +/-20kVAR prototype

Various issues of DSP based STATCOM are discussed in [13]. In the developed proto type, the VSI is implemented using Semikron make IGBT H-bridge inverter with skyperpro-32 IGBT driver card. Block diagram of prototype is shown in Fig. 14. The coupling inductor and DC capacitor values are as shown in Fig. 14. The DC capacitor is externally charged to 60% of the set voltage by externally connected bridge rectifier. The charging circuit (not in Fig. 14) is disconnected and then the firing pulses are applied to the VSI and the main contactor is turned on. A harmonic filter is used to filter out 25^{th} and 27^{th} harmonics from the injected current. The control hardware for +/-20kVAR STATCOM is built around Texas instruments 16-bit DSP Processor TMS320LF2406 operating at 40MHz clock frequency. The supply voltage is sensed by a 230V/5V potential transformer. Supply current and STATCOM current are sensed by using a Hall-effect sensor. AC signals are sampled at 10ksps using on-chip 10bit ADC. The DC voltage is attenuated to a suitable level and sensed by using an analog opto-isolator (Analog Devices, AD-202). The signal conditioning is done by a 3.3V op-amp, Texas Instrument's OPA348). It is attempted to keep minimum analog circuitry to get rid of EMI problems and the signal processing is mainly in digital form. Various software modules include:

1) **Phase synchronization**: Phase sync logic is as described in [13]. The output of the PLL is a logic signal generated on T1PWM of Timer T1, synchronized to fundamental component of the supply voltage. Timer T1 belongs to event manager EVA.
2) **Power line parameters**: Software routines for active, reactive, apparent power, power factor, etc. Timer T2 of event manager EVA is used to trigger ADC for sampling of instantaneous supply voltage and current and the DC bus voltage. Timer T2 period, T2PR, is adjusted according to frequency of the supply voltage so that 200 samples are taken for each power cycle.
3) **Reactive power controller**: It is a PI controller that controls the modulation index, *m*, to track the command kVAr. Based upon the value of *m* switching angles, α_1, α_2,... α_{12} are calculated by solving polynomial equations. A zero kVAr reference is taken in presently.
4) **DC voltage PI controller**: It adjusts phase shift (δ) between supply voltage and VSI output fundamental. The output of the DC bus voltage controller is δ. Phase shifted reference signal for the fundamental VSI output is generated on T4PWM of timer T4 that belongs to event manager EVB. The DC voltage is maintained at 400V.
5) **SHE PWM pulse generation**: The synchronized SHE PWM pulse generation is done by using two 16-bit timers T3PWM and T4PWM. T3PWM generates actual SHE pulses synchronized with reference of phase shifted reference signal generated by T4PWM. SHE pulses are generated by configuring T3PWM in up-counting mode. The compare and period values (for T3PWM) for each α are calculated for every fundamental cycle. The compare and period values are stored in a 24 element array (12 switching angles in quarter cycle).The array counter is reset on period interrupt of T4PWM. The routine for α calculation for given *m,* is in main program and takes less than 500μsec.
6) **Protections**: Various protections are provided for over-current, over-voltage, DC Bus over-voltage, IGBT bridge short circuit and over temperature.

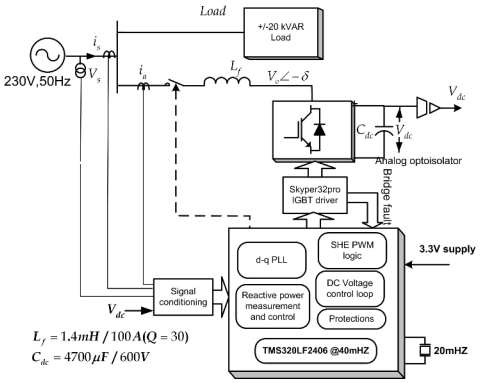

Fig. 14. Block diagram of the practical setup of +/- 20kVAR STATCOM

9. Responses of +/20 kVAR prototype

The response of the prototype was tested at rated conditions. The supply voltage and current waveforms of STATCOM and source for 20kVAR inductive load is shown in Fig. 15 and Fig. 16. and that for 20kVAR capacitive load is shown in Fig. 17 and Fig. 18. The current waveforms also show the effect of harmonic filtering. The VSI output is shown in Fig. 19 along with the coupling inductor current before harmonic filtering. The step response was tested by giving a step input of 5kVAR and the response is as shown in Fig. 20. The response time is less than 4 power cycles for step input of 5kVAr. A tuned filter is used to filter out switching frequency component in the injected current. The current THD is 15%. The average power losses of the 20kVAr STATCOM module are 20W/kVAr.

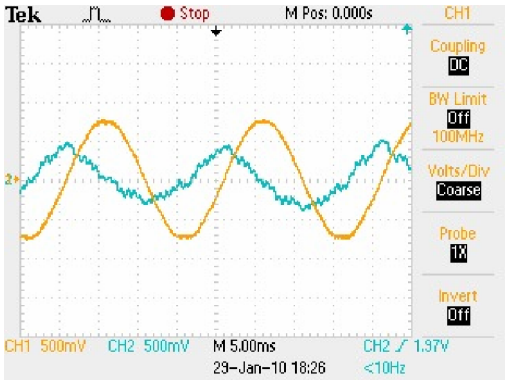

Fig.15.Supply voltage and STATCOM current when compensating +20kVAR

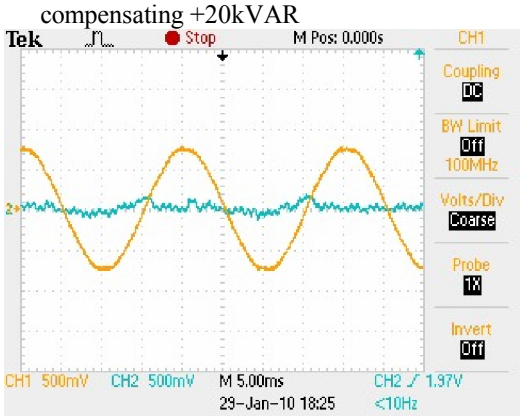

Fig. 16. Supply voltage and current after +20kVAr compensation

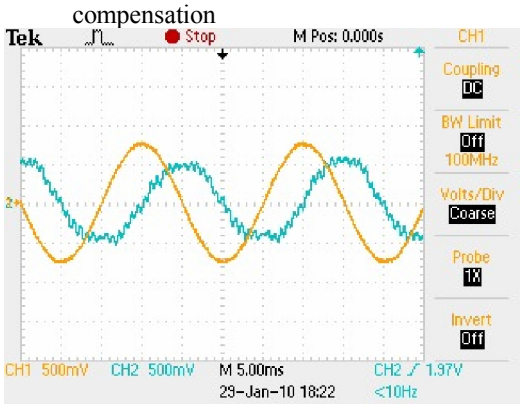

Fig.17 Supply voltage and STATCOM current when compensating -20kVAR

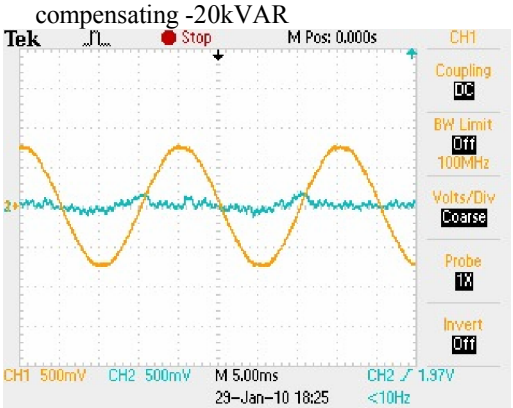

Fig.18. Supply voltage and current after -20kVAR compensation

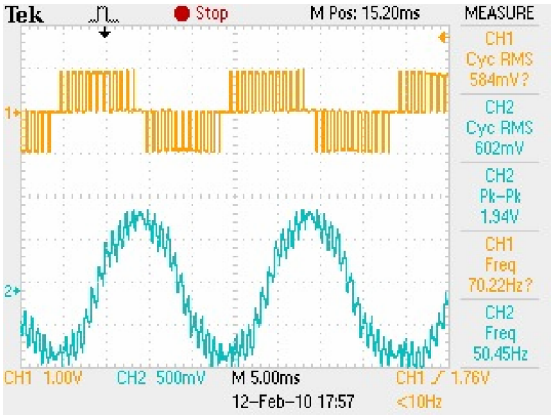

Fig. 19. VSI output and coupling inductor current

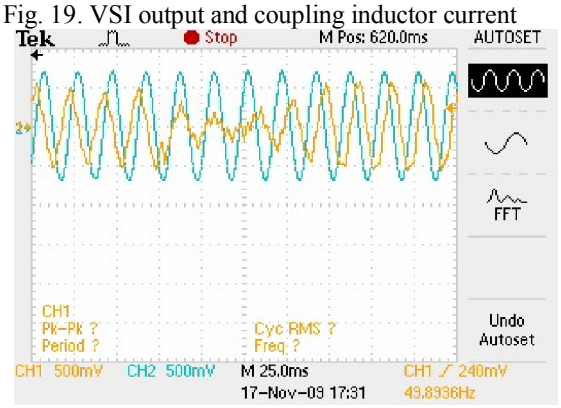

Fig. 20. Step response to -5kVAR to +5kVAR Step input

10. Conclusions

Results of simulated model and prototype are in good agreement and responses of the prototype confirm the efficacy of the proposed method for on-line control of SHE VSI and encourage for implementation for a larger capacity STATCOM as proposed in the simulation. Accurate phase locking with minimum jitter, proper selection of passive parameters, execution time, fast acting protections, are some of the important aspects attempted to be addressed in the prototype design to ensure satisfactory operation of the STATCOM. The speed of response (3 cycles) need to be further enhanced by adopting a faster processor having larger bit-width. Implementation of the parallel connected STATCOM modules as shown in simulation can be with networking of STATCOM controllers.

11. Acknowledgment

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12. References

1. Hingorani, N., Gyugyi, L.: *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*, IEEE Press, Piscataway, NJ, 1999.
2. Acha, E., Fuerte-Esquivel, C.R.: *FACTS Modelling and Simulation in Power Networks*, John Wiley and Sons, ISBN 0-470-85271-2, 2004.
3. Patel, H., Hoft, R.: *Generalized technique of harmonic elimination and voltage control is thysristor inverters. Part I harminic elimination*. In: IEEE Transactions on Industrial Applications, Vol IA-9, no. 3, May-June 1973, pp 310-317.
4. Enjenti, P., Ziogas, P., Lindsay, J.: *Programmed PWM techniques to eliminate harmonics-a critical evaluation*. In: IEEE Trans. On Industry Applications, Vol. 26, No.2, March 1990, pp.302-315.
5. Czarkowski, D., chudnovsky, D., Chudnovsky, G., Selensnick, I.: *Solving the optimal PWM problem for Single-Phase Inverters*. In: IEEE Trans. On Circuits and Systems-I: fundamental theory and applications, Vol. 49, No.4., April 2002, pp. 465-475.
6. Chiasson, J., Tolbert, L., Mckenzie, K., Du, Z.: *A Complete Solution To Harmonic Elimination Problem.* In: IEEE Transactions on Power Electronics, Vol. 19, No.2, March 2004, pp. 491-499.
7. Jabr, R.: *Solution Trajectories Of The Harmonic Elimination Problem*. In: IEE Electric Power Applications, Vol. 153, No.1, Jan. 2006, pp. 97-104.
8. Azli, N., Yatim, A.H.M.: *Curve Fitting Technique For Optimal Pulsewidth Modulation (PWM)Online Control Of A Voltage Source Inverter (VSI)*. In: Proceedings of TENCON 2000, Vol. 1, pp. 419-422.
9. Eknayake, Jenkins, N.: *Selection Of Passive Elements For Three Level Inverter Based Static Compensator*. In: IEEE Trans. On Power Delivery, Vol.14, No.2, April 1999, pp. 665-661.
10. Moran, L., Ziogas, P., Joos, G.: *Analysis And Design Of A Three-Phase Synchronous Solid-State Var Compensator*. In: IEEE Transactions On Industrial Applications, Vol.25, No.4, July-August 1989, pp. 598-610.
11. Singh, B., Murthy, S., Gupta, S.:*Analysis And Design Of Statcom-Based Voltage Regulator For Self-Excited Induction Generators*. In: IEEE Trans. On Energy Conservation, Vol.19, No.4, Dec.2004, pp. 783-790.
12. Liang, Y., Nwankpa, C.: *A New Type Of STATCOM Based Cascading Voltage-Source Inverters With Phase-Shifted Unipolar SPWM*. IEEE Trans. On Industry Applications, Vol. 35, No. 5, Sept-Oct. 1999, pp.1118-1123.
13. Xu, L. Agelidis, V.G. Acha, E.: *Development Considerations of DSP Controlled PWM-VSC Based STATCOM*. In: Proc. of IEE Electric Power Applications, Vol.148, No.5, Sep. 2001, pp. 449-455.
14. Arruda, L. N., Silva, S. M., Filho, B.J.C.: *PLL Structures for Utility Connected Systems*. In: Proceedings of Industry Applications Conference, 2001, Vol.4, pp. 2655 – 2660, Oct.2001.
15. Mihai, C., Remus, T., Blaabjerg, F.: *Improved PLL Structures For Single-Phase Grid Inverters*. In: Proceedings of PELINCEC 2005, pp. 1-6.