

DESIGN AND VALIDATION OF SIMPLE SPACE VECTOR PWM SCHEME FOR THREE-LEVEL NPC - MLI WITH INVESTIGATION OF DC LINK IMBALANCE USING FPGA IP CORE

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Abstract: This paper presents a generalized implementation of the 3-level SVPWM technique and investigation of the imbalances in the D.C-link capacitor voltage in Three Level Neutral point diode clamped (NPC) multilevel inverter (MLI), which is one of the main drawbacks of NPC multilevel inverter. The proposed scheme easily determines the location of the reference vector and calculates on-times. It uses a simple mapping to generate gating signals for the inverter. The capacitor imbalance is also investigated depend upon the phase currents available in the each switching state. The redundant state guarantees to achieve voltage balancing up to 0.75 % with no requirement of any additional control effort. VHDL language is used to model the inverter switching strategies. The benefit of the proposed scheme has been verified through the Mat lab simulation and it's validated in FPGA- SPARTEN III IP Core

Key words: D.C-link capacitor voltage balance, Neutral-point Diode-clamped Multi Level inverter (NPC-MLI), Space Vector PWM (SVPWM), Mat lab-Simulation, Field Programmable Gate Array (FPGA).

1. Introduction

Multilevel inverters were proposed in 1981 by Nabae.A [1]. Since then multilevel inverters have drawn interest in the electrical power industry in recent years. They offer a set of features that are well suited to high-voltage drive systems and power system applications such as high voltage dc (HVDC) transmission, reactive power compensation equipment[2], power conditioning, and active power filtering and so on. They were initially proposed as an extension of the conventional inverters to withstand increased dc link voltage produced by series connection of the semiconductor devices and effective clamping of voltage across each semiconductor in phase leg, through diodes (Neutral Point Clamped inverter) or capacitors. On the basis of which multilevel inverters

have been classified as Diode clamped inverter, Capacitor Clamped inverter and Hybrid type inverter. The unique structure of multilevel voltage source inverters allow them to operate at high voltages with low harmonic content without the use of transformers and filter circuits, and without the need to increase the switching frequency. Neutral point diode clamped inverter (NPC) inverter fig.1 suffer from the problem of the dc link capacitor voltage imbalance; this problem increases complexity with an increasing number of levels. This imbalance degrades the operation of the inverter by increasing the voltage stress on the semiconductor devices and introduces harmonics and distorts the waveform of the output voltage.

The dc link capacitor voltage in the NPC inverter has to be controlled. In the case of two back-to-back-connected NPC converters, the two converters can share the task of balancing voltages on the dc-link capacitors [3]. However, such improvement strongly depends on the modulation indices and power factors of the two converters at the operating point. The dc link capacitor balancing using SVM is an attractive feature as it has a number of redundant states for the implementation of the balancing algorithm and it is suitable for improving the DC link utilization, reducing commutation losses. Some multilevel carrier PWM can be implemented using a single counter. The most attractive approach is to modify the inverter switching Pattern according to a capacitor control strategy to balance NP voltages [6] Although this approach requires a more elaborate control algorithm as compared with the previous methods, it provides an economical approach to tackle the main technical issues of the NPC three-level inverter. Karuppanan P *et al.* [8] use a single counter to generate time base for the modulation. However, it requires elaborate peripheral

circuit. José Darío Betanzos Ramírez *et al*, paper [7] proposed algorithm for a three-level Neutral-Point Clamped NPC) inverter is implemented on a Free scale DSP56F8037. a combination of several DSPs, On the

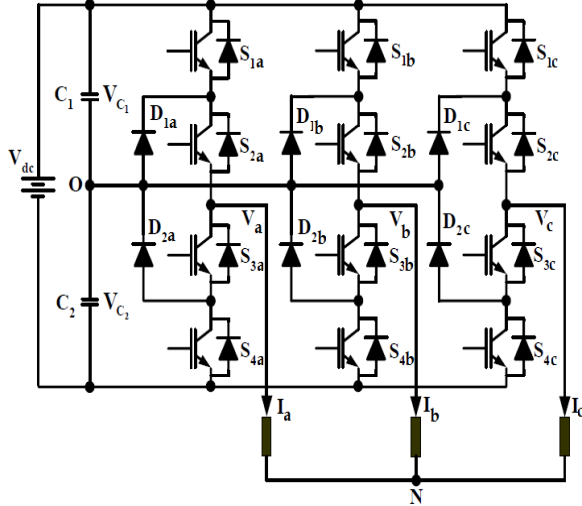


Fig.1. Circuit diagram for 3-level Neutral point diode clamped inverter (NPC-MLI)

In this paper propose, a proposed Space Vector PWM concept capable to balance the D.C link voltage in three level NPC MLI using redundancy state vectors and the effect of Switching Vector on the D.C link balance is obtained. Also the performance of this proposed modulation approach verified and Easily Implemented in FPGA IP core with reduced Timing calculation.

2. Implementation Of SVPWM

The basic idea of the SVPWM is bought from the operation of the induction motor. Traditionally in the induction motor the transformation of the three phase stator current into the two phase rotor flux is the basic formation of the space vector modulation. Space vector modulation (SVM) is an algorithm for the controlling the switching operation of the inverter. The space vector modulation mostly creates the AC waveforms to operate a 3-phase AC drives at variable speed [2]. The space vector modulation it used for the different controlling operations and for computational requirements. SVM utilize the available DC bus voltage by 15 % more than SPWM. One of the main research area for the development of high voltage and reduction of total harmonic distortion (THD) created by the rapid switching. Its Treats the sinusoidal voltage as constant amplitude vector rotating at constant frequency, It directly uses the control variable given by the control system and identifies each switching vector as a point in complex space [4]. Sector identification and triangle determination is to calculate the switching intervals for all vectors make SVM method quite

other hand, the proposed scheme can make use of existing two level SVPWM platform with minor modifications.

complicated.

A. For 3-level inverter

Any of the three phases n-level SVPWM can be divided into 6 sectors. For the n-level SVPWM consist of n^3 switching States there are 27 states for 3-level inverter. There are $(n-1)^2$ sub triangles available for each sector that means four triangles for the 3-level inverter as shown in fig.2.

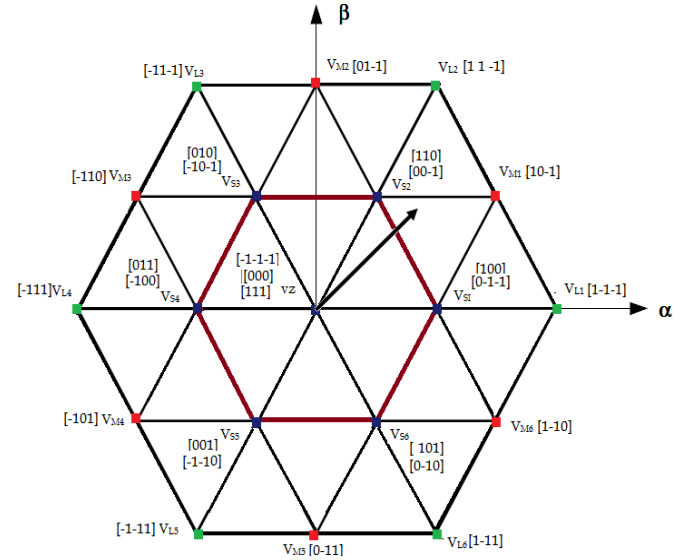


Fig.2. 3-level space vector pulse width modulation

The SVPWM uses the number of carrier waves to compare with the reference phase voltages signals depend upon n-level inverters. For the 3-level inverter the 27 switching states can be divided into the four vectors [4]. The vectors are zero, small, medium and large vectors. In the zero vectors consist of 1 vector and it has two redundant states. The small vector consists of 6 vectors and it has 6 redundant states. The medium and large vector each consist of 6 vectors. The space vector diagram of a three-phase three level consist three different switching states that are represented as 1,0,-1 to obtain the positive, zero, and negative switching sequences.

The space vector modulation treats sinusoidal voltage as constant amplitude vector rotating at constant frequency with reference voltage vector V_{ref} , defined by $V^* = |V_{ref}| e^{j\omega t}$, rotating around the centre of the space vector (SV) diagram at an angular frequency $\omega = 2\pi f_m$ [4,5]. The below contents explain the sector identification, triangle determination and on-time

calculations.

B. Sector identification

From the space vector modulation it is evident that rotating angle rotates at an angle of 0° to 360° . In space vector the angle is divided to form the six sectors all are identically same. According to this paper the sector identification based on the 2-level inverter. The space vector divided the rotating angle and divided the each sector with the phase angle difference of $\pi/3$. Implementation of this algorithm needs the reallocation of reference vector lying at any sector to sector 1 by rotating through $n\pi/3$ ($n=1, 2, 3, 4, 5, 6$) [4].

The sector can be identified using the formula (1) and rotating angle (2)

$$S_i = \text{int}(\theta/60) + 1 \quad (1)$$

$$\gamma = \text{rem}(\theta/60) \quad (2)$$

where θ is the angle of the reference vector with respect to α -axis, and int and rem represent standard function integer and remainder, respectively.

C. Triangle determination

After the sector identification the triangle determination is the most important one with respect to the magnitude and rotating angle α of reference vector V^* . Each sector in the 3-level inverter can be split into four triangles Δ_i , where $i=0,1,2,3$. The four triangle can be split into two types to simply the on-time calculations and for the easy determination of the triangle in the sector. The sub triangle can be categorized into type 1- base side of the triangle is at bottom and type 2- base side of the triangle at top side [4,5]. The triangle $\Delta_0, \Delta_1, \Delta_3$, belonged to the type 1 and the triangle Δ_2 , belong to type 2.

The triangle determination is important feature in the space vector modulation depend upon that only the on-time calculations and switching pulse can be generated. The triangle formed in the space vector modulation is the equilateral triangle. From the fig.2 it shows the reference vector at a magnitude of V^* and an angle of γ it may be lies in the any of the four sub-triangles. In the determination process the objective is to identify the where the V^* reference is located [6]. The search of the triangle of the small vector (V^*) can be narrowed down by using two integers k_1 and k_2 . They are defined by the coordinates ($V_{\alpha 0}, V_{\beta 0}$) of point V^* as

$$K_1 = \text{int}(V_{\alpha 0} + V_{\beta 0}/\sqrt{3}) \quad (3)$$

$$K_2 = \text{int}(V_{\beta 0}/h) \quad (4)$$

K_1 represents the part of the sector between the two lines joining the vertices, separated by distance h and inclined at 120° with respect to α -axis. From the fig.3 $K_1 = 0$ signifies that the point V^* is below line $X_1 X_2$. $k_1 = 1$ signifies that point V^* is between line $X_1 X_2$ and line $X_3 X_5$. K_2 represents the part of the sector between the two lines joining the vertices, separated by distance h and parallel to α -axis. $k_2 = 0$ signifies that the point P is between line $X_0 X_3$ and line $X_2 X_4$. $k_2 = 1$ signifies that the point V^* is above line $X_2 X_4$. Geometrically, the values of K_1 and K_2 are an intersection of two rectangular regions which is either a triangle or rhombus.

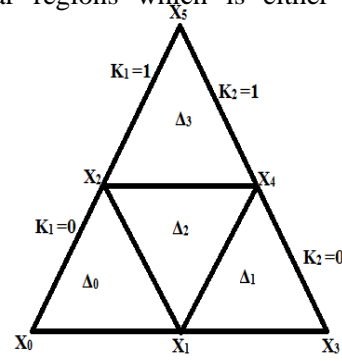


Fig.3. 3-level SVPWM sector-1 with sub-triangles

In other words, V^* the point lies in triangle (a) Δ_0 if $k_1 = 0$ and $k_2 = 0$, (b) rhombus $X_1 X_3 X_2 X_4$ (shaded) if $k_1 = 1$ and $k_2 = 0$, and (c) triangle Δ_3 if $K_1 = 1$ and $K_2 = 1$. The same analogy can be used for any level. In Fig. 3, the reference vector is located in rhombus $X_1 X_3 X_2 X_4$. This rhombus is made up of two triangles Δ_1 and Δ_2 . The point V^* can be located in any of the two. Let $(V_{\alpha i}, V_{\beta i})$ be the coordinates of the point V^* with respect to the point X_1 obtained as

$$V_{\alpha i} = V_{\alpha} - K_1 + 0.5 K_2 \quad (6)$$

$$V_{\beta i} = V_{\beta} - K_2/h \quad (7)$$

If $V_{\beta i} \leq \sqrt{3}V_{\alpha i}$ is true, then the point V^* is within the triangle Δ_1 , otherwise it is within the triangle Δ_2 .

The triangle type can be determined for the on-time calculation it is determine the adjacent vectors for the switching pulse generation.

For a type 1 triangle, the triangle number Δ_{ib} is obtained as (8)

$$\Delta_{ib}=K_1^2+2K_2 \quad (8)$$

For a type 2 triangle, the triangle number Δ_{it} is obtained as (9)

$$\Delta_{it}=K_1^2+2K_2 \quad (9)$$

To conclude, the triangle in a sector is found by an integer Δ_i . It is obtained by a simple logical expression. The triangle number Δ_i is formulated to provide a simple way of arranging the triangles, leading to ease of identification and extension to any level[4].

D. On-time calculations

The on time calculations can be obtained from the two level inverter. The sector consists of the 4 sub triangle. On-time calculation for any of the six sectors $S_i, i = 1, 2, \dots, 6$ is same, so let us consider the operation in sector 1 [6].

On-time calculation is based on the location of the reference vector V^* within a sector. (11)

$$V^* \delta_{S1} + V^* \delta_{S2} + V^* \delta_{M1} = V^* \quad (10)$$

$$\delta_{S1} + \delta_{S2} + \delta_{M1} = 1 \quad (11)$$

δ_{S1}, δ_{S2} and δ_{M1} are the calculated duty cycles of the switching vectors,

on- time calculations for the three level space vector modulation(12)(13)(14)

$$\delta_a = V_\alpha - V_\beta / \sqrt{3} \quad (12)$$

$$\delta_b = V_\beta / m \quad (13)$$

$$\delta_0 = 1 - \delta_a - \delta_b \quad (14)$$

3. Investigation of capacitor imbalance depend upon Switching Vector in 3 Levels-SVM

In the space vector modulation scheme the D.C link capacitor imbalance problem is investigated in the DC-MLI. In the proposed SVPWM the 27 switching states are properly utilized [5]. How the D.C link imbalance produced? The D.C link imbalance is produced due to the improper sharing of the voltage across the capacitor. The capacitor balance is achieved in the zero and large vectors. When inverter is operating in the state [000] the 3-phase shares the capacitor voltage due to that state obtains D.C link balance. Since other switching states like [111], [-1-1-1] the inverter is connected to positive or negative of D.C supply without using the voltage across the point

O. It is applicable for the large vector also [6]. According to the small vectors have $(-i_a + i_a = 0)$ and the medium vectors having some value of phase currents. While using the small vectors states like [100] the b & c phase utilizing the voltage across the point o. only the a-phase not using the voltage across the point O due to that phase current i_a will be available [9].

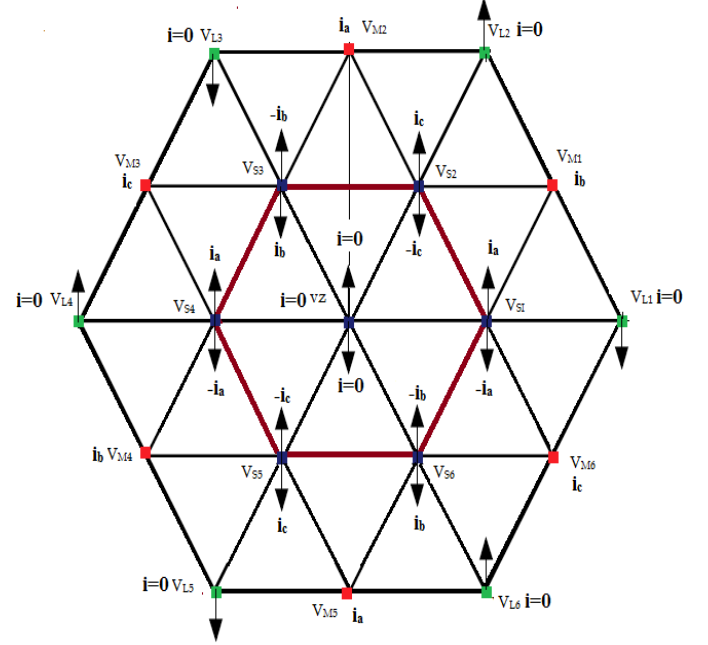


Fig.4. 3-level space vector pulse width modulation

By using the proper redundancy in the small vectors the D.C link balance can be achieved. In the medium vector the phase current i_b is available due to that D.C link imbalance will be occur. The Fig.4 shows the phase currents in the vectors. So the utilization of the middle vectors will not balance the capacitor. The Table.1 below shows the current value in sector 1 for all switching state [10].

| Vector (V_{Xi}) | State vector | Average i_{ph} |
|---------------------|--|-----------------------|
| V_{Z0} | $V_{0(000)}$ | 0 |
| V_{Si} | $V_{S1} = 1/2 \{ V_{S1(100)} + V_{S1(0-1-1)} \}$ | $-i_a + i_a = 0$ |
| | $V_{S2} = 1/2 \{ V_{S2(110)} + V_{S2(0-0-1)} \}$ | $-i_c + i_c = 0$ |
| V_{MI} | $V_{MI} = 1/3 \{ V_{S1(0-1-1)} + V_{M1(101)} + V_{S2(110)} \}$ | $i_a + i_b + i_c = 0$ |
| V_{Li} | $V_{L1} = V_{L1(1-1-1)}$ | 0 |
| | $V_{L2} = V_{L2(1-1-1)}$ | 0 |

Table.1. Phase currents according to sector 1

The redundant states of a vector produce the same According to the table.1 the phase currents in the zero, short, medium and large states are shown. The state zero and large vector has the zero phase current. While going for the short vectors without using redundancy the positive or negative phase currents available in that switching state due to that capacitor is in imbalance [10]. By the proper redundancy in the short vectors the phase current in the short vector also become zero the capacitor balance can be achieved. The switching pulse for the sector 1 in triangle Δ_0 is shown in fig.5.

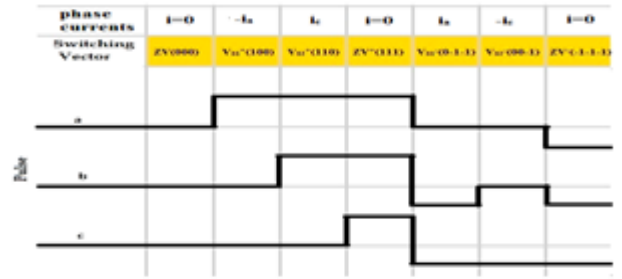


Fig.5. SVPWM Switching Pulse for Sector 1 - Δ_0

4. The proposed SVPWM IP Core

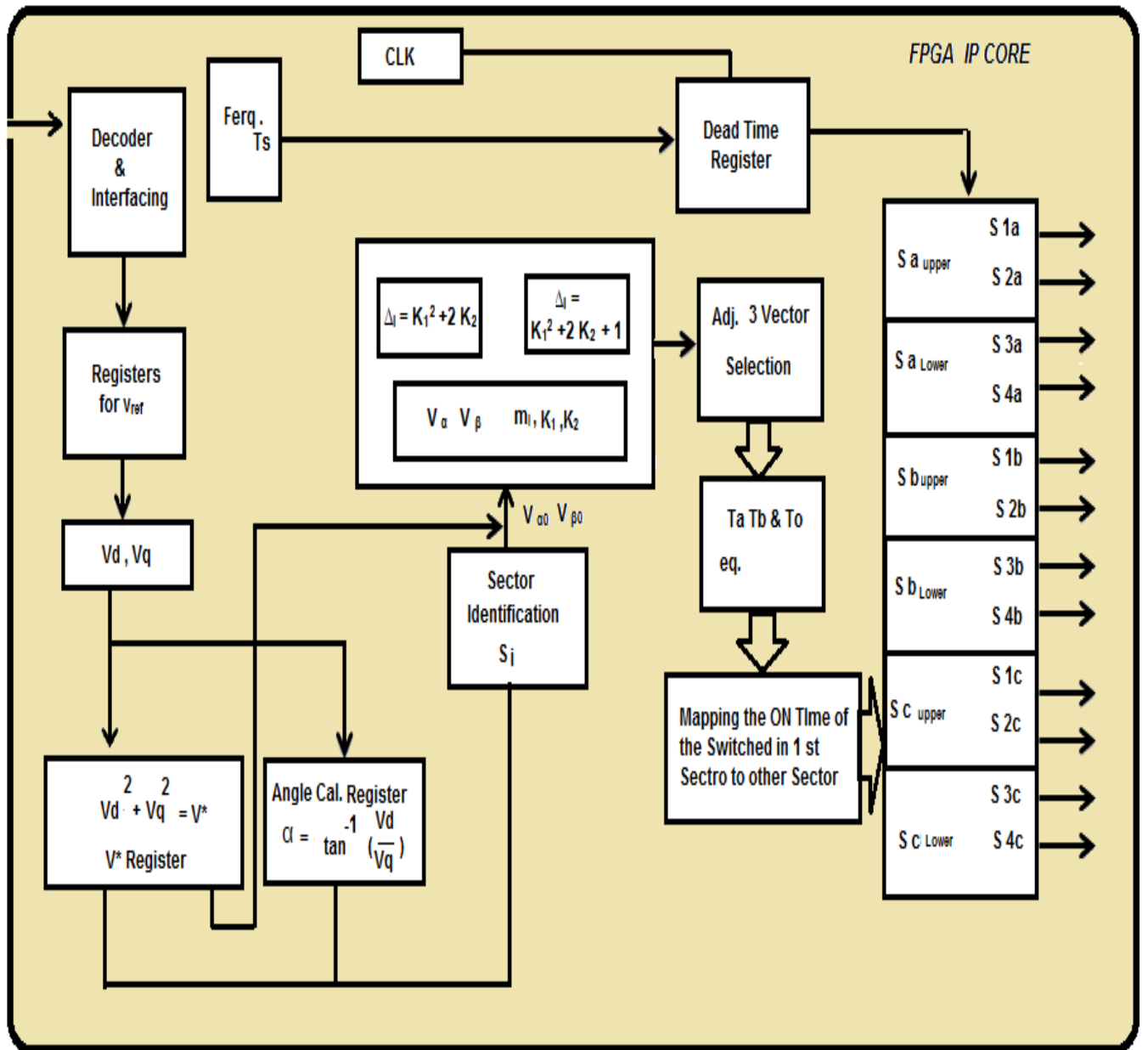


Fig.6. SVPWM IP Core Block diagram

1) *Component freq.*: This is block for the selection of the switching frequency that calculates the switching period T and the dead time T_d by using four-channel multiplexer [11].

2) *V_{ref} Register Block*: This component implements the following abc/dq transformation: Fig. 6 shows the Simulink models used to describe the components and to generate their VHDL description files

3) *Sector Identification Block*: from angle α finds the Sector, its use the look up table

4) *Switching vector selection*: Using sector S_i and Sub triangle Δi the 2D look-up table where created using VHDL code the selected Switching Sequence stored in the lookup table.

5) *Component dead time*: This block generates the inverse of the trigger signals adding the corresponding dead time. It was implemented using an edge detector together with counter [12].

6) *PWM Drive Block*: The implementation of the Component SVPWM is very similar the 50-MHz master clock of the S3 board was divided by using the Digital Clock Manager of the FPGA in order to obtain a 10-kHz clock. That clock allows generating the PWM signals with a time precision of 0.1 μ sec. Due to the fact that vector times are 8-b wide, the maximum switching frequency available in this system is 39.2 kHz [11].

7) *Protection circuit*

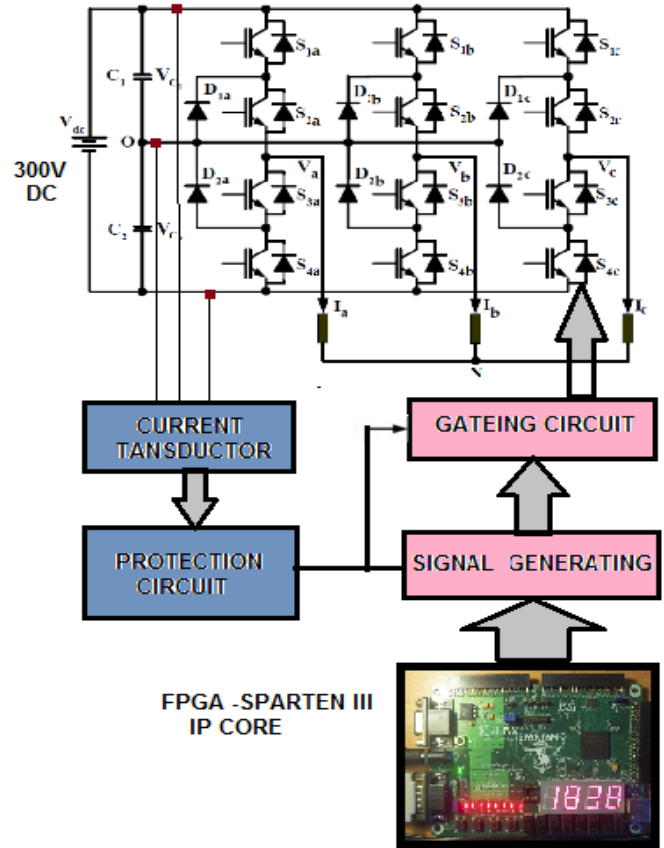
Three Hall-effect current protection circuits is used. The sensors were fitted in such a way all possible overcurrent faults are detected. Once an overcurrent has been detected the three-level inverter is disabled by means of an input “shutdown SD” of the circuit’s.

5. HARDWARE IMPLEMENTATION

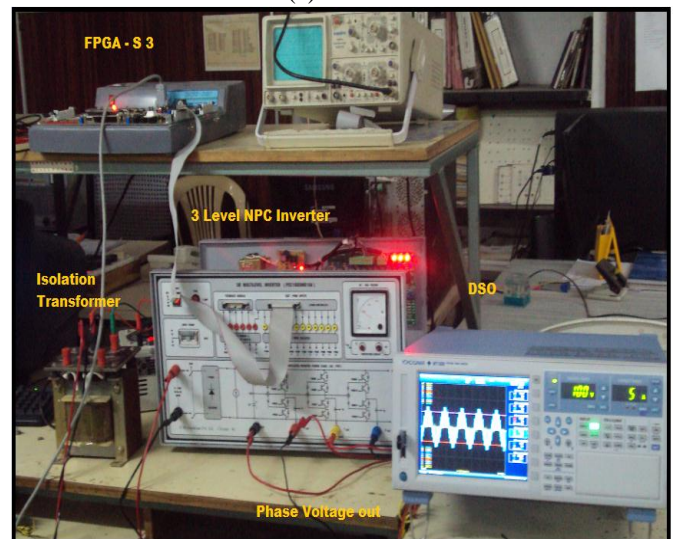
This board is separately designed for a high performance power electronics controller with more than 1000 MIPS. This board consists of the latest floating point DSP processor 6713, Four Nos. of high speed ADC 16 MSPS. DSP Processor on TI’s TMS320C6713, the highest performance floating point DSP, 28K x 16 bit RAM for Program memory, 64K x 16 bit RAM for Data memory USB Interface [11, 12].

FPGA for PWM Generations: Spartan 3 of 400K gates, 16 PWM outputs (Isolated) 24 Isolated Digital I/Os, 8 Capture Isolated Inputs 16 Output LEDs, One 34 Pin header is provided to

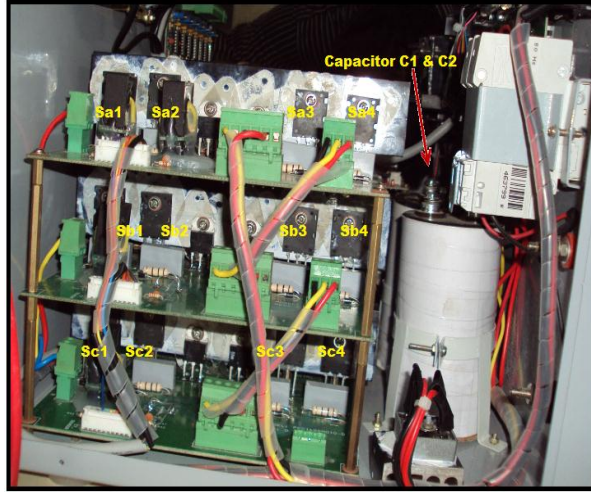
This board hosts FPGA from Xilinx, which has 4,320 logic cells, each constituted by two 16×1 lookup tables (LUTs) and two flip-flops. This FPGA also has twelve 18×18 hardware multipliers, as well as twelve 18-kb block random access memories [13, 14].



(a)



(b)



(c)

Fig.7. Experimental test setup. (a) Diagram. (b) Hardware set up Photograph (c) 12 switches NPC-MLI with DC Link capacitor.

Although FPGAs allow a great degree of freedom, Operations are done with a 10-MHz clock, which is enough frequency to achieve a real-time operation in this algorithm. A tradeoff between precision and area led to choose 8 bite for the input variables: vd , vq , and θ . The Pulse module connected to MLI Switches through the gating drive .the protection connected in the input side to prevent the circuit from any fault. for 2.2Kw, 1440 r/min Induction motor with a rated voltage of 380 V& current of 5 A. An open loop constant v/f control is used to regulate the motor speed .

7. SIMULATION RESULTS

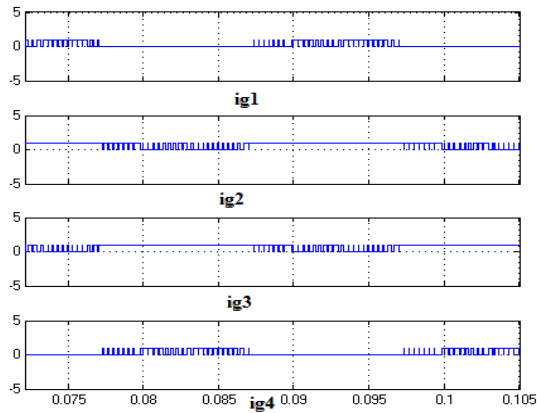


Fig.8. SVPWM switching pulse leg (Sa1,Sa2,Sa3,Sa4)

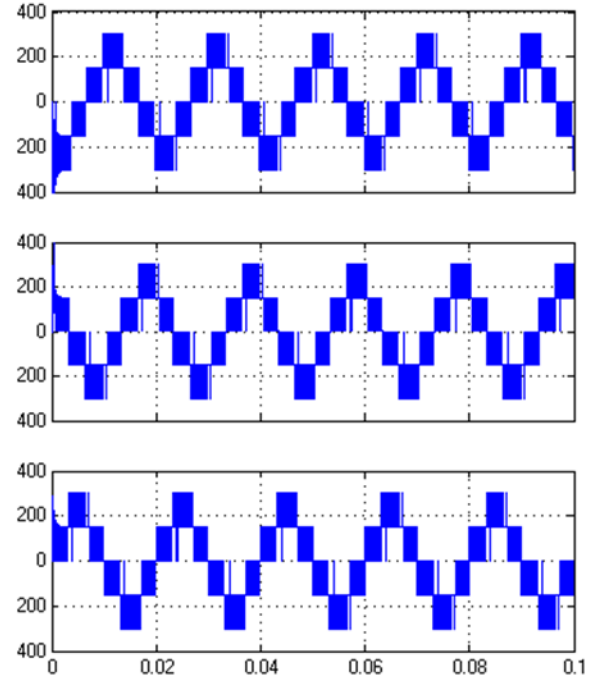


Fig.9. Mat lab simulation result: Line-to-line voltage at $f_s = 1$ kHz and $m = 0.8$

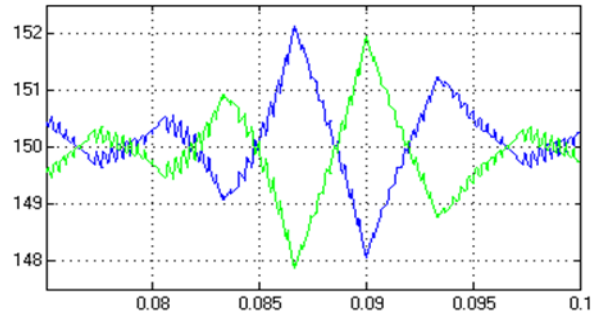
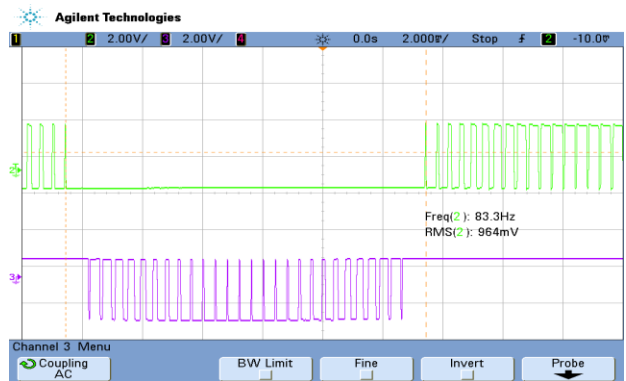
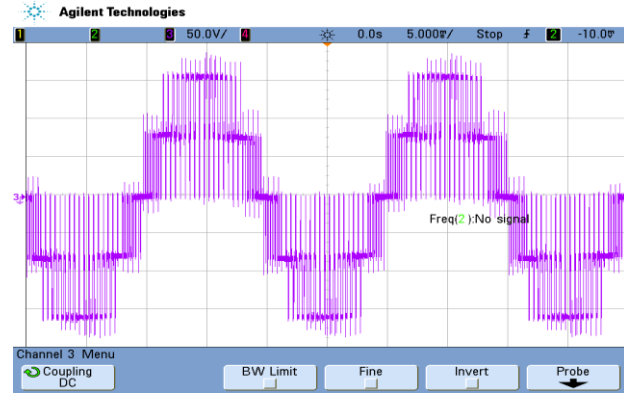


Fig.10. Mat lab simulation result: DC Link Capacitor Voltage V_{c1} & V_{c2} using propose SVM switching $f_s = 1$ kHz and $m = 0.8$ With reduced Capacitor imbalance of 0.25%

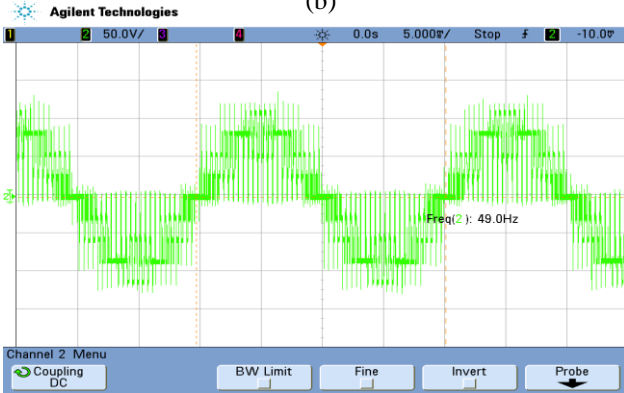
6. HARDWARE RESULTS



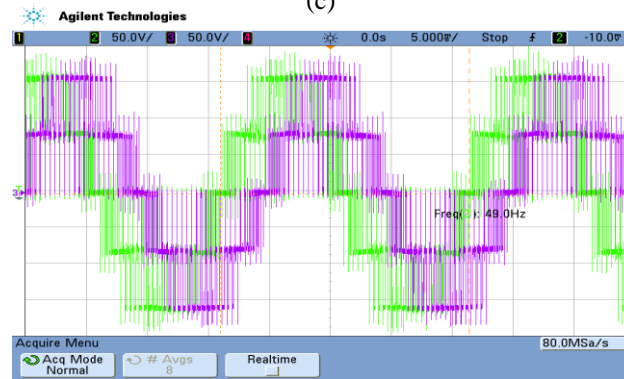
(a)



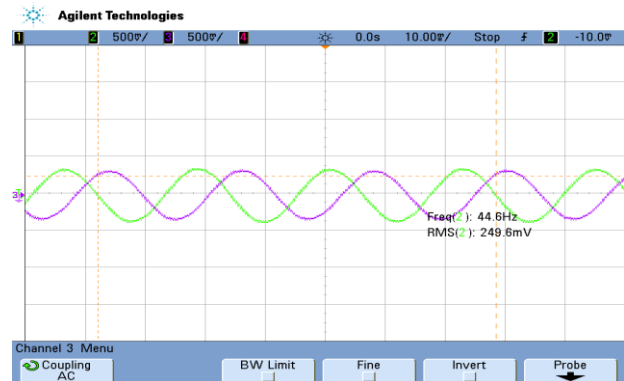
(b)



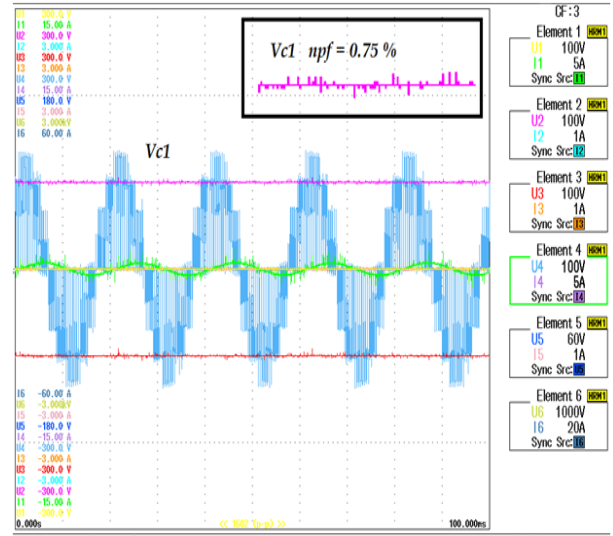
(c)



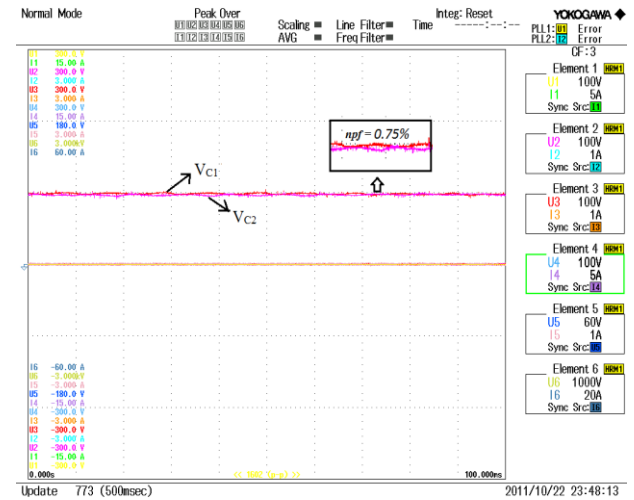
(d)



(e)



(f)



(g)

Fig.11. Experimental results: 3 –level DCMLI :
 (a) SVM Pulse Sa1 & Sa3 (b) Line-to-line voltage at $f_s = 1$ kHz and $m = 0.8$; 5ms/div, 50V/div. (c) Line-to-neutral voltage at $f_s = 1$ kHz and $m = 0.8$; 5ms/div, 50V/div. (d) V_{an} , V_{bn} Line-to-line voltage with 120 degree phase shift at $f_s = 1$ kHz and $m = 0.8$; 5ms/div, 50V/div,(e) i_a , i_b Line-current with 120 degree phase shift at $f_s = 1$ kHz and $m = 0.8$; 5A/div, 5ms/div.(f) Line-to-line voltage at $f_s = 1$ kHz and $m = 0.8$ with 0.75% Capacitor balancing(g) Experimental results for V_{c1} and V_{c2} [50 V/div], and $V_{dc} = 300V$, $m = 0.907$, $f = 50Hz$, $C_1 = C_2 = 100$ micro Farad, Proposed NSTV-SVM, $f = 5$ kHz

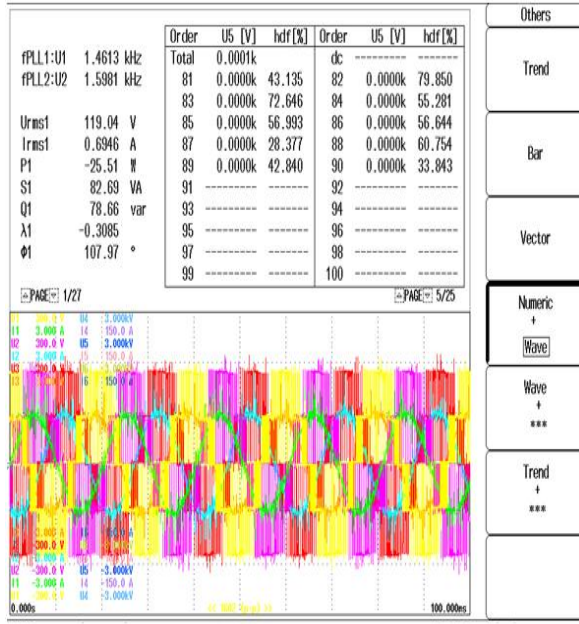


Fig.12. Experimental results: 3 –level DCMLI: 3 phase Line-to-line voltage and current at $f_s = 1$ kHz and $m = 0.8$; 5ms/div, 50V/div, 3 A/div.

7. EXPERIMENTAL RESULTS

With the aim of validating the SVPWM algorithm an experimental setup was built (see Fig. 7) and a validation test procedure was performed using FPGA –SPARTEN III IP – CORE. The experimental validation test consisted of executing the simplified SVM algorithm to make the reference vector follow a trajectory, as illustrated in Fig. 11. The validation algorithm generates a sinusoidal signal and stepwise waveform by means of digital to analog converters. The stepwise signal represents the areas the reference vector goes through when the SVM algorithm is applied. The proposed Simple SVPWM scheme based on 2 Level inverter has done using VHDL and simulated using Modelsim 5.9e , verified and the same. Synthesized using Xilinx SPARTEN and its also tested. Switching state for the Simple SVM scheme with capacitor balancing is mapped in 2D look up table.

The 12 SVM pulses fig.7(c) of the 3 Level MLI is given through gating driver to Diode Clamped Multilevel Inverter with 300 V DC Link, Two 100Micro F Capacitor, 1KHZ Switching frequency and 0.866 modulation index. The validated results are captured using 2 channel– Agilent Technology and 6 channel YOKOGAWA –DSO .fig (b),(c) show Line& phase voltages ,These voltages were

obtained by using the simplified SVM algorithm with a switching frequency (f_s) of 1kHz and modulation ratio of 0.866 and fig. 11(f) shows the live – live voltage with reduced 0.75 % percentage of capacitor unbalancing.the inverter never changes directly between states P and N without passing through 0.The line-to-line voltage has five voltage levels $+2V_{dc}$, $+V_{dc}$, 0 , $-V_{dc}$ and $-2V_{dc}$. Finally, the line-to-neutral voltage has nine voltage levels $+4V_{dc}/3$, $+V_{dc} + 2V_{dc}/3 + V_{dc}/3$, 0 , $-V_{dc}/3$, $-2V_{dc}/3$, $-V_{dc}$, and $-4V_{dc}/3$.From the voltage waveforms it can be concluded that the SVM algorithm and the circuit control of the inverter are working well.

The following are the striking features of the proposed scheme.

- 1) In the proposed SVPWM scheme gives the computations free. The Processing Unit remains the same for any level.
- 2) On-time calculation equations do not change with traditional approach as in [5], it saving storage space.
- 3) The computations required by the PU are significantly lesser than the other exiting methods [6]
- 4) The sub Triangle number Δj is easily identified as an integer using (12) or (13) for any level.
- 5) The scheme is based on a 2-level SVPWM. Therefore, an existing 2-level SVPWM module can be easily adapted to the any MLI.
- 6) The proposed method can be easily implemented using a commercially offered motion-control like DSP or microcontroller.
- 5) The proposed scheme also balancing the capacitance (reduced DC Link fluctuation up to 0.75%).

7. EXPERIMENTAL RESULTS

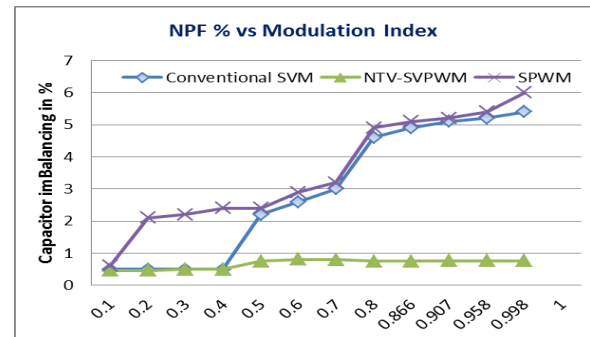


Fig.13.% of DC-link imbalance chart verses Modulation index for SPWM, Conventional SVM & Proposed NTV-SVPWM

Fig.13. gives comparison of steady npf % for different PWM schemes with the proposed NTV –SVPWM scheme at different modulation index, in the range of 0.45 to 0.907. proposed NTV SVM scheme reduces the percentage of npf to 0.75%(which is well below the IEEE standards) and the THD% to 10.882%. In addition to this, the same NSTV - SVM scheme can be extended to over modulation region (modulation index more than 0.907) with small changes in duty cycle calculations and vector participation .

8. CONCLUSION

A simple SVPWM algorithm for a 3 NPC multilevel inverter based on a standard two-level inverter has been proposed. The computations do not increase with level. The proposed method can be easily implemented using a commercially available motion controls or microcontroller, which normally supports only two-level modulation. The main advantage of the proposed scheme over earlier schemes is that, it provide voltage reference in $\alpha-\beta$ coordinates, the proposed scheme uses most of the two level calculations and adapts to any n -level inverter. The scheme has been implemented for three-level NPC and it can be extended to any level. The scheme can be used for both enhanced performance of NPC MLI and with Capacitor balancing. The scheme can be easily extended to include over modulation range.

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